ANALYSIS AND DESIGN OF SINGLE-PHASE GRID-CONNECTED BATTERY INVERTER USING DUAL ACTIVE BRIDGE DC-DC CONVERTER

AKEKACHAI PANNAWAN

A Thesis Submitted to the Graduate School of Naresuan University
in Partial Fulfillment of the Requirements
for the Doctor of Philosophy in Renewable Energy
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By Akekachai Pannawan

has been approved by the Graduate School as partial fulfillment of the requirements for the Doctor of Philosophy in Renewable Energy of Naresuan University

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Title	ANALYSIS AND DESIGN OF SINGLE-PHASE GRID-CONNECTED BATTERY INVERTER USING DUAL ACTIVE BRIDGE DC-DC CONVERTER
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Academic Paper	Ph.D. Dissertation in Renewable Energy, Naresuan University, 2023
Keywords	Dual Active Bridge (DAB) DC-DC converter, LCL-filtered Voltage Source Converter (VSC), Battery storage; DC-DC converter; solar photovoltaic.

ABSTRACT

Combining residential energy storage with solar photovoltaic (PV) power generation within low-voltage distribution networks holds promise for attaining energy self-sufficiency. This research presents the design and implementation of such an approach using a 3-kW single-phase grid-connected battery inverter. The inverter pairs a 51.2-V lithium iron phosphate battery pack witha 220-V, 50-Hz grid. Its prototype design incorporates both an LCL-filtered voltage source converter (VSC) and a dual active bridge (DAB) DC-DC converter, both operating at a 20 kHzswitching frequency.

The VSC employs a swift DC bus voltage control strategy alongside a comprehensive approach to mitigate current harmonics. Similarly, the DAB DC-DC converter integrates a proportional-integral regulator to efficiently manage the average battery current, incorporating dynamic DC offset mitigation for the medium-frequency transformer's currents within its single-phase shift modulation scheme. The control strategies for both converters are executed on a 32-bit TMS320F280049C microcontroller within the same interrupt service routine, demonstrating the integration of control systems to enhance performance. This study introduces a synchronization technique aligning the switching signal generation of both converters with the sampling of analog signals for the control system, ensuring coordinated operations.

The prototype inverter exhibited exceptional performance, achieving an efficiency exceeding 90% and maintaining total harmonic distortion in the grid current below 1.5% at a battery power output of ±1.5 kW, suggesting its potential to enhance grid stability and energy efficiency.

ACKNOWLEDGEMENTS

First and foremost, I extend my deepest gratitude to my thesis advisor, Associate Professor Dr. Sakda Somkun, for their unwavering support, insightful guidance, and invaluable advice throughout this research journey. Their expertise and encouragement were pivotal in shaping both the direction and success of this work.

I would also like to express my sincere thanks to the members of my thesis committee. Your constructive feedback, thoughtful criticisms, and engaging discussions have significantly contributed to refining my research. The depth and breadth of your expertise have enriched this work in countless ways.

I am immensely grateful to my lab mates and colleagues at Sepcon/SGtech for creating a stimulating and supportive work environment. Your camaraderie and collaborative spirit have made all the difference in my research experience. Working alongside such dedicated individuals has been both an honor and a pleasure.

To my friends and family, who have provided endless encouragement, understanding, and patience throughout the ups and downs of this academic pursuit: your belief in my abilities and unwavering support have been my strength during challenging times. I cannot thank you enough for standing by me every step of the way.

Finally, I want to express gratitude for the financial assistance provided by The Royal Golden Jubilee (RGJ) Ph.D. Program (Grant no. PHD02282560), which played a vital role in supporting my research and academic pursuits. This funding not only supported my studies but also created opportunities that were pivotal in finalizing this thesis.

This thesis stands as a testament to the collective effort and encouragement of all who have been part of this journey. Your contributions and support have been invaluable, and for that, I am forever grateful.

Akekachai Pannawan

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CHAPTER I

INTRODUCTION

Introduction

In the quest for the innovative solutions that facilitate the integration of the renewable energy to enhance power management in residential settings, the demand of compact, efficient, and reliable power conversion systems has led to the development of tailored designs for small-scale applications. This study focuses on two-stage, single-phase, grid-connected low-voltage (LV) battery inverter, which is specifically designed to meet the energy requirements of small residential applications. The central of this system is the dual-active bridge (DAB) DC-DC converter, which employs phase-shift modulation strategies to achieve bidirectional power flow and isolation for the LV battery pack. Complementing the DAB converter, the integration of LCL-filtered grid-connected voltage source converters (VSCs) enhance the system's capability to deliver clean and stable power from the grid to homes and vice versa. This introduction paves the way for the in-depth examination of the system's design, the operational efficiency, and the pivotal role, that plays in advancing residential power management and renewable energy adoption.

The Dual Active Bridge (DAB) DC-DC converter exemplifies the interest in power conversion technology, merging efficiency, reliability, and flexibility into a remarkably compact form factor, distinguished by its dual full-bridge architecture and the DAB converter enables bidirectional power flow. This capability makes it exceptionally suitable for the wide array of applications that demand a high efficiency and a precise power control across extensive ranges. Its operation at elevated switching frequencies facilitates the utilization of smaller magnetic components, therefore, diminishes both of dimensions and expenses, while maintaining its performance.

A standout feature of the DAB converter is its proficiency in achieving zero-voltage switching (ZVS) over a broad load range. This ability drastically cuts down

not only switching losses, but also substantially boosting the system's overall efficiency. Coupled with its effective phase-shift modulation technique, the converter ensures a smooth power transfer control. This contributes to enhance the refined and stabled power output, in addition to epitomize technical finesse in managing energy flows.

The converter's adaptability is showcased in its broad spectrum of applications, ranging from electric vehicle charging infrastructures and the integration of renewable energy to enhancing grid stability and providing solutions for energy storage. Its efficiency in converting and regulating power between varying voltage levels plays a pivotal role in the seamless incorporation of renewable energy sources into the grid. This integration is crucial in steering the energy sector toward more sustainable practices.

Furthermore, the design of the DAB DC-DC converter incorporates sophisticated control strategies, which allow for dynamic adjustments in response to shifting loads and operational conditions. This flexibility guarantees sustained optimal performance and reliability, even amidst fluctuating power demands, encapsulating the essence of cutting-edge power electronics engineering.

Ultimately, the Dual Active Bridge DC-DC converter is a tribute to the advancements in power conversion technology. Its harmonious blend of efficiency, flexibility, and adaptability establish as a foundational element in the development of energy-efficient and environmentally friendly power systems. This marks a considerable stride towards achieving energy optimization and underscores a committed effort in environmental stewardship.

Background and Significance of the Study

The widespread adoption of renewable energy had transformed electrical generation and distribution systems into the distributed generation system (Lasseter, 2011). Generation sites were located based on the availability of renewable energy resources, e.g. wind, solar, small hydro, together with the conventional centralized power plants, e.g. natural gas, coal, nuclear etc. Energy storage devices such as batteries, hydrogen-fuel cells, pumped hydro storage systems, etc. were commonly used to overcome the intermittency such renewable energy sources (Boicea, 2014)[2]. Battery electric vehicles (BEVs) and plug-in hybrid electric vehicles (PHEVs) were also integrated into the electricity grid to utilize the cleaner renewable energy sources (Boulanger et al., 2011). In addition, energy stored in the BEVs and PHEVs could be used to support the grid when the demand was greater than the generation and reactive power injection for voltage regulation with the so-called vehicle to grid (V2G) operation (Falahi et al., 2013). The Smart grid system had been introduced to cope with the uncertainties of demand response and the variable generation of renewable energy sources (Kezunovic et al., 2012). One of the key characteristics of the smart grid was to accommodate of all power generation and storage options (Kezunovic et al., 2012). Thailand is also aware of the global context in the renewable generation and smart grid. According to the alternative energy development plan (*Alternative Energy Development Plan: AEDP2018*, 2018), Thailand had set a target that the share of renewable energy in the electricity production should increase from 9.87% in 2014 to 20.11% in 2036. Thailand smart grid development plan (2015 - 2036) had been also launched to ensure energy security, to improve system reliability and power quality, and increase energy efficiency. Several smart grid pilot projects would be implemented throughout the country (*Thailand Smart Grid Master Plan (2015-2036)*, 2015). EGAT, MEA and PEA are the key players in this smart grid plan.

Power electronic converters now play the vital role in the modern electric generation and distribution systems (Liserre et al., 2010)[8]. They are used to converse the AC variable voltage variable frequency (VVVF) sources/storages (wind, hydro, flywheel, etc.) and DC variable voltage (VV) sources/storages (photovoltaic, fuel cell, electrolyser, battery etc.) to AC constant voltage constant frequency

(CVCF), for delivering power to the utility grid. The most commonly used circuits are the voltage source AC-DC converters and DC-DC converters (De Doncker et al., 1991). Among these dual active bridge (DAB) DC-DC converters shown in Fig.1 are the most promising topology that gains attention from research communities. The basic principle is each bridge generates a square wave voltage to the transformer windings and the power transfer is controlled by the phase difference between the two voltage waveforms. The advantages of the DAB converters can be listed below (Kheraluwala et al., 1992):

- Bidirectional power transfer capability
- Zero voltage switching (ZVS) operation for efficiency enhancement
- Galvanic isolation through the high-frequency transformer
- High power density with the AC-link high-frequency voltage through the high-frequency transformer
- Easy voltage matching via the transformer turn ratio
- Fault current is limited with the auxiliary/leakage inductor (Harrye et al., 2015)[12].

The DAB DC-DC converters were widely used in solid state transformers (She et al., 2013)[13], on-board battery chargers of EVs and PHEVs (Xue et al., 2015), grid-connected battery converters (Inoue & Akagi, 2007a), railway traction systems (Baars et al., 2014), power conditioner circuits for fuel cells and photovoltaic modules with a high voltage step-up ratio (Cacciato et al., 2010), and uninterruptable power supplies (Zhao et al., 2013). Research on the DAB DC-DC converter could be mainly classified into three directions. First, control and modulation strategies had been developed so as to increase the efficiency and power factor of the high-frequency transformer (Jain & Ayyanar, 2011). The second approach was the application of wide-band gap semiconductor devices, mainly SiC IGBTs and SiC MOSFET (Zhao et al., 2014), as the power switches operating at a higher frequency in order to enhance the efficiency and power density. The third approach direction was the development of topology variants such as multi-input isolated DC-DC converter (Zhao et al., 2014), or three-phase DAB DC-DC converter (Waltrich et al., 2016) for high power applications with low ripple currents.

The high-frequency transformer and auxiliary inductor are the key components of the DAB DC-DC converter along with the two bridges. Ferrite materials were commonly used in transformers and inductors (Zhao et al., 2008). Iron-based nanocrystalline materials with a higher saturation induction and lower loss were also used as the transformer cores of the DAB converters (Inoue & Akagi, 2007a). Air-core inductors were commonly used in high power DAB DC-DC converters. Iron powder materials with higher saturation induction and lower permeability than the ferrite cores are also another choice for high-frequency inductors in power switching converters, which was found to be more compact than the ferrite cores (Rafiq et al., 2013). However, No direct comparison of high-frequency magnetic materials for the DAB converters has been made.

Thus, this project aims to explore the applications of high-frequency materials for the transformers and auxiliary inductors of the DAB DC-DC converters. As indicated in figure1. Commercial and custom-made iron powder cores will be used to construct the auxiliary inductors. Commercial nanocrystalline materials will be selected for the transformers. Comparisons with the commonly used ferrites materials will be made. Lower losses and less core volumes lead to a higher efficiency and power density. This project is beneficial for the electronic, renewable energy and power transformer industry of Thailand. The knowledge obtained from this research can be transferred to the industry sector, therefore our domestic production of power converters can be competing with the imported products.

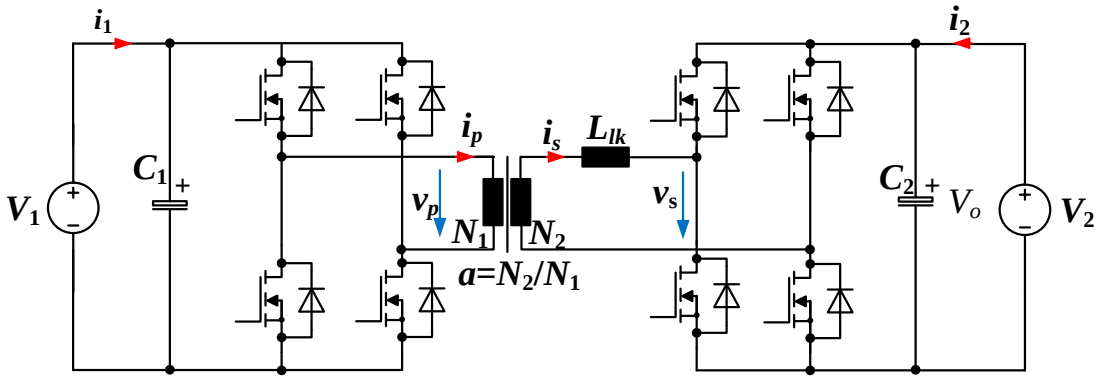


Figure 1 Dual active bridge DC-DC converter.

Objectives of the Study

1. To develop a Single-phase Grid-connected Voltage Source Converter (VSC) utilizing a full bridge topology.
2. To design and build a bidirectional isolated DC/DC converter based on a dual active bridge (DAB) configuration.
3. To develop and implement an advanced control strategy for a bidirectional isolated DC/DC converter using the Dual Active Bridge configuration, in addition to a single-phase grid-connected inverter employing a Voltage Source Converter (VSC).

Scope of the Study

1. Develop a Single-phase Grid-connected Voltage Source Converter (VSC) utilizing a full bridge topology. This involves the design and implementation of a converter capable of efficiently converting alternating current (AC) to direct current (DC) and vice versa, utilizing a full bridge configuration.
2. Design and construct a bidirectional isolated DC/DC converter based on a dual active bridge (DAB) configuration. The focus will be on creating a converter capable of bidirectional power transfer with isolation, using the DAB topology to achieve high efficiency and reliability.
3. Develop and implement an advanced control strategy for the bidirectional isolated DC/DC converter employing the Dual Active Bridge configuration. Additionally, integrate this control strategy with a single-phase grid-connected inverter utilizing a Voltage Source Converter (VSC). This involves developing sophisticated control algorithms to manage power flow and ensure stable operation in both the DC/DC converter and the grid-connected inverter.

Significance of the study

The study's significance is rooted in its contribution to the advancement of power conversion technologies and energy management strategies, which are essential for the integration of renewable energy sources into the power grid and the development of more efficient and sustainable energy systems. Below is a refined presentation of the study's significance:

1. The study introduces a Single-phase Grid-connected Voltage Source Converter(VSC) , improving conversion efficiency. This is the key for integrating renewable energy, supporting energy storage, and enhancing electric vehicle charging, thereby promoting more sustainable energy use by reducing losses.
2. The development of a bidirectional isolated DC/DC converter based on a dual active bridge (DAB) enables safer, more efficient power transfer across voltage levels. The Essential of high-safety, low-noise applications such as renewable energy and electric vehicles, promotes wider adoption.
3. Implementing a control scheme for the isolated Dual Active Bridge (DAB)converter and a Voltage Source Converter (VSC), the study improves energy flow and grid stability with renewable sources. This supports reliable renewable use and smarter energy management, crucial for smart gride advancements.

CHAPTER II

LITERATURE REVIEW AND BASIC THEORY

Literature review and basic theory

Integrating solar PV and battery storage into low-voltage distribution networks can be done using different configurations. One approach involves connecting the battery storage to the solar PV at the DC side of the grid inverter, as illustrated in Figure 2. Such configurations are known as DC-coupled solar PV-battery hybrid inverters. Typically, the voltage of the DC bus exceeds that of the PV, requiring the use of non-isolated boost DC-DC converters to match the PV string voltages with the DC bus voltage. The control system of the boost DC-DC converter incorporates maximum power point tracking (MPPT) to optimize performance. (Ahmed et al., 2022; Ko et al., 2020). A high voltage (HV) battery pack can be directly linked to the DC bus of the grid inverter, as depicted in Figure 2a (Galkin et al., 2021). For successful connection, the battery's voltage needs to exceed the grid inverter's minimum voltage requirement, which is the peak grid voltage for a single-phase system or the peak line-to-line voltage for a three-phase system. Additionally, an HV battery pack may be connected to the DC bus through a non-isolated DC-DC converter, as illustrated in Figure 2b. Usually, a bidirectional buck-boost DC-DC converter facilitates a broad battery voltage spectrum (200 V – 500 V), while ensuring the DC bus voltage remains above the grid-interfaced inverter's minimum threshold. Additionally, a battery pack necessitates an electronic battery management system (BMS) for the purpose of voltage equalization, overseeing, and safeguarding the galvanic cells. (Cao & Emadi, 2011). Hence, high-voltage battery storage solutions featuring intricate battery management systems (BMS) may be appropriate for select residential applications. On the other hand, for smaller homes (below 5 kW), low-voltage battery storage (below 100 V) with a simpler and more cost-effective BMS presents a viable alternative, as shown in Figure 2c.(Galkin et al., 2021). The low-voltage (LV) battery pack connects to the DC bus via a bidirectional isolated

DC-DC converter that uses a medium frequency (MF) transformer (20-150 kHz) to align the voltage of the LV battery pack with that of the DC bus. (Biao et al., 2014; Somkun et al., 2021). Battery storage can be incorporated into the low-voltage (LV) network using the AC coupling configurations depicted in Figure 3. Differing from the DC coupling arrangements depicted in Figure 2, which illustrates various examples of DC-coupled grid-connected photovoltaic-battery hybrid inverters, such as: (a) a high-voltage (HV) battery making a direct connection to the DC bus; (b) an HV battery connected to the DC bus via a non-isolated DC-DC converter; and (c) a low-voltage (LV) battery attached to the DC bus through an isolated DC-DC converter. The AC coupling strategy, on the other hand, incorporates a grid-interfaced inverter specifically for the battery systems and facilitates the flow of power between the solar photovoltaic system. (P_{PV}), battery power (P_{Batt}), load power (P_L), and grid power (P_g) at the AC point of common coupling (PCC). However, AC coupling topologies are less efficient than their DC counterparts due to the additional conversion stage involved. (Lo Franco et al., 2021). However, AC coupling systems, as shown in Figure 3 which presents examples of AC-coupled grid-connected photovoltaic-battery hybrid inverters, including: (a) a single-stage high-voltage (HV) battery inverter; (b) a two-stage HV battery inverter; and (c) a two-stage low-voltage (LV) battery inverter, can be deployed with existing grid-connected PV inverters or independently of any PV inverters. They serve functions such as energy arbitrage or the reduction of peak load demand. (Galkin et al., 2021). Two-stage AC-coupled low-voltage (LV) battery inverters, depicted in Figure 3c, are commonly employed in small residential environments with power needs under 5 kW. These power conversion stages and the battery pack can be integrated into a single, unified unit.("Duracell Energy Bank," 2024; "What to Expect for Powerwall 3," 2024).

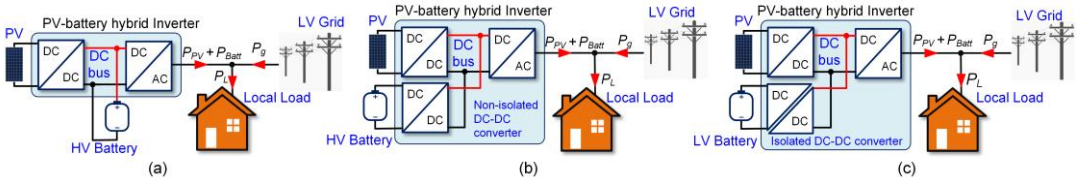


Figure 2 DC coupling grid-connected PV-battery hybrid inverters: (a) Direct connection of the HV battery to the DC bus.

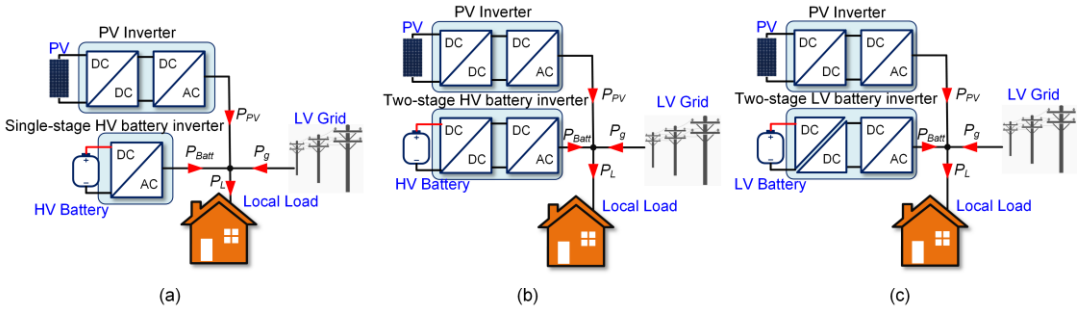


Figure 3 AC coupling grid-connected PV-battery hybrid inverters.

This research centers on a two-stage, single-phase, grid-connected low-voltage (LV) battery inverter designed for small-scale residential use. Typically, a dual-active bridge (DAB) DC-DC converter, utilizing phase-shift modulation techniques, serves as the bidirectional isolated DC-DC converter for the LV battery pack. For the grid-interfaced inverter, LCL-filtered grid-connected voltage source converters (VSC) are often chosen. Nonetheless, the efficiency may drop due to a limited zero-voltage switching (ZVS) range of the DAB DC-DC converter, especially when the voltage ratio across its terminals strays from its nominal value. (Kheraluwala et al., 1992). The efficiency of the dual-active bridge (DAB) DC-DC converter can be improved by integrating resonant networks with the medium frequency (MF) transformer, thereby expanding the range of zero-voltage switching (ZVS). (Jin et al., 2023; Zhou & Sun, 2022). The power transfer in the resonant dual-active bridge (DAB) DC-DC converter can be regulated by adjusting the switching frequency, a method that proves to be more complex than the fixed frequency operation seen in traditional DAB DC-DC converters. Additionally, the DAB DC-DC converter is prone to issues arising from an imbalance in the voltage-second applied to the medium frequency (MF) transformer, leading to a DC offset in the transformer's current. (Shu et al., 2019). To identify the DC offset component, the currents on both the primary and secondary sides of the transformer were measured ten times within a single switching period, and based on these measurements, the DC offset was corrected by adjusting the duty ratios of the two active bridges. This approach is effective in reducing both the dynamic and static components of the DC offset (Wang et al., 2018). For ease of implementation, the compensation for dynamic DC offset can be incorporated directly

into the modulation strategy by independently controlling the phase angle of each leg in the dual-active bridge (DAB) DC-DC converter. (Guzmán et al., 2021; Takagi & Fujita, 2018). The methods for compensating dynamic DC offset solely necessitate the use of delay elements.

The bus voltage regulation was managed via the voltage source converter (VSC). An inherent double-frequency ripple present in the bus voltage has the potential to distort the waveform of the grid current. (Karimi-Ghartemani et al., 2013). Typically, a notch filter is utilized to prevent the double-frequency ripple component from entering the bus voltage control loop. This allows for an expansion of the loop's bandwidth with decreased bus capacitance, resulting in a nearly sinusoidal grid current waveform. (Somkun et al., 2023; Taghizadeh et al., 2019). Nevertheless, the presence of low-frequency harmonic components in the grid voltage and at the VSC terminal, arising from the dead time effect, could still lead to distortion in the grid current waveform. In a recent development, have implemented a comprehensive strategy for mitigating current harmonics in grid-connected voltage source converters (VSCs). This technique ensures that the grid current remains closely sinusoidal by rapidly controlling the bus voltage and eliminating harmonic components caused by grid fluctuations and the VSC's suboptimal switching.

Single-phase voltage source converters (VSCs) have been extensively utilized in various applications such as integrating renewable energy sources into the grid (Karimi-Ghartemani et al., 2013; Li et al., 2017; Nguyen et al., 2017; Wang & Cai, 2010), battery storage systems (G. Liu et al., 2020), railway traction systems (Y. Liu et al., 2020), and as on-board battery chargers for plug-in vehicles(Nguyen et al., 2018; Taghizadeh et al., 2019). Figure 4 illustrates a common use case for the VSC, in which the DC bus voltage $v_D(t)$ is typically connected to either a DC-DC converter or a three-phase VSC. The control strategy for these VSCs often involves a cascaded layout featuring an external loop for DC bus voltage control and an internal loop for managing the grid current. The primary goals of this control approach are to minimize fluctuations in the bus voltage, ensure a swift transient response to abrupt changes in bus power, and maintain low distortion in the grid current. However, challenges such as the distorted grid reference current $i_g^*(t)$, distorted voltage $v_{pcc}(t)$ at the point of

common coupling (PCC), and the VSC terminal voltage $v_c(t)$ affected by the dead-time voltage $v_{DT}(t)$, can introduce harmonic distortions into the grid current $i_g(t)$.

The double-frequency ripple within the DC bus voltage control loop leads to distortion in the reference current intended for the grid current control loop. Traditionally, this issue of the distorted current reference is mitigated by setting the control bandwidth of the bus voltage to significantly lower than the ripple's double frequency, typically around 10 Hz (Karimi-Ghartemani et al., 2013). Therefore, to curb significant transient fluctuations in the bus voltage, large aluminum electrolytic capacitors are employed. Furthermore, active ripple cancellation circuits (Mellincovsky et al., 2018; Zhong et al., 2016) separate the pulsating power from the average power, leading to reduced bus capacitance and enhanced control loop bandwidth. Nonetheless, these methods necessitate the use of extra semiconductor switches, more passive components, and complex control strategies.

Allowing for some degree of ripple voltage can lead to a reduction in bus capacitance (Strajnikov & Kuperman, 2022). Consequently, widening the bandwidth of the bus voltage control loop contributes to diminishing transient voltage fluctuations. Additionally, distortion in the reference current is typically reduced by preventing the ripple voltage from entering the bus voltage control loop. The prevalent approach to achieve this has been the use of a notch filter, which effectively blocks the double-frequency ripple(Khajehoddin et al., 2013; Li et al., 2017; Taghizadeh et al., 2019; Vongkoon et al., 2019). Other strategies include adaptive bus voltage control (Merai et al., 2019), ripple voltage estimation (Somkun & Chunkag, 2016a; Taghizadeh et al., 2019), nonlinear observers (Vule & Kuperman, 2022), and synchronizing bus voltage sampling with the grid frequency (Eren et al., 2015). These methods facilitate the generation of a clean reference current alongside rapid DC bus voltage control.

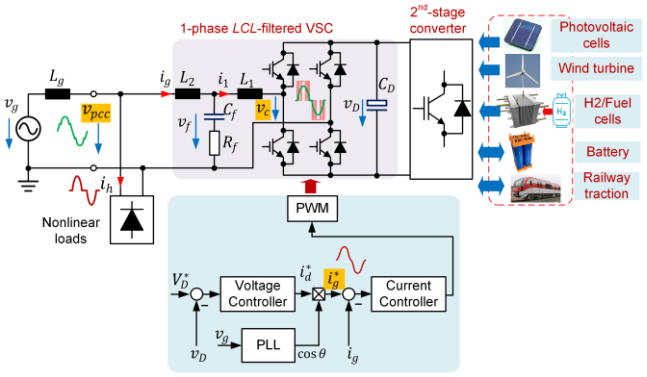


Figure 4 Single-phase LCL-filtered VSC and DAB DC-DC converter

Harmonic voltages lead to distortion in the grid current at both the point of common coupling (PCC) and the VSC terminals, attributed to a dead time, T_{DT}, present in each leg of the VSC. (Somkun, 2021; Yang et al., 2018). Incorporating feedforward of the voltage at the point of common coupling (PCC) has been partly effective in reducing the distortion of the grid current (Somkun, 2021). Nevertheless, a DC offset in the voltage measurement resulted in the undesirable injection of a DC component into the grid (Guo et al., 2021). The influence of dead time is markedly nonlinear and varies according to the current direction in the VSC. Reducing the dead-time voltage is achievable by adjusting the duty ratio, which is computed using either an adaptive algorithm (Herran et al., 2013) or an immune algorithm(Jiaxin et al., 2015). The harmonic voltages originating from the point of common coupling (PCC) and those arising due to dead time acted as disturbances within the grid current control loop. These disturbances could be alleviated by implementing a grid current controller equipped with selective harmonic mitigation techniques. Effective solutions include multi-frequency synchronous reference frame controllers (Somkun, 2021), multi-frequency proportional-resonant controllers(Elkayam & Kuperman, 2019; Kumar et al., 2022; Somkun, 2021), and repetitive controllers (RC) as demonstrated by previous studies(Yang et al., 2018).

The presence of harmonic voltages resulted in grid current distortion at both the Point of Common Coupling (PCC) and the terminals of the Voltage Source Converter (VSC) as a consequence of a dead time(T_{DT}) in each VSC leg (Somkun, 2021; Yang et al., 2018). Employing feedforward of the PCC voltage helped alleviate some of the distortion in the grid current (Somkun, 2021). Nevertheless, the presence

of a DC offset in voltage measurement led to an unwanted injection of a DC component into the grid (Guo et al., 2021). The impact of dead-time exhibited a highly nonlinear behavior, contingent upon the direction of VSC current. Mitigation of dead-time voltage could be achieved through adjustment of the compensated duty ratio, determined either via an adaptive algorithm (Herran et al., 2013) or an immune algorithm (Jiaxin et al., 2015). Both PCC and dead-time harmonic voltages represent disturbances within the grid current control loop, which can be addressed through the utilization of a grid current controller equipped with selective harmonic mitigation techniques. Effective solutions include multi-frequency synchronous reference frame controllers (Somkun, 2021), multi-frequency proportional-resonant controllers (Elkayam & Kuperman, 2019; Kumar et al., 2022; Somkun, 2021), and repetitive controllers (RC), as demonstrated in prior studies (Yang et al., 2018).

The Dual Active Bridge DC-DC converter

The DAB DC-DC converter was originally presented by De Doncker et at (De Doncker et al., 1991) as shown in Figure 1, where each bridge generates a square wave voltage to the transformer windings. The direction and magnitude of the transferred power was determined by the phase difference δ between the primary and secondary voltages (v_p and v_s) as follows (Kheraluwala et al., 1992).

$$P = \frac{N_1}{N_2}\frac{V_1 V_2}{\omega_{sw} L_{lk}}\delta\left(1 - \frac{|\delta|}{\pi}\right) \qquad (1)$$

where ω_{sw} is the switching frequency and L_{lk} is the leakage inductance of the transformer. Normally, an auxiliary inductor is added to L_{lk} to limit the delivered maximum power of the circuit. Figure 5 illustrates the primary voltage v_p , secondary voltage v_s , and the primary current i_p operating in the single phase shift (SPS) modulation (Inoue & Akagi, 2007a; Kheraluwala et al., 1992), where the current reversion occurring after/before the reversion of the voltages allows the ZVS operation in the power switches. Figure 6 shows the normalized power transfer characteristic of the single-phase DAB DC-DC converter where

$$d = \frac{N_1}{N2}\frac{V_2}{V_1} \qquad (2)$$

It is important to keep the voltage ratio between the two ports close to the transformer turn ratio $(d = 1)$ so that the converter can be operated in the ZVS conditions for higher efficiency.

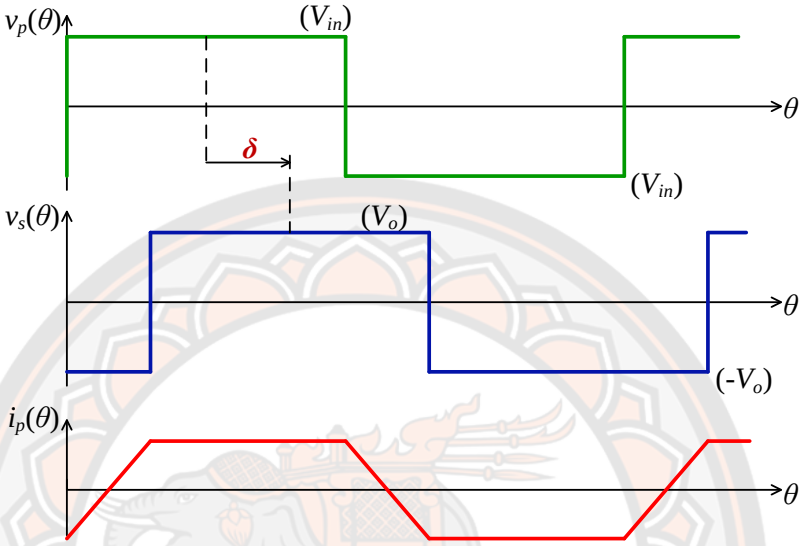


Figure 5 Key waveform of the DAB converter in the SPS modulation strategy.

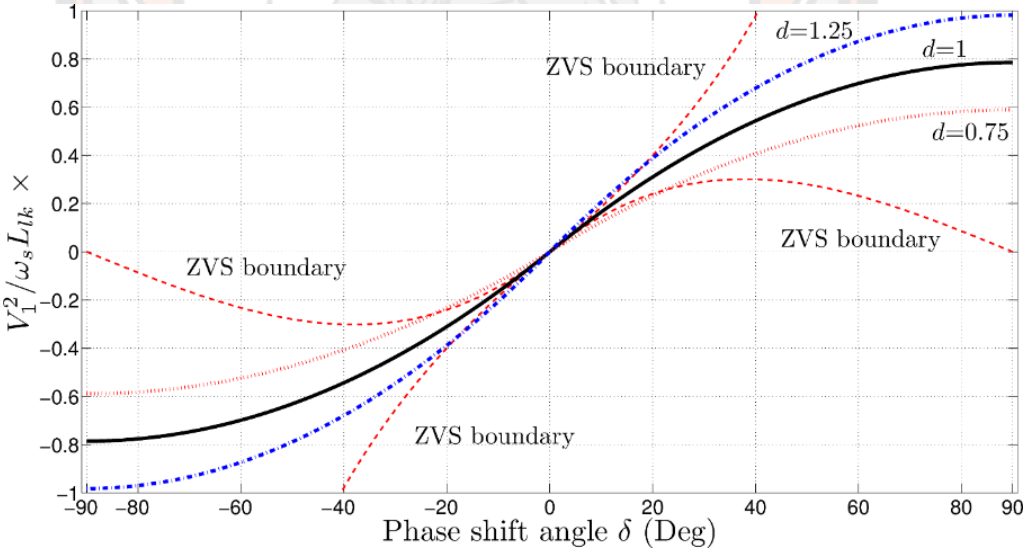


Figure 6 Transferred power characteristic and the soft switching boundary conditions of the single-phase DAB DC-DC converter with the SPS strategy.

Apart from the narrow ZVS operation range, the SPS modulation scheme also faces pure transformer utilization due to the circulating current in the auxiliary inductor. Thus, the pulse width of the primary and/or secondary voltages are adjusted

to accommodate a wider voltage regime by adding a phase shift between two phase legs of each bridge in order to increase the ZVS range and reduce the circulating current (Jain & Ayyanar, 2011). The pulse width modulation schemes of the single-phase DAB DC-DC converter can be summarized in Figure 7. The extended phase shift (EPS) method varies the pulse width only in one side of the transformer (Oggier et al., 2009), whereas the dual phase shift (DPS) and triple phase shift (TPS)(Zhao et al., 2012) schemes adjust the pulse width of both primary and secondary voltages. The difference between the DPS and TPS methods is that the TPS method varies the pulse width of the two voltage sides independently, while the pulse width of the two sides is identical for the DPS scheme. It is noted the phase angle δ is also the main variable for the power transfer. In other words, the TPS is considered as the unified representation of the phase shift control for the single-phase DAB DC-DC converter. Although the TPS method gives the best performance among these modulation strategies, but it requires three control variables. Thus, the DPS scheme is considered to be optimal for a large-scale implementation. The SPS method is simple, and it is suitable for a narrow voltage range.

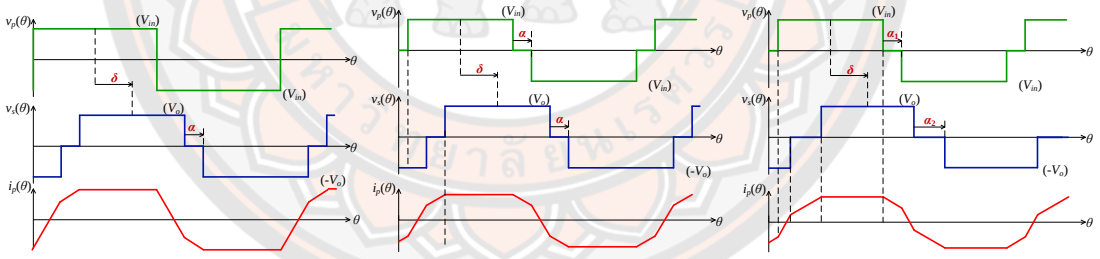


Figure 7 Pulse width modulation of the single-phase DAB DC-DC converter
(a) Extended phase shift scheme, (b) Dual phase shift scheme, (c) Triple phase shift scheme

A third wining can be added to the transformer connected to another active bridge as shown in Figure 8 (Zhao et al., 2008). This topology is suitable for connecting a renewable energy source such as fuel cells or photovoltaic modules with the main DC bus and the third port is connected to an energy storage device such a battery. The advantages of this configuration are a compact structure due to the common use of a single transformer core, galvanic isolation, ease of voltage matching via the transformer turn ratios.

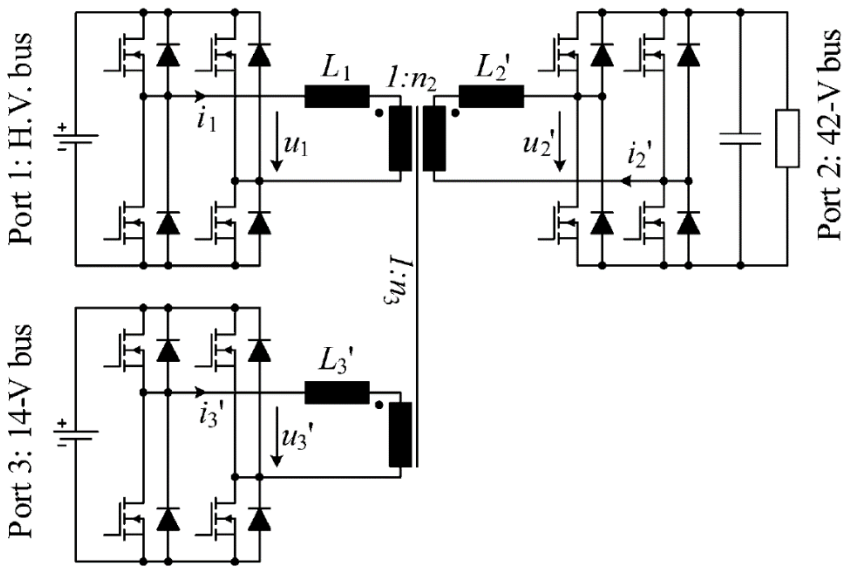


Figure 8 Triple active bridge DC-DC converter (Zhao et al., 2008)

For high power applications, the DAB DC-DC converter could be implemented in the three-phase configuration as exhibited in Figure 9 (Baars et al., 2014)[32]. Each three-phase voltage source converter operates in the six-step mode and the power transferred is determined by the phase shift in each phase similar to the single-phase DAB converter. High power capability and lower component rating are the advantages of this topology. Moreover, the ripple current in each bridge is lower resulting in smaller filter capacitors. A six-leg inverter could be used instead of the three-leg inverter as shown in Figure 10 which increases control degrees (Waltrich et al., 2016). Moreover, the switches rating are reduced by half.

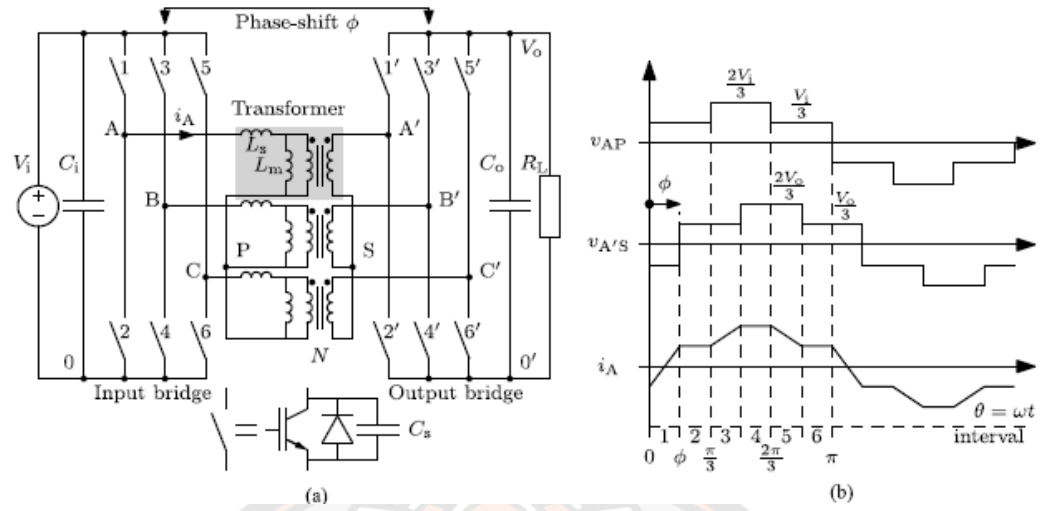


Figure 9 Three-phase DAB DC-DC converter and its ideal waveforms (Baars et al., 2014)

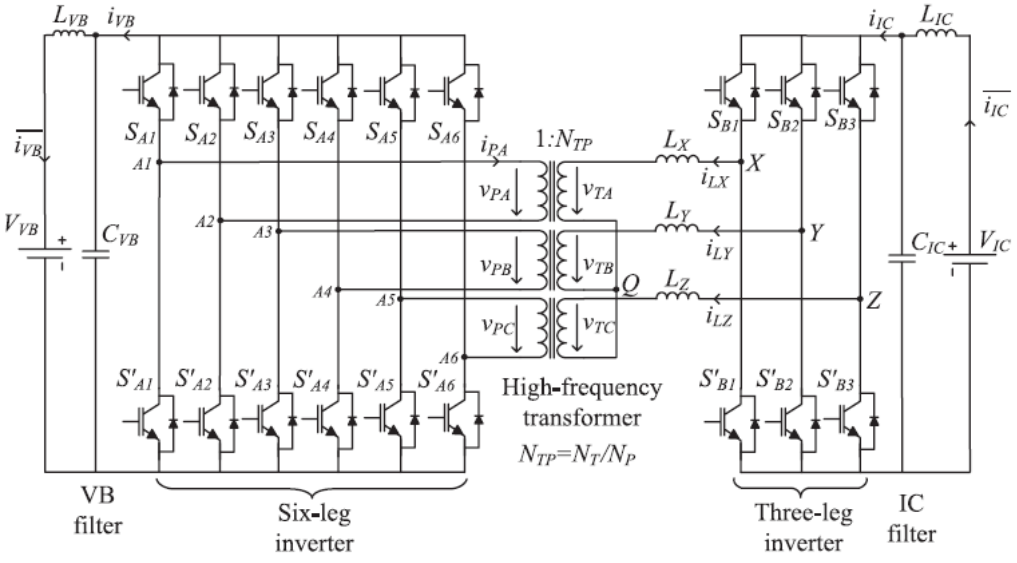


Figure 10 Six-leg three-phase DAB DC-DC converter (Waltrich et al., 2016)

High-frequency magnetic materials and their application in power electronic converters

High-frequency magnetic materials are used in the inductors of power electronic converters should exhibit low permeability so that a large amount of energy can be stored underneath the B-H curve as illustrated in Figure 11 (green curve). Moreover, the width of the B-H curve within a magnetizing period should be narrow to maintain low hysteresis loss. On the other hand, large permeability is desirable for

the high-frequency transformers so that large energy will be transferred across via the induced magnetic flux in the core (blue curve in Figure 11). For the electrical engineering point of view, large permeability results in lower magnetising current. Large saturation induction is preferred.

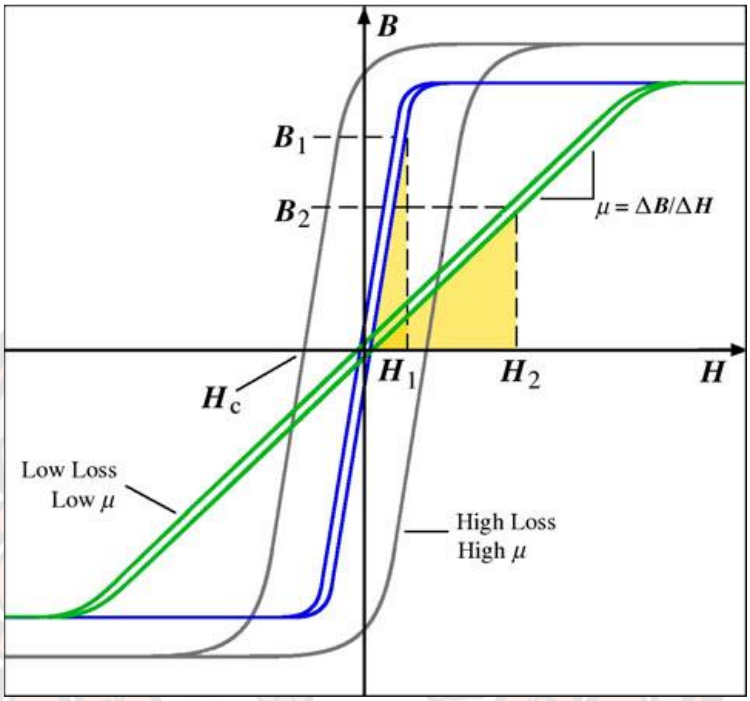


Figure 11 B-H characteristics of soft magnetic materials

Table 1 compares the typical high-frequency materials is used in power electronics converters. Ferrites are the most commonly applied materials, which are made up of iron oxide (Fe2O3) mixed with other metals such as manganese (Mn), Zinc (Zn) etc.. Ferrites in general have low Curie temperature. Thus, magnetic properties of ferrites vary with temperature significantly. For example, the saturation flux density of Epcos N87 MnZn material reduces from 0.49 T at 25°C to 0.39 T at 100°C. Ferrites have relatively high permeability. Cut cores with air gap are normally used to construct a high-frequency inductor. However, poor manufacturing techniques are greatly influence to cut core properties and can lead to higher loss (Leary et al., 2012).

Table 1 Summary of high-frequency soft magnetic materials

Materials	Ferrites	Nanocrystalline	Powdered iron
Model	Epcos N87	Vitroperm 500F	Micro-metals 75μ
Permeability, μ_i	2,200	15,000	75
$\hat{B}$, T	0.49	1.2	0.6-1.3
P_{fe}, W/cm^3	228 at 0.2T 50kHz	312 at 0.2 T 100kHz	1032 at 0.2 T 10 kHz
Curie temp., °C	210	600	665

Iron powder materials are the suitable alternatives for the high-frequency inductor cores (Mori et al., 2014; Rafiq et al., 2013). They are manufactured from an iron or an iron alloy powder, that's mixed or glued with an insulation material, then compressed, either to a ring, or a toroid shape. The distributed gap causes a low permeability, which is a function of powder size, spacing and chemical composition. Rafiq et al (Rafiq et al., 2013)compared inductors constructed from ferrite and iron powder cores of a 60-kW bidirectional DC-DC converter and found that the iron powder materials gave a lighter weight design than the ferrites with an insignificant difference in the converter efficiency.

Nanocrystalline materials contain ultra-fine iron-based alloy crystals, typically 7-20 μm in size. Their relative permeability is typically 20,000 and the saturation flux density is as high as 1.5 T. They are made into a form of thin ribbon with a thickness of 15-25 μm, which yields a low eddy current. Their advantages over the ferrites are the saturation flux density up to 1.2 T and stable magnetic properties over a wide temperature range due to the Curie temperature up to 600°C. They are suitable for high-frequency transformers up to 150 kHz. Example applications of nanocrystalline materials in the DAB DC-DC converters were illustrated in (Inoue & Akagi, 2007a; Zhao et al., 2014) Figure 12 shows a 10-kVA 20-kHz transformer made from Hitachi FINEMENT toroid (Inoue & Akagi, 2007b).

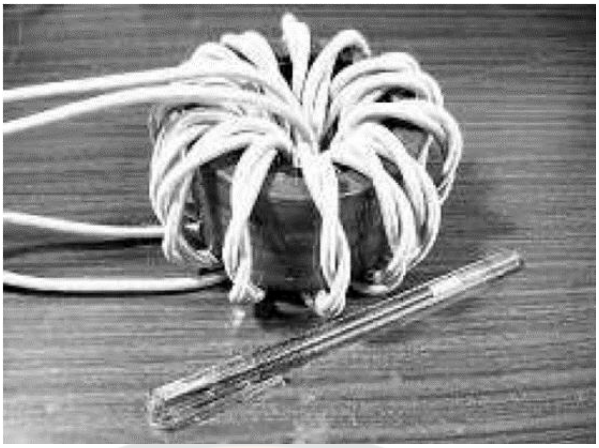


Figure 12 350-V 10-kVA and 20-kHz transformers for a DAB DC-Dc converter Using FINEMET nanocrystalline toroid from Hitachi metal (Inoue & Akagi, 2007a)

As previously noted, the control methodologies for the DAB DC-DC converter and grid-connected VSC have been extensively discussed. However, there is a lack of documentation on the microcontroller-based implementation techniques for these converters, including the generation of switching signals, interrupt requests, and analog signal sampling. Therefore, this study focuses on designing and implementing a single-phase grid-connected low-voltage battery inverter. This inverter comprises a DAB DC-DC converter and an LCL-filtered VSC, chosen for their consistent switching frequency application, which simplifies the control system's implementation. Both converters' control systems are executed in the same microcontroller within a shared interrupt service routine (ISR). The synchronous operation of generating switching signals for both the VSC and DAB DC-DC converter, as well as the analog signal sampling, is emphasized. Additionally, this research introduces a battery current control strategy, addressing dynamic DC offset mitigation of the MF transformer. The proposed inverter's experimental validation is also presented.

CHAPTER III

MITIGATION OF GRID CURRRENT DITORTION OF SINGLE-PHASE GRID-CONNECTED VOLTRAGE SOURCE CONVERTERS

Research Methodology

The flowchart illustrates the research methodology for a study focused on voltage source converters, detailing a systematic process followed by researchers from initial literature review to empirical experimentation.

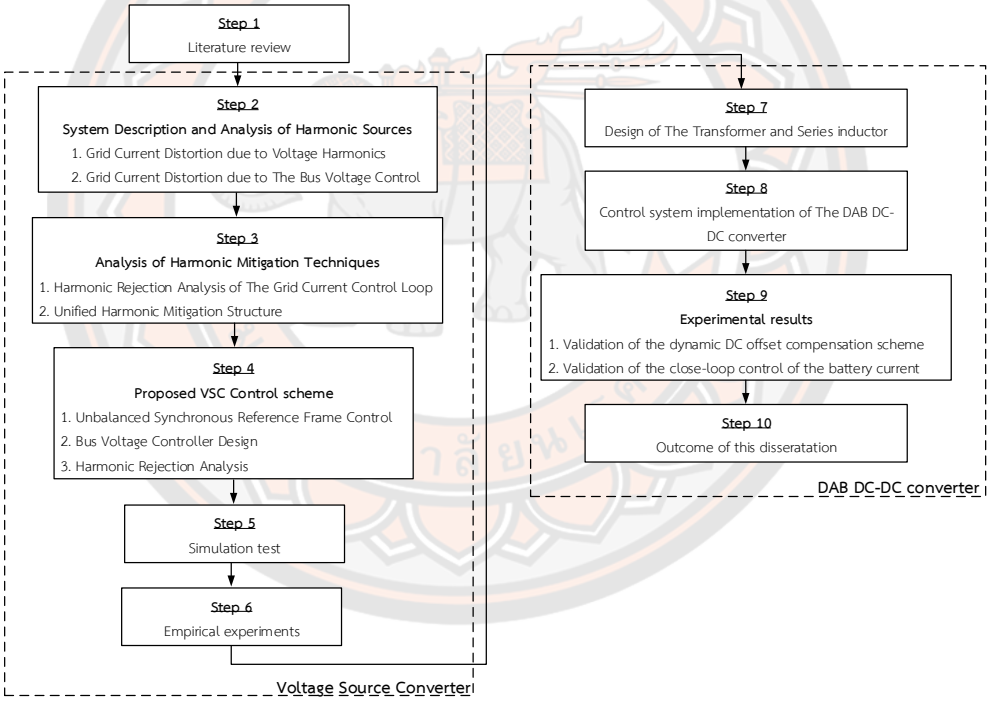


Figure 13 research methodology for a study.

Figure 13 illustrates a method flowchart that encompasses two main sections: Voltage Source Converter (VSC) and Dual Active Bridge (DAB). The steps outlined in the flowchart include conducting a comprehensive literature review to understand the current state of voltage source converters and related technologies, analyzing voltage source conversion systems to identify sources of harmonic distortion, exploring techniques to reduce harmonic distortion within the converter, developing a

new control scheme for the VSC based on the analysis, simulating and validating the proposed control scheme in a virtual environment, conducting real-world empirical experiments to further verify and refine the control scheme, and finally, focusing on improving the control of the DC-DC converter section within the dual active bridge in subsequent steps (7-9). This flowchart provides a structured approach to investigating and enhancing voltage source converters, integrating theoretical insights with practical validation to advance understanding and performance.

Grid current distortion due to voltage harmonics.

The increasing penetration of non-linear loads and power electronic-based devices in electrical networks has accentuated the issue of voltage harmonics, a deviation from the ideal sinusoidal voltage waveform that can lead to various adverse effects on the power grid, including grid current distortion. This phenomenon has become a significant concern for both of utilities and end-users, as it directly impacts the efficiency, reliability, and quality of power delivery. The interaction between voltage harmonics and the grid introduces complex challenges that necessitate a comprehensive understanding and strategic mitigation approaches to ensure the stability and efficiency of the power system.

Voltage harmonics are primarily generated by non-linear loads, such as variable-speed drives, compact fluorescent lamps, and various types of power converters, which draw current in a non-sinusoidal manner. These harmonic currents, while injected into the power system, can cause voltage distortions due to the impedance of the network. The distortion in the voltage waveform, in turn, leads to current distortion in other parts of the grid, affecting devices and systems that are sensitive to waveform quality. The consequences of grid current distortion are numerous, ranging from heightened heat generation in electrical equipment to the improper functioning of protective devices and disruptions to communication lines. These issues can ultimately lead to reduced system efficiency and higher operational expenses.

The criticality of addressing grid current distortion due to voltage harmonics is underscored by the continuous evolution of power systems towards smart grids and

the integration of renewable energy sources. As the energy landscape becomes increasingly complex, the resilience of the electrical grid to harmonic disturbances is paramount. This necessitates the adoption of innovative harmonic analysis, modeling, and mitigation techniques to preemptively address the issues posed by voltage harmonics.

This chapter aims to delve into the genesis of grid current distortion due to voltage harmonics, exploring its implications on power system operation and performance. By examining the mechanisms through which voltage harmonics induce current distortion, the paper seeks for highlight the interdependencies within the electrical grid that exacerbates this issue. Furthermore, it will review the existing strategies for harmonic mitigation and control, evaluating their effectiveness and exploring potential advancements in technology and regulation that could mitigate the impact of voltage harmonics on grid current distortion. Through this investigation, the paper endeavors to contribute to the ongoing dialogue on enhancing power quality and grid stability in the face of evolving electrical loads and generation paradigms.

In this investigation, a LCL-filtered grid-connected VSC depicted in Figure 14 and characterized by the parameters outlined in Table I is chosen. In accordance with the notation for grid current, the VSC operates in rectifier mode. The DC bus is linked to a DAB DC-DC converter serving as the second-stage converter to interface with a 400-V bidirectional DC source. This configuration finds utility in bidirectional onboard electric vehicle chargers and locomotive traction transformers. Control over the bidirectional bus power is achieved through phase shift modulation of the DAB DC-DC converter, manipulating the phase angle δ between the primary and secondary voltages of the medium frequency transformer.

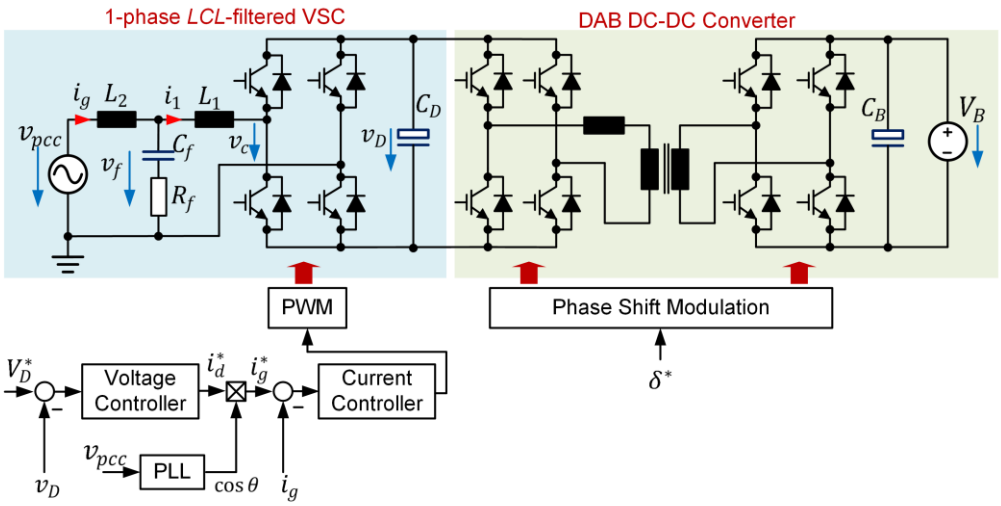


Figure 14 Single-phase LCL-filtered VSC and DAB DC-DC converter.

In Figure 15, the grid current control block diagram of the VSC in the stationary reference frame is presented. This study incorporates the distorted PCC voltage.

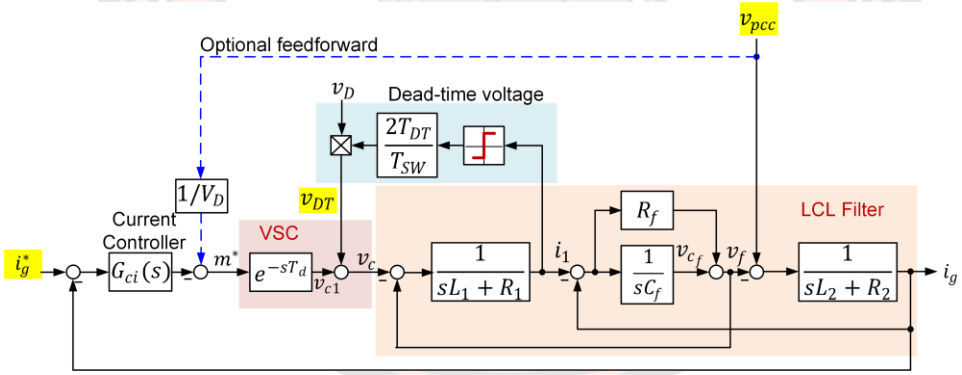


Figure 15 Single-phase LCL-filtered VSC

The distorted PCC voltage $v_{pcc}(t)$, as represented by

$$v_{pcc}(t) = \underbrace{\hat{V}_1 \cos\theta}_{v_1(t)} + \underbrace{\sum_{h=2}^{n} \hat{V}_h \cos(h\theta + \psi_h)}_{v_h(t)} \tag{3-1}$$

Here, $\theta = \omega t$, $\hat{V}_1$, and $\hat{V}_h$ represent the voltage amplitudes, and ψ_h signifies the phase angle of each harmonic component. The current controller $G_{ci}(s)$ may take the form of a proportional-resonant (PR) regulator in the stationary reference frame or a PI

regulator in the synchronous reference frame. This controller ensures an infinite gain at the grid frequency ω to attain zero steady-state error. The LCL filter governs the grid current $i_g(t)$ in the following manner.

$$L_2 \frac{di_g(t)}{dt} + R_2 i_g(t) = v_{pcc}(t) - v_f(t) \tag{3-2}$$

$$v_f(t) = v_{cf}(t) + R_f\big(i_g(t) - i_1(t)\big) \tag{3-3}$$

$$C_f \frac{dv_{cf}(t)}{dt} = i_g(t) - i_1(t) \tag{3-4}$$

$$L_1 \frac{di_1(t)}{dt} + R_1 i_1(t) = v_f(t) - \underbrace{(v_{c1}(t) + v_{DT}(t))}_{v_c(t)} \tag{3-5}$$

Disregarding the switching frequency elements, the ideal output voltage $v_{c1}(t)$ of the VSC, as stated in equation (3-5), is regulated by the modulation signal$m^*(t)$ expressed as

$$v_{c1} \approx V_D m^*(t). \tag{3-6}$$

Equations (3-2) to (3-6) demonstrate the control of the grid current $i_g(t)$ using the modulation signal $m^*(t)$ with $v_{pcc}(t)$ and $v_{DT}(t)$ act as disturbances, leading to the introduction of low-order harmonics into the grid current. The dead-time voltage $v_{DT}(t)$ in (3-5) can be approximated as

$$v_{DT}(t) \approx \frac{2T_{DT}}{T_{SW}} \text{sign}\big(i_1(t)\big) v_D(t) \tag{3-7}$$

Here, T_{SW} represents the switching period. The term $v_{DT}(t)$ can be compensated in $m^*(t)$ using (3-7). However, for the LCL filter with the grid current feedback control used in this study, an additional current sensor is required for the dead time voltage compensation. A feedforward of $v_{pcc}(t)$ helps alleviate grid current distortion to some extent (Somkun, 2021). Nevertheless, there might be a DC offset in voltage measurement, leading to the introduction of a DC component in the grid current (Guo et al., 2021).

Grid current distortion due to the bus voltage control

Figure 16 illustrates the simplified block diagram of the bus voltage control loop, where the grid current control loop is simplified to unity gain. The bus voltage $v_D(t)$ undergoes filtering through the bus voltage filter $G_{fv}(s)$ before being compared with the reference bus voltage V_D^* by the bus voltage controller $G_{cv}(s)$. The bus voltage filter may take the form of either a low-pass filter or a notch filter tuned at 2ω

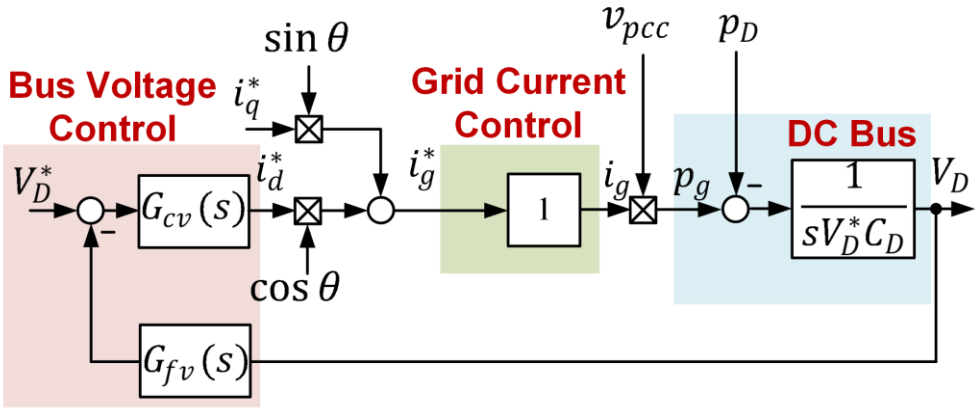


Figure 16 Equivalent bus voltage control block diagram.

Typically, a Proportional-Integral (PI) controller is used as the bus voltage controller. This controller produces the reference current i_d^* indicating the necessary active power to be drawn from or injected into the grid. Additionally, the reference current i_q^* sets the reactive power. These reference currents, i_d^* and i_q^* are multiplied by $\cos\theta$ and $\sin\theta$ templates derived from a phase-locked loop (PLL). This multiplication yields the reference signa i_g^* for the inner current control loop.

In this analysis, let's assume that the grid current$i_g(t)$ initially comprises a DC component I_{g0} and an AC fundamental component $i_{g1}(t)$ The expression for the grid current $i_g(t)$ is as follows:

$$i_g(t) = I_{g0} + \underbrace{\hat{I}_1 \cos(\theta + \phi_1)}_{i_{g1}(t)} \tag{3-8}$$

Here, $\hat{I}_1$ and ϕ_1 represent the amplitude and phase angle of $i_{g1}(t)$. The presence of asymmetry in semiconductor properties, gate driver delays, and offset in

grid current measurement contribute to the DC component current I_{g0} (Zhang et al., 2019). The grid current $i_{g1}(t)$ can be split into its components producing active and reactive power, $i_d(t)$ and $i_q(t)$, expressed as:

$$i_{g1}(t) = \underbrace{\hat{I}_1 \cos\phi_1}_{i_d} \cos\theta - \underbrace{\hat{I}_1 \sin\phi_1}_{i_q} \sin\theta. \tag{3-9}$$

Using the fundamental component of the PCC voltage, the instantaneous grid power can be expressed as follows:

$$\left.\begin{aligned} p_g(t) &= v_{pcc}(t) \cdot i_g(t) \\ p_g(t) &= \underbrace{\tfrac{\hat{V}_1}{2}\hat{I}_1 \cos\phi_1}_{P_{g1}} + \underbrace{\tfrac{\hat{V}_1}{2}\hat{I}_1 \cos(2\theta+\phi_1)}_{\tilde{p}_{g1}(t)} + \underbrace{\hat{V}_1 I_{DCg}\cos\theta}_{\tilde{p}_0} \\ p_g(t) &= \underbrace{\tfrac{\hat{V}_1}{2} i_d}_{P_{g1}} + \underbrace{\underbrace{\tfrac{\hat{V}_1}{2} i_d}_{P_{g1}} \cos 2\theta - \underbrace{\tfrac{\hat{V}_1}{2} i_q}_{Q_{g1}} \sin 2\theta}_{\tilde{p}_{g1}(t)} + \underbrace{\hat{V}_1 I_{DCg}\cos\theta}_{\tilde{p}_0} \end{aligned}\right\}. \tag{3-10}$$

The instantaneous grid power comprises the average power P_{g1} and the oscillating power components $\tilde{p}_{g1}(t)$ and $\tilde{p}_0(t)$ resulting from the AC and DC components of the grid current. Disregarding losses in the LCL filter and VSC, the power equilibrium at the DC bus can be expressed as:

$$v_D(t)\left(C_D \frac{dv_D(t)}{dt}\right) = p_g(t) - P_D(t) \tag{3-11}$$

In this equation, $P_D(t)$ represents the power output from the bus to the DAB DC-DC converter. It is assumed that $v_D(t)$ is closely controlled to remain around the reference value V_D^* (Vule & Kuperman, 2022). Consequently, the linearization of (3-11) results in:

$$V_D^*\left(C_D \frac{dv_D(t)}{dt}\right) \approx p_g(t) - P_D(t) \tag{3-12}$$

The bus voltage $v_D(t)$ comprises the average value $V_D(t)$ and the ripple component $\tilde{v}_D(t)$ expressed as:

$$v_D(t) = V_D(t) + \tilde{v}_D(t). \tag{3-13}$$

Therefore, replacing equations (3-10) and (3-13) into equation (3-12) yields the average and oscillating components as follows:

$$V_D^* C_D \frac{dV_D(t)}{dt} \cong \frac{\hat{V}_1}{2} i_d - P_D(t). \tag{3-14}$$

$$V_D^* C_D \frac{d\tilde{v}_D(t)}{dt} \cong \tilde{p}_{g1}(t) + \tilde{p}_0(t)\ . \tag{3-15}$$

It's important to note that the dynamics of the average bus voltage equation (3-14) hold true when the loop bandwidth is lower than the frequency of the oscillating components. The oscillating powers$\tilde{p}_{g1}(t)$ and $\tilde{p}_0(t)$ result in an approximation of the bus voltage ripple, given by:

$$\left.\begin{aligned}\tilde{v}_D(t) &\approx \frac{1}{V_D^* C_D}\int\left(\tilde{p}_{g1}(t)+\tilde{p}_0(t)\right)dt \\ \tilde{v}_D(t) &\approx \underbrace{\frac{\hat{V}_1\hat{I}_1}{4\omega C_D V_D^*}\sin(2\theta+\phi_1)}_{\tilde{v}_{D2\omega}} + \underbrace{\frac{\hat{V}_1 I_{DCg}}{\omega C_D V_D^*}\sin\theta}_{\tilde{v}_{D\omega}}\end{aligned}\right\}. \tag{3-17}$$

The oscillating power component $\tilde{p}_{g1}(t)$ induces the 2ω ripple component $\tilde{v}_{D2\omega}(t)$, while the ω component $\tilde{v}_{D\omega}(t)$ results from I_{g0}. Both of these ripple components traverse through the bus voltage control loop. Subsequently, the bus voltage controller $G_{cv}(s)$ generates the reference current $i_d^*(t)$ as:

$$i_d^*(t) = \hat{I}_1\cos\phi_1 + \underbrace{\hat{I}_{rp2}\cos(2\theta+\psi_2)}_{\tilde{\imath}_{d2\omega}^*(t)} + \underbrace{\hat{I}_{rp1}\cos(\theta+\psi_1)}_{\tilde{\imath}_{d\omega}^*(t)} \tag{3-18}$$

The components of ripple $\tilde{\imath}_{d\omega}^*(t)$ and $\tilde{\imath}_{d2\omega}^*(t)$ in $i_d^*(t)$ represent the residuals from the bus voltage regulator. The bus voltage control loop regulates the amplitudes $\hat{I}_{rp2}$ and $\hat{I}_{rp1}$, as well as the phase anglesψ_2 and ψ_1. The reference grid current is expressed as:

$$i_g^*(t) = i_d^*(t)\cos\theta + i_q^*(t)\sin\theta. \tag{3-19}$$

Replacing equation (3-18) into equation (3-19) yields:

$$i_g^*(t) = \underbrace{\hat{I}_1\cos\phi\cos\theta}_{Active\ power} - \underbrace{i_q^*\sin\theta}_{Reactive\ power} + \underbrace{\frac{\hat{I}_{rp2}}{2}\cos(\theta+\psi_2)}_{Additional\ reactive\ power} + \underbrace{\frac{\hat{I}_{rp2}}{2}\cos(3\theta+\psi_2)}_{i_{g3}^*(t)} + \underbrace{\hat{I}_{rp1}\cos\psi_1 + \hat{I}_{rp1}\cos(2\theta+\psi_1)}_{Caused\ by\ I_{g0}}. \tag{3-20}$$

The desired components of $i_g^*(t)$ comprise the first two terms in equation (3-20). The 2ω ripple component generates the 3rd harmonic and additional reactive power components, typically mitigated by either a low-bandwidth bus voltage control loop (Karimi-Ghartemani et al., 2013) or a notch filter. The DC component I_{g0} of the grid current introduces the DC and 2nd harmonic components in $i_g^*(t)$. This DC component I_{g0} can be minimized through precise calibration of the grid measurement.

Suppression techniques involving additional circuits enable online adjustment of the DC component (Zhang et al., 2019).

Analysis of Harmonic Mitigation Techniques

Harmonic Rejection Analysis of The Grid Current Control loop

Figure 17 illustrates the block diagram representing the grid current control in the stationary reference frame. The transfer functions of the LCL filter, denoted as $G_{LCL}(s)$ and $G_{FW}(s)$,

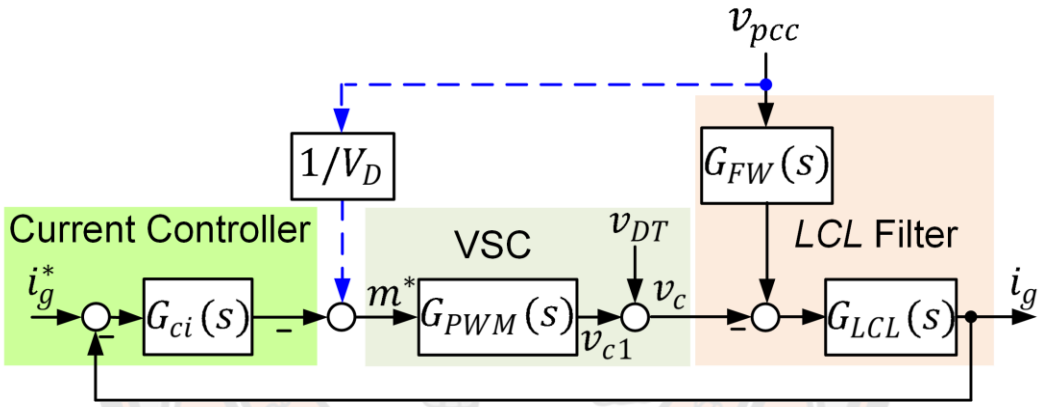


Figure 17 Block diagram depicting grid current control in the stationary reference frame.

are defined as:

$$G_{LCL}(t) = \frac{sC_fR_f+1}{C_fL_1L_2s^3+C_f(L_1+L_2)R_fs^2+C_f(L_1+L_2)s} \quad (3\text{-}21)$$

$$G_{FW}(s) = \left(\frac{L_1C_fs^2}{C_fR_fs+1}+1\right) \quad (3\text{-}22)$$

Here L_1, L_2, C_f, and R_f represent the parameters of the LCL filter. The ideal voltage $v_{c1}(t)$ of the VSC is derived through pulse width modulation (PWM) using the modulation signal m^* from the output of the current controller. The PWM process is characterized by the following transfer function model:

$$G_{PWM}(s) = \frac{v_{c1}(s)}{m^*(s)} = V_De^{-sT_d} \quad (3\text{-}23)$$

Here, $T_d = 2T_s$ represents the delay time attributed to the sampling process and transport delay (Holmes et al., 2009), where T_s denotes the sampling period. The current controller $G_{ci}(s)$ may take the form of a proportional-resonant (PR) regulator in the stationary reference frame or a proportional-integral (PI) regulator in the synchronous reference frame.

$$G_{ci}(s) = K_{p1} + \frac{K_{i1}s}{s^2+\omega^2} \tag{3-24}$$

Here K_{p1} and K_{i1} denote the controller gains. The closed-loop transfer function of the grid current control is expressed as:

$$G_{cl}(s) = \frac{i_g(s)}{i_g^*(s)} = \frac{G_{ci}(s)G_{PWM}(s)G_{LCL}(s}{1+G_{ci}(s)G_{PWM}(s)G_{LCL}(s)}. \tag{3-25}$$

The current controller $G_{ci}(s)$ in (3-24) in equation (3-24) exhibits an infinite gain at the grid frequency ω, ensuring that $|G_{cl}(j\omega)| \approx 1$. However, the controller's finite gain at frequencies 2ω and 3ω still partially follows the 2ω and 3ω components of $i_g^*(t)$ in equation (3-20). The admittances $Y_{DT}(s)$ and $Y_{pcc}(s)$ represent the influence of the dead-time and PCC voltages on the grid current, given by:

$$Y_{DT}(s) = \frac{i_g(s)}{v_{DT}(s)} = \frac{-G_{LCL}(s)}{1+G_{ci}(s)G_{PWM}(s)G_{LCL}(s)} \tag{3-26}$$

$$Y_{pcc}(s) = \frac{i_g(s)}{v_{pcc}(s)} = \frac{G_{FW}(s)G_{LCL}(s)}{1+G_{ci}(s)G_{PWM}(s)G_{LCL}(s)}. \tag{3-27}$$

Equations (3-26) and (3-27) show that $G_{ci}(s)$ in equation (3-24) can only attenuate the fundamental components of $v_{DT}(t)$ and $v_{pcc}(t)$. Optionally, incorporating a feedforward of the PCC voltage enhances dynamic performance and aids in mitigating PCC voltage harmonics (Somkun, 2021), expressed as:

$$Y_{pcc}(s) = \frac{i_g(s)}{v_{pcc}(s)} \approx \frac{(G_{FW}(s)-1)G_{LcL}(s)}{1+G_{ci}(s)G_{PWM}(s)G_{LCL}(s)} = \frac{\left(\frac{L_1C_fs^2}{C_fR_fs+1}\right)G_{LcL}(s)}{1+G_{ci}(s)G_{PWM}(s)G_{LCL}(s)} \tag{3-28}$$

Unified Harmonic Mitigation Structure

To address voltage harmonics, mitigation often involves employing a harmonic compensator (HC) $G_{cih}(s)$, the transfer function of which in the stationary reference frame is described as:

$$G_{cih}(s) = \sum_{h=3}^{n} \frac{K_{ih}s}{s^2+(h\omega)^2} \tag{3-29}$$

Here, K_{ih} represents the controller gain at the harmonic order h. The HC $G_{cih}(s)$ can be implemented using PI controllers in the multiple-synchronous reference frame, proportional-multi-resonant (PMR) regulators, or repetitive controllers, all of which exhibit sufficiently large gains at the chosen frequencies. Figure 18 depicts the typical parallel structure of the grid current control with a harmonic controller in the stationary reference frame. The outputs m_1^* and m_h^* from the fundamental and harmonic controllers combine to form the modulation signal m^*. Equations (3-30) to (3-32) in Table 2 summarize the harmonic responses of this parallel structure. Equation (3-30) illustrates that this structure follows the harmonic components of the reference current $i_g^*(t)$ at the selected frequencies due to the large gains of the HC. These large gains attenuate the harmonic components of the PCC and dead-time voltages, as shown in equations (3-31) and (3-32) (Somkun, 2021).

Table 1 Harmonic Rejection Characteristics of the Grid Current Control Structures

Transfer functions	Parallel HC structure in Fig. 6		Zero-reference HC structure in Fig. 7	
$G_{cl}(s) = \frac{i_g(s)}{i_g^*(s)}$	$\frac{\{G_{ci}(s)+G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)}{1+\{G_{ci}(s)+G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)}$	(3-30)	$\frac{G_{ci}(s)G_{PWM}(s)G_{LCL}(s)}{1+\{G_{ci}(s)+G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)}$	(3-33)
$Y_{DT}(s) = \frac{i_g(s)}{v_{DT}(s)}$	$\frac{-G_{LCL}(s)}{1+\{G_{ci}(s)+G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)}$	(3-31)	$\frac{-G_{LCL}(s)}{1+\{G_{ci}(s)+G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)}$	(3-34)
$Y_{pcc}(s) = \frac{i_g(s)}{v_{pcc}(s)}$	$\frac{G_{FW}(s)G_{LCL}(s)}{1+\{G_{ci}(s)+G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)}$	(3-32)	$\frac{G_{FW}(s)G_{LCL}(s)}{1+\{G_{ci}(s)+G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)}$	(3-35)

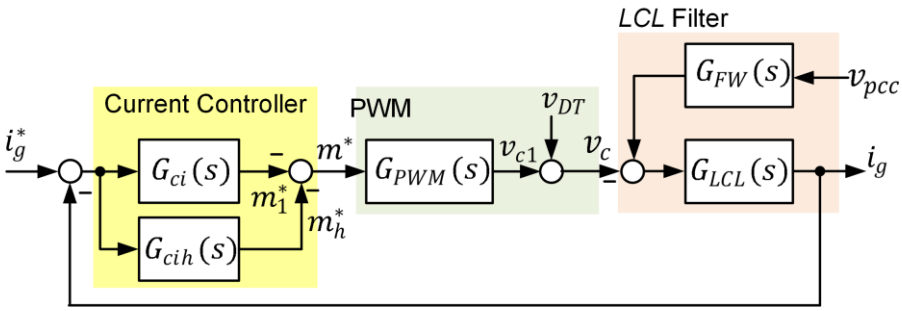


Figure 18 Grid current control with parallel HC scheme.

Figure 19(a) illustrates an alternative grid current control structure, which is equivalent to Figure 19(b) when the reference signal for the selective harmonic controller is set to zero. The transfer functions of this zero-reference HC structure are outlined in equations (3-33) to (3-35) in Table 2. The substantial gains of the HC at the selected frequencies simultaneously dampen the harmonic components in $i_g^*(t)$, $v_{DT}(t)$, and $v_{pcc}(t)$. Additionally, both the parallel and zero-reference HC schemes exhibit identical suppression characteristics of the dead-time and PCC voltages, as indicated in equations (3-31) and (3-34), as well as equations (3-32) and (3-35). Consequently, the zero-reference HC scheme enhances the bandwidth of the conventional bus voltage control, thereby improving dynamic response and reducing bus capacitance without constraining grid current distortion. In contrast, existing bus voltage control schemes have primarily focused on generating a clean reference for the grid current control loop.

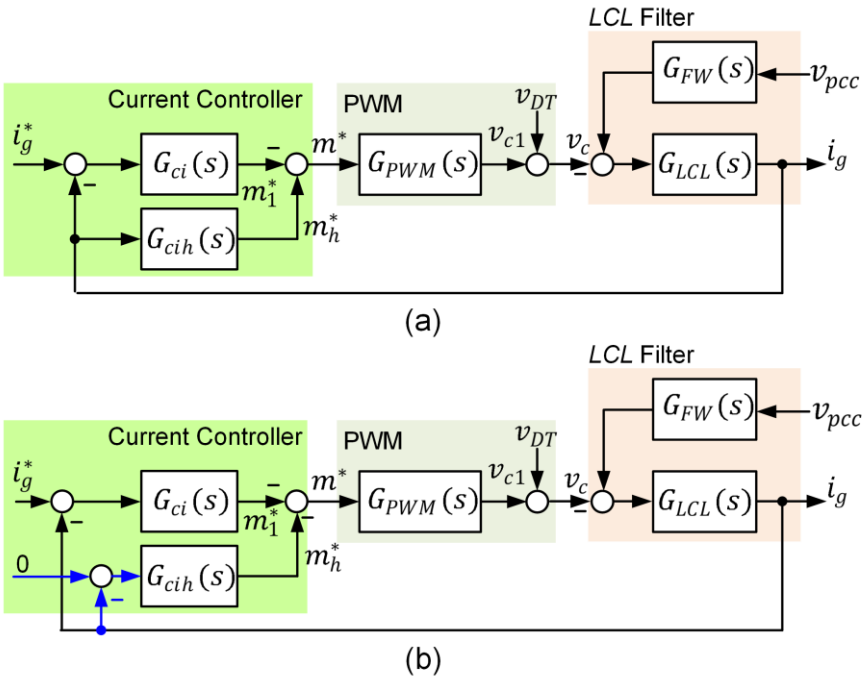


Figure 19 Grid current control proposal featuring a zero-reference HC scheme.

Proposed VSC Control scheme

Unbalanced synchronous reference frame control

The unbalanced synchronous reference frame control (Somkun & Chunkag, 2016b) is adopted for controlling both the fundamental and harmonic components of the current. Figure 20 illustrates the stationary frame representation of the transfer function $H_{DC}(s)$ implemented on the synchronous reference frame at $h\omega t$ (Monfared et al., 2014). The error signals in the stationary reference frame $e_\alpha(t)$ and $e_\beta(t)$ are derived from:

$$\begin{bmatrix} e_\alpha(t) \\ e_\beta(t) \end{bmatrix} = \begin{bmatrix} x_{\alpha ref}(t) \\ x_{\beta ref}(t) \end{bmatrix} - \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} \tag{3-36}$$

Here $x_\alpha(t)$ and $x_\beta(t)$ represent the controlled signals, while $x_{\alpha ref}(t)$ and $x_{\beta ref}(t)$ denote the reference signals in the $\alpha\beta$ −axes. The error signals $e_\alpha(t)$ and $e_\beta(t)$ are converted to the error signals $e_d(t)$ and $e_q(t)$ in the synchronous reference frame using the Park transformation:

$$e_d(t) + je_q(t) = \big(e_\alpha(t) + je_\beta(t)\big)e^{-jh\omega t}. \tag{3-37}$$

In the case of single-phase application, only the α-component output $y_\alpha(t)$ is taken into account. Utilizing the convolution and modulation properties of the Laplace transformation results in:

$$y_\alpha(s) = \frac{1}{2}\{(H_{DC}(s+jh\omega) + H_{DC}(s-jh\omega)\}e_\alpha(s) - \frac{1}{2}j\{(H_{DC}(s+jh\omega) - H_{DC}(s-jh\omega)\}e_\beta(s). \quad (3\text{-}38)$$

Therefore, by substituting $H_{DC}(s) = K_{ih}/s$ and $e_\beta(t) = 0$ into equation (3-38), the equivalent transfer function in the stationary reference frame $H_{AC}(s)$ becomes:

$$H_{AC}(s) = \frac{Y_\alpha(s)}{e_\alpha(s)} = \frac{K_{ih}s}{s^2+(h\omega)^2}. \quad (3\text{-}39)$$

This approach, known as *unbalanced synchronous reference frame control* is analogous to the resonant controller (Somkun & Chunkag, 2016b). Various control structures exist to ensure the error in the β −axis ($e_\beta(t)$) is zero, all with identical performance.

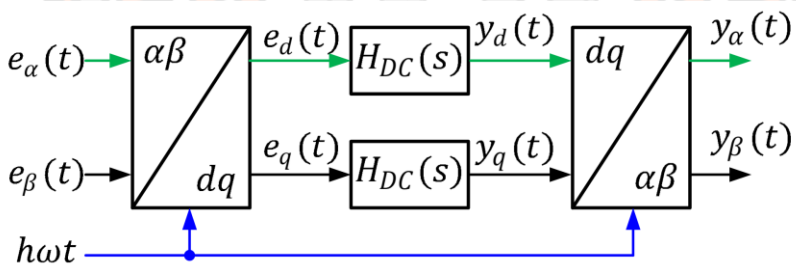


Figure 20 Stationary frame representation of the synchronous reference frame control.

Figure 21 illustrates the unified structure of the unbalanced synchronous reference control. An arbitrary signal $x_{\beta}^{*}(t)$ is employed for the Park transformations on both the reference and feedback sides, ensuring $e_{\beta}(t) = 0$. Figure 22 depicts an implementation structure of the unbalanced synchronous reference frame control using reference signals in the dq −axes, Here, the reference signal in the β −axis $x_{\beta ref}(t)$ serves as the orthogonal signal for the axis transformation of the feedback signal $x_{\alpha}(t)$.

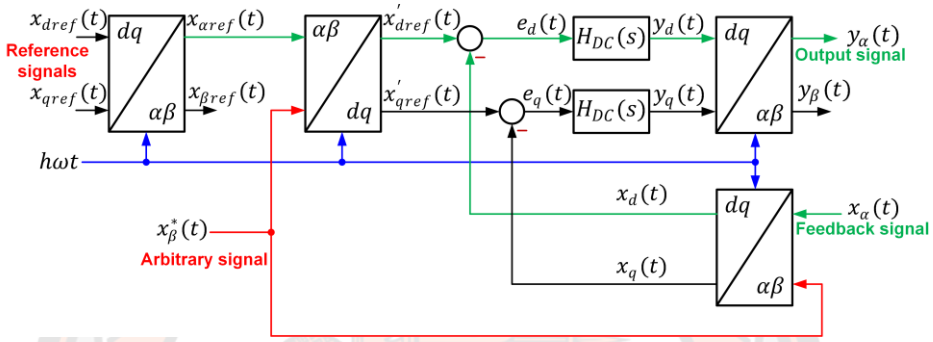


Figure 21 Unified structure of the unbalanced synchronous reference frame.

The signal $x_d(t)$ and $x_q(t)$ in Figure 22 mirror those of the conventional synchronous reference frame control in the steady state (Somkun & Chunkag, 2016b). On the other hand, Figure 11 illustrates an alternative implementation configuration of the unbalanced synchronous reference frame control with $x_{\alpha ref}(t)$ as the reference signal, ensuring $e_{\beta}(t) = 0$. This structure is suitable for an AC reference signal such as HCs. It has been demonstrated that the error signals $e_d(t)$ and $e_q(t)$ in Figure 20 are identical to those in Figures 21 and 22, resulting in similar performance (Somkun & Chunkag, 2016b).

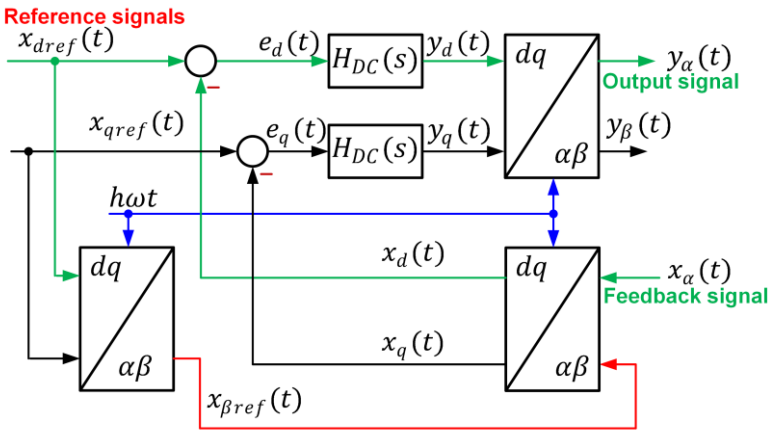


Figure 22 Unbalanced synchronous reference frame control with the references in the dq-axes.

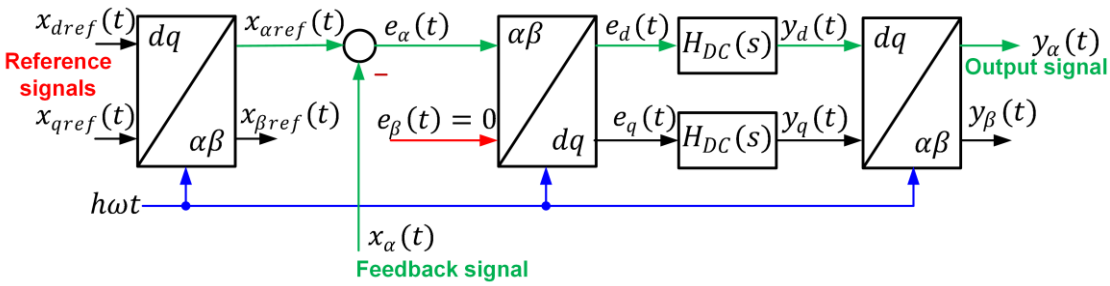


Figure 23 Unbalanced synchronous reference frame control with the reference in the α-axis.

Proposed bus voltage control scheme

Conventional methodologies for bus voltage control in single-phase VSC systems primarily aim to generate a clean reference signal for the grid current control loop (Eren et al., 2015; Khajehoddin et al., 2013; Levron et al., 2016; Pahlevani & Jain, 2015; Somkun & Chunkag, 2016a; Taghizadeh et al., 2019). However, this study introduces an alternative approach involving a conventional bus voltage control system tuned to operate at a rapid bandwidth. Nevertheless, this method results in distortion in the grid reference current $i_g^*(t)$. Therefore, instead of pursuing this approach, we utilize the current control with a zero-reference HC scheme depicted in Figure 19(a) as the primary mechanism to concurrently attenuate the harmonic

components in the grid reference current $i_g^*(t)$, PCC voltage $v_{pcc}(t)$, and VSC's dead-time voltage $v_{DT}(t)$.

Figure 24 illustrates the Proposed DC bus voltage control system with unified current harmonic mitigation, outlining the recommended method for regulating the bus voltage in the VSC. This strategy incorporates a standard proportional-integral (PI) controller within the bus voltage control circuit.

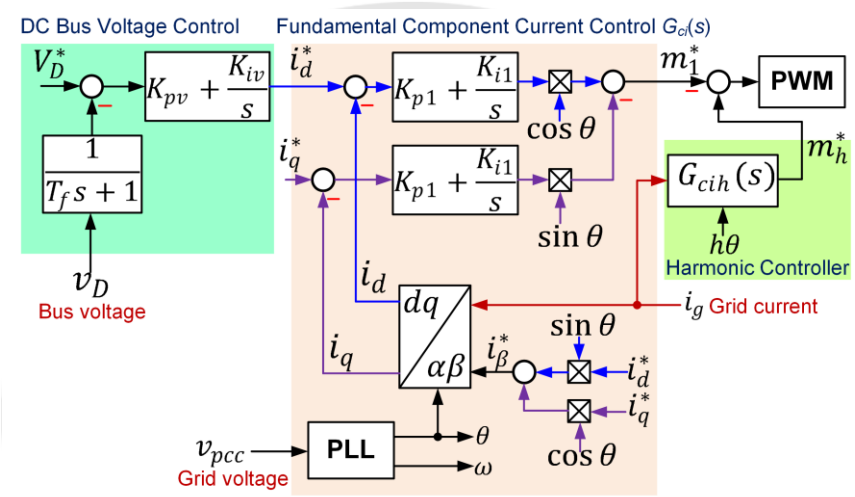


Figure 24 Proposed DC bus voltage control system.

The bus voltage undergoes processing by the low-pass filter $G_{fv}(s)$ which is described by the equation:

$$G_{fv}(s) = \frac{1}{T_f s+1}. \tag{3-40}$$

It's important to highlight that $G_{fv}(s)$ serves the purpose of loop shaping rather than reducing the ripple effect, a detail further elaborated in the controller's design segment. The primary current control system, $G_{ci}(s)$, utilizes the unbalanced synchronous reference frame, assigning the reference current on the β-axis $i_\beta^*(t)$, as the orthogonal component for the Park transformation. This method is a simplification derived from Figure 22. As a result, the virtual β-axis current error signal $e_{i\beta}(t)$ is set to zero. Following equation (3-38), the fundamental current control loop's equivalent transfer function in the stationary reference frame is found to be the same as that in

(3-24). Additionally, the control scheme based on the unbalanced synchronous reference frame inherently supports frequency adjustment and power extraction functionalities.

The harmonic current controller, $G_{cih}(s)$, is integrated into the basic current controller, $G_{ci}(s)$. creating a system that matches the structure shown in Figure 19(a).

Figure 25 depicts how of $G_{cih}(s)$, is set up, streamlining each harmonic element based on the unbalanced synchronous reference frame control illustrated in Figure 22. The functionality of each harmonic level corresponds to equation (3-29). As a result, the fundamental and harmonic current control depicted in Figure 24 aligns with the stationary reference frame current control system shown in Figure 19(a). It's important to note that this $G_{cih}(s)$ arrangement naturally adapts to frequency changes. Harmonic controllers for the 3rd, 5th, 7th, 9th, 11th, and 13th orders were utilized. Additionally, a second-order harmonic controller was introduced to mitigate the 2ω component of $i_g^*(t)$ resulting from the grid current's DC part, as indicated in equation (3-20). To lessen computational demands, it's feasible to use multiple-resonant regulators that adjust to frequency changes as the harmonic controller (Taghizadeh et al., 2019). This research employs the inverse Park transformation Phase-Locked Loop (PLL) as outlined by Golestan et al.(Golestan et al., 2013).

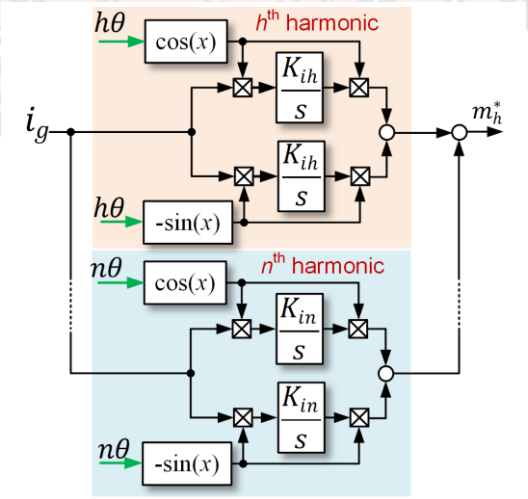


Figure 25 Harmonic controller $\boldsymbol{G_{cih}(s)}$ in the unbalanced synchronous reference frame.

The proposed control method is compared with both conventional control (Figure 26) and notch filter-based control (Figure 27), where only the primary component controller is utilized for grid current regulation. In contrast, the notch filter-based approach replaces the low-pass filter with a notch filter denoted as $G_{NF}(s)$ defined by the equation:

$$G_{NF}(s) = \frac{s^2+4\omega^2}{s^2+2\omega_d s+4\omega^2} \tag{3-41}$$

Here, ω_d represents the damping frequency. This notch filter effectively eliminates the 2ω component of the bus voltage.

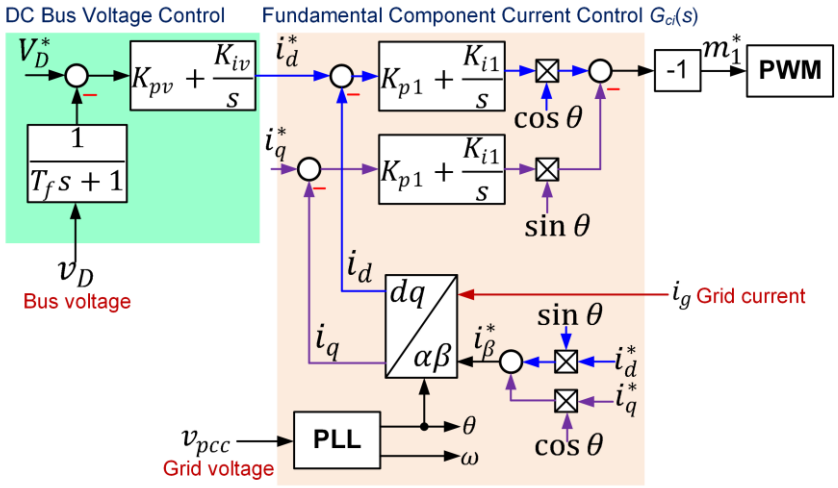


Figure 26 Traditional voltage regulation for a single-phase grid-connected VSC.

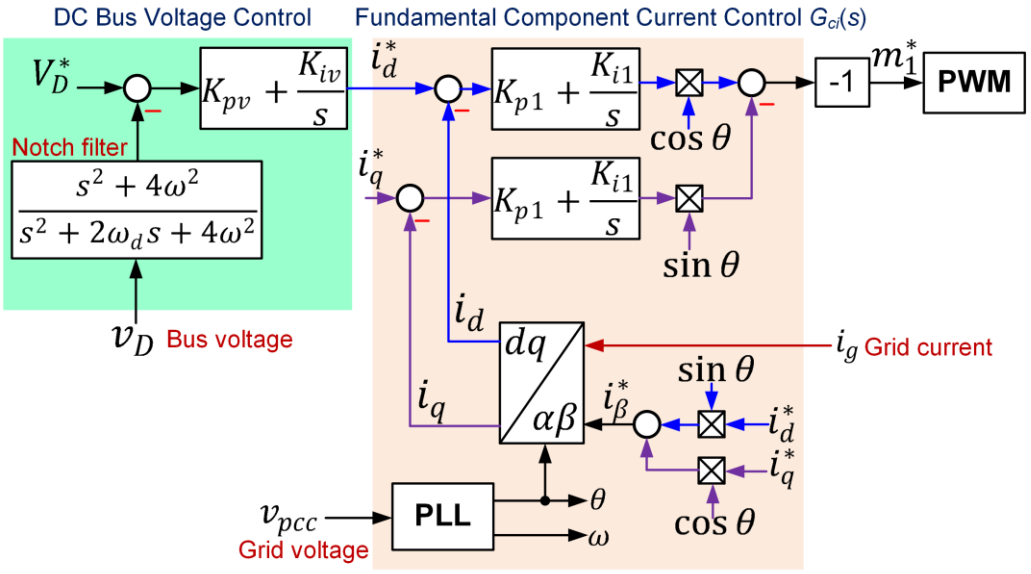


Figure 27 Notch filter-based bus voltage control of the single-phase grid-connected VSC.

Controller Design and Harmonic Rejection Analysis

Grid Current Controller Design

The *LCL* filter, with parameters detailed in Table 2, possesses a resonant frequency f_r of 5.03 kHz, while the control system operates at a sampling frequency of f_s =20 kHz. This resonant frequency f_r meets the stability criterion $f_s/6 < f_r < f_s/2$ for grid current feedback as stated by Wang et al. (Wang et al., 2016).

Table 2 Parameters of the VSC and DAB DC-DC converter

Parameters	Values
RMS line voltage	220 V
Nominal frequency	50 Hz
Nominal output DC bus voltage, V_D	400 V
Maximum apparent power	2 kVA
VSC-side and grid-side inductor, L_1 and L_2	1 mH
L_1 and L_2 winding resistance, R_1 and R_2	0.07 Ω
Filter capacitor, C_f	2.2 μF
Damping resistor, R_f	2.2 Ω
Bus capacitor, C_D	680 μF
Transformer ratio	1:1
Nominal DC output voltage, V_B	400 V
Output capacitor, C_B	1,100 μF
Switching and sampling frequencies	20 kHz

Initially, the primary component current controller is formulated within the stationary reference frame. It is imperative to select a loop bandwidth that falls below f_r. Within this frequency range, the LCL filter can be streamlined into an L filter, where $L_t = L_1 + L_2$ and $R_t = R_1 + R_2$ (Dannehl et al., 2009). The stationary reference frame equivalent of the open-loop grid current control system is articulated as:

$$G_{oi}(s) = \underbrace{K_{p1}\left(1 + \frac{K_{i1}}{K_{p1}} \cdot \frac{s}{s^2+\omega^2}\right)}_{Current\ controller} \underbrace{V_D e^{-sT_d}}_{PWM} \underbrace{\frac{1}{sL_t+R_t}}_{LCL\ filter}. \quad (3\text{-}42)$$

The highest possible crossover frequency, denoted as $\omega_{ci,max}$ is derived from the equation provided by Holmes et al (Holmes et al., 2009).

$$\omega_{ci,max} = \frac{\pi/2-\phi_{mi}}{T_d} \quad (3\text{-}43)$$

Given a selected phase margin ϕ_{mi}, the maximum crossover frequency $\omega_{ci,max}$ results in an approximation for K_{p1} as follows:

$$K_{p1} = \frac{\omega_{c,max}L_t}{V_D}. \quad (3\text{-}44)$$

The determination of K_{i1} is subsequently derived from the following equation:

$$K_{i1} = \frac{\omega_{c,max}}{10K_{p1}} \quad (3\text{-}45)$$

Where the argument of the arctangent function equals 85 degrees, implying $\tan^{-1}(\omega_{ci,max}K_{p1}/K_{i1}) = 85°$. A conservative phase margin of $\phi_{mi} = 60^{\circ}$ was chosen. Utilizing the parameters provided in Table 2 and $T_d = 2T_s$, K_{p1} and K_{i1} were computed from equations (3-44) and (3-45) with$\omega_{ci,max} = 2{,}222\pi$ rad/s. The integral gains K_{ih} of the harmonic controller should not exceed the value obtained from equation (3-45) to ensure negligible magnitude contributions at the crossover frequency (Elkayam & Kuperman, 2019). Therefore, the integral gains were set as follows:

$$\left.\begin{aligned} K_{i2} = K_{i3} = K_{i5} = K_{i7} = \frac{K_{i1}}{3} \\ K_{i9} = K_{i11} = K_{i13} = \frac{K_{i1}}{5} \end{aligned}\right\}. \quad (3\text{-}46)$$

With this array of harmonic gains, the phase margin diminishes to $\phi_{mi} = 43°$ at the designated crossover frequency ω_{ci}, yet it remains sufficiently large to ensure stability, as depicted in Figure 28. The open-loop gains at the specified frequencies are below -100 dB, effectively attenuating the current error signal at those frequencies. Despite the harmonic controller reducing the gain of the first harmonic, it remains substantial enough to accurately track the fundamental component current with zero steady-state error. The open-loop system exhibits multiple gain crossover frequencies with the harmonic controller at the designated frequencies. However, the system's stability is evaluated at the highest gain crossover frequency (Ogata, 2010). Furthermore, the two gain crossover frequencies around the resonant frequency of the *LCL* filter, with phase margins $\phi_{m1} = 43°$ and $\phi_{m2} = 189°$ as illustrated in Figure 28, ensure adherence to the stability criteria for grid current feedback.

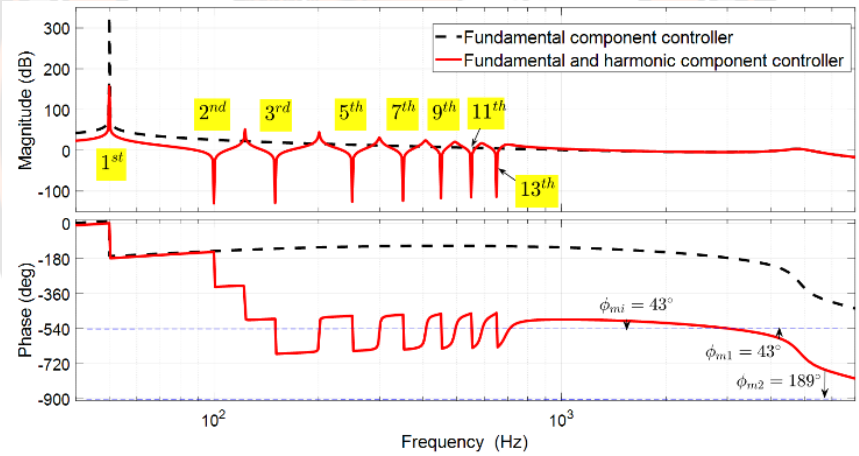


Figure 28 Open-loop frequency response of the grid current control systems

Bus Voltage controller design

Figure 29 illustrates the simplified block diagram of bus voltage control, derived from Figure 27. In this depiction, the grid current control loop is approximated as having unity gain, while the grid oscillating powers $\tilde{p}_{g1}(t)$ and $\tilde{p}_0(t)$ are treated as disturbances. The extended symmetrical optimum method (Preitl & Precup, 1999) is employed, which has been demonstrated to offer superior transient response and lower grid current distortion compared to the method described in (Karimi-Ghartemani et al., 2013; Somkun & Chunkag, 2022). With this tuning

approach, the phase angle of the forward path reaches its maximum at the crossover frequency frequency ω_{cv}. The phase margin ϕ_{mv} is determined from a constant β as:

$$\phi_{mv} = tan^{-1}\left(\frac{\beta-1}{2\beta^{1/2}}\right). \tag{3-47}$$

The suggested range for β are from 4 to 16, corresponding to ϕ_{mv} values ranging from 36° to 60°. The PI controller parameters K_{pv} and K_{iv} along with the low-pass filter time constant T_f are co-optimized based on the desired bandwidth ω_{nv} as follows:

$$\left.\begin{aligned} T_f &= \left(\sqrt{\beta}\omega_{cv}\right)^{-1} \\ K_{iv} &= \frac{\omega_{cv}^2}{\sqrt{\beta}}\left(\frac{2V_D^* C_D}{\hat{V}_1}\right) \\ K_{pv} &= \omega_{cv}\left(\frac{2V_D^* C_D}{\hat{V}_1}\right) \end{aligned}\right\}. \tag{3-48}$$

The parameters derived from equation (3-48) result in the closed-loop transfer function provided as:

$$\frac{V_D(s)}{V_D^*(s)} = \frac{\beta^{1/2}s/\omega_{cv}+1}{s^3/\omega_{cv}^3+\beta^{1/2}s^2/\omega_{cv}^2+\beta^{1/2}s/\omega_{cv}+1}. \tag{3-49}$$

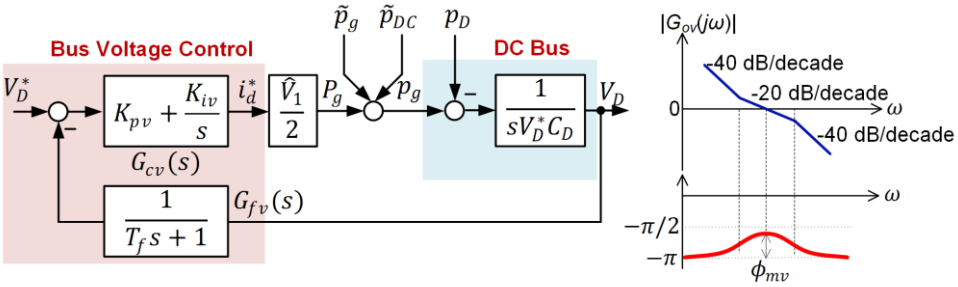


Figure 29 Equivalent bus voltage control block diagram and its open-loop frequency response.

The bus voltage control loop was engineered at $\omega_{cv} = 50\pi$ rad/s and $\beta = 5.83$ with $\phi_{mv} = 45^{\circ}$. This investigation juxtaposes the proposed control method with the conventional bus voltage control depicted in Figure 15, where two scenarios of $\omega_{cv} = 20\pi$ rad/s and $\omega_{cv} = 50\pi$ rad/s. In Figure 16, the notch filter is simplified as a low-pass filter with $T_f = \omega_d/(2\omega^2)$ facilitating the adoption of the bus voltage control design methodology. The notch filter $G_{NF}(s)$ tuned at 2ω with $\omega_d = 140\pi$ rad/s, exhibits a

frequency response below 2ω closely resembling that of a low-pass filter for $\omega_{cv} = 50\pi$ rad/s. Consequently, K_{pv} and K_{iv} for the notch filter-based control can be borrowed from the conventional control setup with $\omega_{cv} = 50\pi$ rad/s.

HARMONIC REJECTION ANALYSIS

Figure 30 depicts the closed-loop frequency response of the grid current control, where the reference current is plotted as per equation (33). In this closed-loop grid current system, there is unity gain with a zero-phase angle at the grid frequency, ensuring zero steady-state error. Simultaneously, the harmonic controller suppresses the reference current at the specified frequencies. Figure 31 showcases the frequency responses of the admittances $Y_{DT}(j\omega)$ in (3-34) and $Y_{pcc}(j\omega)$ in (3-35). The proposed grid current control strategy, supplemented by the harmonic controller $G_{cih}(s)$ effectively mitigates disturbances stemming from the dead-time voltage v_{DT} and grid voltage v_{pcc} at both the fundamental and selected harmonic frequencies. Conversely, without the harmonic controller, the harmonic components of the grid voltage may even be amplified if solely relying on the fundamental current controller.

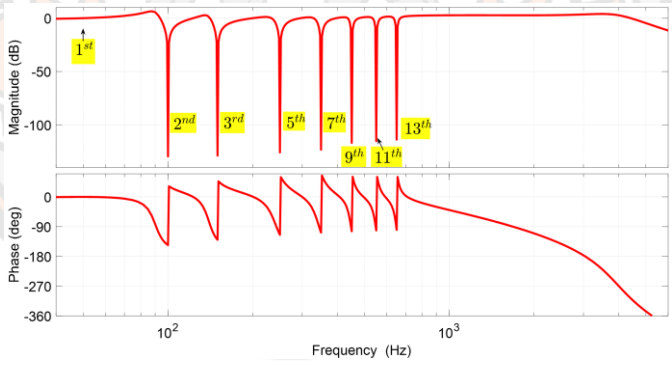


Figure 30 frequency response of the grid current to the reference current $\boldsymbol{G_{cl}(j\omega)}$

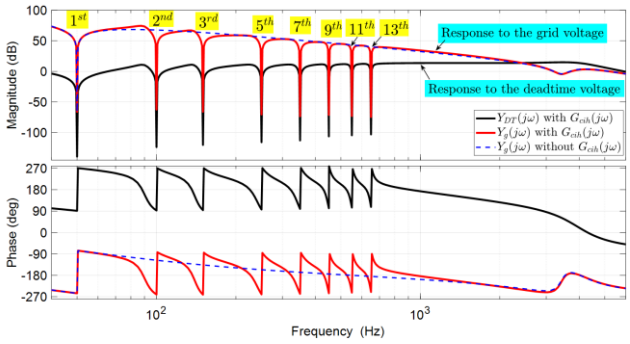


Figure 31 Frequency response of the grid current to the deadtime voltage $\boldsymbol{Y_{DT}(j\omega)}$

Simulation results

A MATLAB/Simulink model was developed to represent a switched-circuit model of the Voltage Source Converter (VSC). Voltage harmonics up to the 13rd order were introduced, with magnitudes of 5%, for the 3rd order, 2% for the 5th order and 1% for orders 7th, 9th, 11th, and 13th in relation to the fundamental component of the Point of Common Coupling (PCC) voltage. These additional harmonics led to a Total Harmonic Distortion (THD) of 5.74%. Additionally, the dead-time voltage $v_{DT}(t)$ computed using equation (3-7) with $T_{DT} = 4$ μs was incorporated into the VSC terminal voltage $v_c(t)$. was incorporated into the VSC terminal voltage 50π rad/s, with a Phase Locked Loop (PLL) bandwidth of 20π rad/s. The VSC was simulated to operate with a nominal bus power $P_D = 2$ kW and $i_q^* = 0$ to achieve unity power factor.

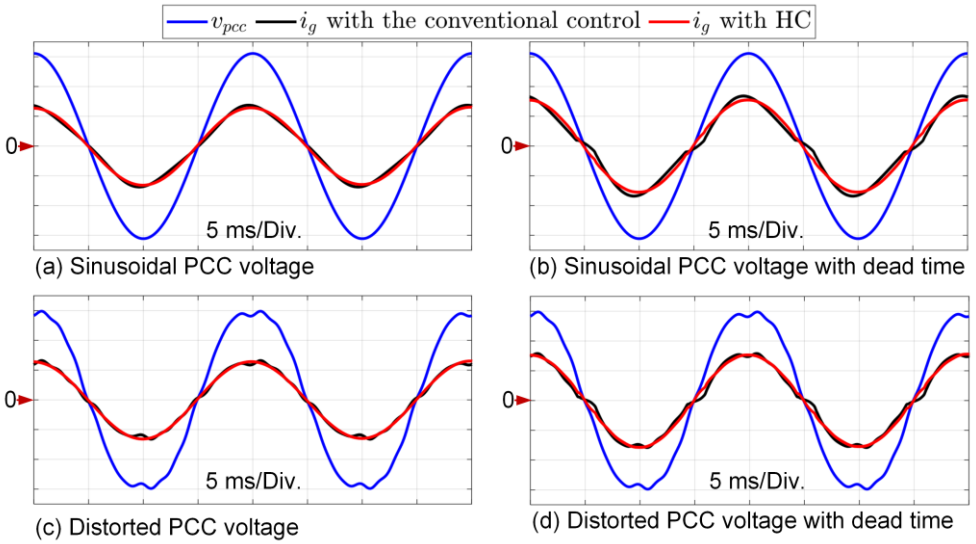


Figure 32 Simulation results of the VSC in the rectifier mode ($\mathbf{v_{pcc}(t)}$: 100 V/division, $\mathbf{i_g(t)}$: 10 A/division)

Figure 32 presents a comparative analysis of the steady-state performance between the conventional control and proposed control strategies under different scenarios: sinusoidal PCC voltage in Fig. 32(a), sinusoidal PCC voltage with the inclusion of dead-time voltage in Fig. 32(b), distorted PCC voltage in Fig. 32(c), and distorted PCC voltage along with dead-time voltages in Fig. 32(d). Under sinusoidal

PCC voltage alone, the grid current $i_g(t)$ of the conventional control scheme still exhibits distortion. Conversely, the proposed control method, aided by the Harmonic Controller (HC), effectively suppresses the harmonic components in the reference current $i_g^*(t)$, as shown in Figure 32(a). Consequently, the presence of distorted PCC and dead-time voltages significantly impacts the grid current waveform in the conventional control scheme, as depicted in Figure 32(b) to Figure 32(d). In contrast, the proposed control method with HC ensures that the grid current closely approximates a sinusoidal waveform even in the simultaneous presence of dead-time voltage and PCC harmonic voltage$v_h(t)$.

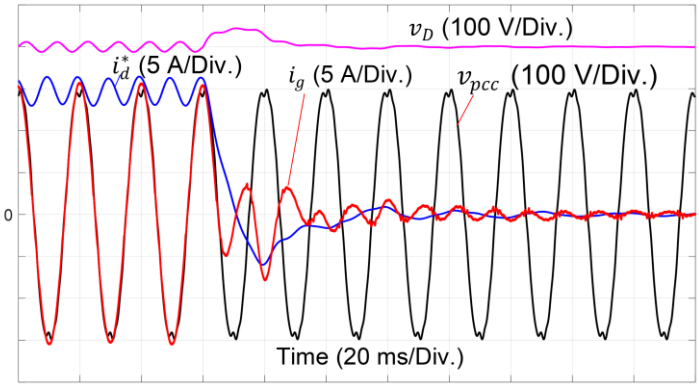


Figure 33 Simulation results of the VSC with the proposed bus voltage control in the rectifier mode when the bus power changes from 2 kW to zero under the PCC voltage distortion and dead-time voltages.

Figure 33 illustrates the transient behavior of the proposed bus voltage control system when subjected to distorted grid voltage and dead-time voltage $v_{DT}(t)$. Initially, the DC bus provides a power of $P_D = 2$ kW. Despite the presence of a 2ω ripple component in the reference current $i_d^*(t)$, maintains a sinusoidal profile similar to that observed in Figure 33. At t =0.2 s, P_D is abruptly removed, simulating a step load change. Consequently, the bus voltage $v_D(t)$ experiences an approximate increase of 50 V and swiftly recovers to its nominal value V_D^* =400 V within a duration of 50 ms.

Experimental setup

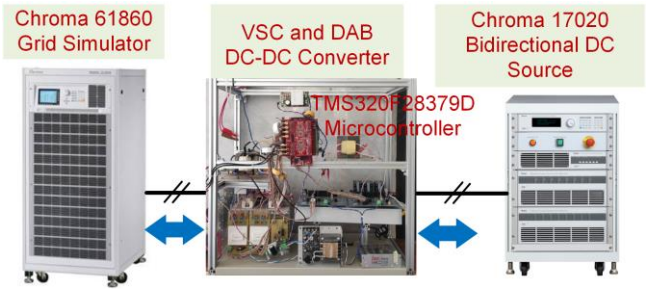


Figure 34 Experimental setup of the VSC.

Figure 34 presents the experimental setup employed in this study. The Voltage Source Converter (VSC) and Dual Active Bridge (DAB) DC-DC converter were constructed using Infineon FF50R12RT4 Insulated-Gate Bipolar Transistor (IGBT) modules, with control schemes executed on a 32-bit TMS320F28379D microcontroller. Dead times of $T_{DT} = 1$ µs and $T_{DT} = 4$ µs in each VSC leg were adjusted via the microcontroller's Pulse Width Modulation (PWM) outputs. A Chroma 61860 60-kVA grid simulator was utilized to replicate the Point of Common Coupling (PCC) voltage. The DC output voltage V_B for the DAB DC-DC converter was maintained at a constant value of 400 V using a Chroma 17020 bidirectional DC source. The output power was controlled within the range of ±2 kW through the angle δ^* of the single phase-shift modulation, also implemented on the same microcontroller. The q-axis reference current was set to $i_q^* = 0$ to achieve unity power factor.

EXPERIMENTAL RESULTS

Figure 35 illustrates the transient behavior of $v_D(t)$ and $i_g(t)$ under distorted PCC voltage and T_{DT} =1 µs when the output power transitions from 2 kW to zero. In the discrete-time control system, the reference current $i_d^*(t)$ was converted into analog form using the embedded 12-bit digital-to-analog converter of the microcontroller, with appropriate scaling. The proposed bus voltage control system compares three different control schemes: conventional control schemes tuned at $\omega_{cv} = 20\pi$ rad/s and $\omega_{cv} = 50\pi$ rad/s and the notch filter-based control system tuned at $\omega_{cv} = 50\pi$ rad/s.

In the proposed control, as well as the conventional and notch filter-based control schemes tuned at 50π-rad/s conventional and notch filter-based control schemes, have voltage fluctuations of approximately 50 V and recover to the 400-V reference within two cycles. This experimental transient response aligns with the simulation results depicted in Figure 33. However, in the case of the conventional control tuned at $\omega_{cv} = 20\pi$ rad/s, $v_D(t)$ rises to 540 V, requiring ten cycles to return to the 400 V reference. This temporarily pushes the grid current control into an unstable range. Therefore, it is suggested to increase the bus capacitance C_D for this particular conventional control scheme operating at $\omega_{cv} = 20\pi$ rad/s.

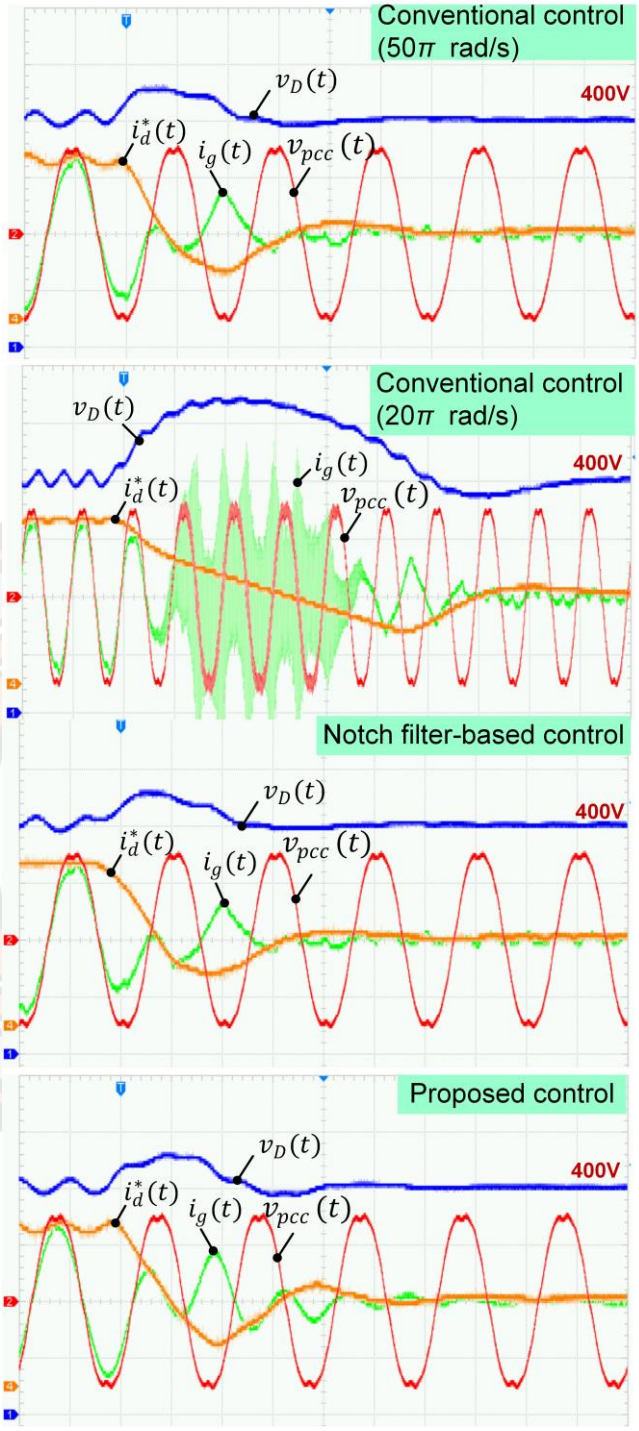


Figure 35 Transient response of the VSC when the output power changing from 2 kW to zero under the distorted PCC voltage and $\boldsymbol{T_{DT}}$ =1 μs ($\boldsymbol{v_{pcc}(t)}$ and $\boldsymbol{v_D(t)}$: 100 V/division, $\boldsymbol{i_g(t)}$ and $\boldsymbol{i_d^*(t)}$: 10 A/division).

Figure 36 depicts a comparison of the steady-state waveforms of $v_{pcc}(t)$, $v_D(t)$, $i_g(t)$ and $i_d^*(t)$ o among different control schemes when the Voltage Source Converter (VSC) operates in rectifier mode with an output power of 2 kW under sinusoidal Point of Common Coupling (PCC) voltage and T_{DT} =1 µs. Despite containing ripple components, the reference current $i_d^*(t)$ in the proposed control system results in a grid current waveform that is nearly sinusoidal. In contrast, the grid current $i_g(t)$ under the 50π-rad/s conventional control scheme exhibits slight distortion due to the ripple component of $i_d^*(t)$ when operating under sinusoidal voltage. However, both the 20π-rad/s conventional control and notch filter-based control systems under sinusoidal voltage generate a clean reference current $i_d^*(t)$, consequently yielding grid currents that are also nearly sinusoidal.

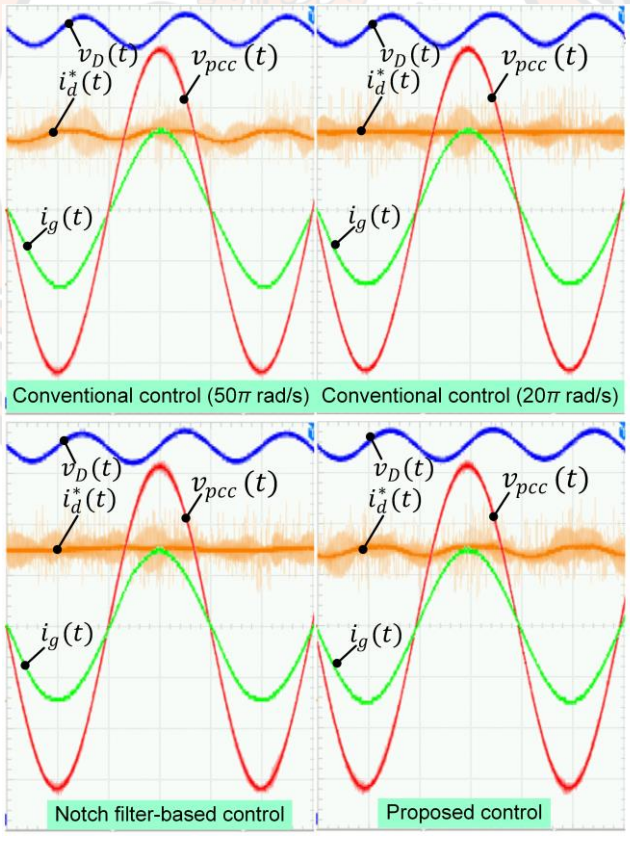


Figure 36 Steady state waveforms of the VSC with the output power of 2 kW under the sinusoidal PCC voltage and $\boldsymbol{T_{DT}}$ =1 µs, ($\boldsymbol{v_g(t)}$ and $\boldsymbol{v_D(t)}$: 100 V/division, $\boldsymbol{i_g(t)}$ and $\boldsymbol{i_d^*(t)}$: 10 A/division).

Figure 37 provides a comparison of the resulting harmonic components of the grid current under sinusoidal Point of Common Coupling (PCC) voltage with T_{DT} =1 µs and T_{DT} = 4 µs. The proposed bus voltage system effectively mitigates grid current harmonics induced by the larger dead time T_{DT} =4 µs, with a Total Harmonic Distortion of current THD$_i$ = 1.85%, compared to 1.18% for the shorter dead time T_{DT} =1 µs. The harmonic components of current under both dead-time values conform to the IEEE1547 standard. While the 20π-rad/s conventional and notch filter-based control systems regulate grid current with THD$_i$ of = 1.40% and 1.84%, respectively, for T_{DT} =1 µs, both control schemes are affected by dead-time voltage harmonics, resulting in THD$_i$ of approximately 5% for T_{DT} =4 µs. Despite having a large loop bandwidth, the 50π-rad/s conventional and notch filter-based control systems fail to attenuate the ω component in $v_D(t)$ caused by the DC component of $i_g(t)$. Consequently, the second harmonic component of the grid current is noticeable for these systems compared to the 20π-rad/s conventional system. In contrast, the proposed control scheme's Harmonic Controller $G_{cih}(s)$ effectively dampens the the 2nd harmonic current.

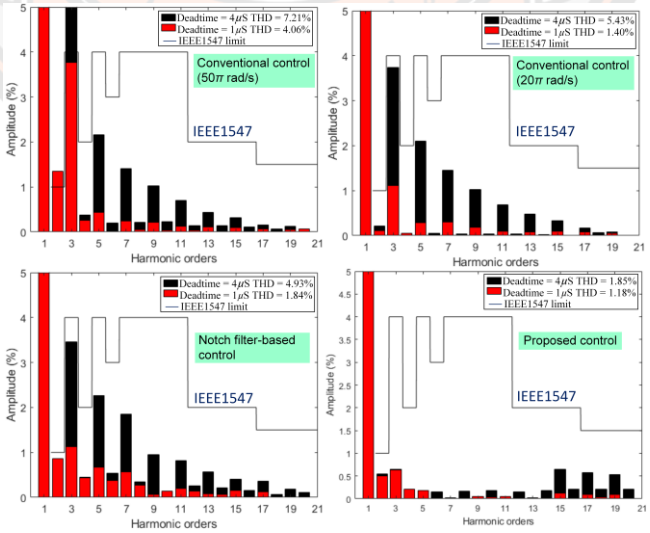


Figure 37 Harmonic components of the VSC current with the output power of 2 kW under the sinusoidal PCC voltage with $\boldsymbol{T_{DT}}$ =1 µs, and $\boldsymbol{T_{DT}}$ =4 µs.).

In Figure 38, when considering the distorted Point of Common Coupling (PCC) voltage and a substantial dead time T_{DT} =4 µs, grid current distortion is evident with both conventional and notch filter-based control schemes. The dead time primarily distorts $i_g(t)$ during zero crossings (Yang et al., 2018), while distortion stemming from PCC voltage harmonics is noticeable during peaks of the current waveform. The Harmonic Controller $G_{cih}(s)$ within the proposed control scheme effectively mitigates harmonic disturbances caused by both dead-time effects and PCC voltage.

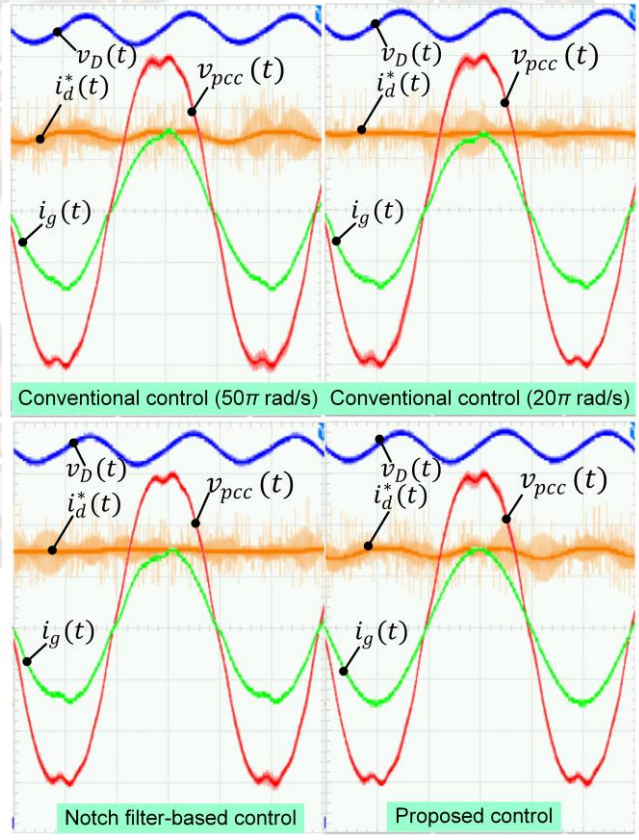


Figure 38 Steady state waveforms of the VSC with the output power of 2 kW under the sinusoidal PCC voltage and $\boldsymbol{T_{DT}}$ =1 µs, ($\boldsymbol{v_g(t)}$ and $\boldsymbol{v_D(t)}$: 100 V/division, $\boldsymbol{i_g(t)}$ and $\boldsymbol{i_d^*(t)}$: 10 A/division).

Furthermore, in Figure 39, grid current harmonics observed under distorted PCC voltage closely resemble those under sinusoidal voltage (as shown in Figure 36), affirming the efficacy of the proposed harmonic mitigation structure. Meanwhile, distorted PCC voltage adversely affects grid current waveforms under conventional and notch filter-based control schemes.

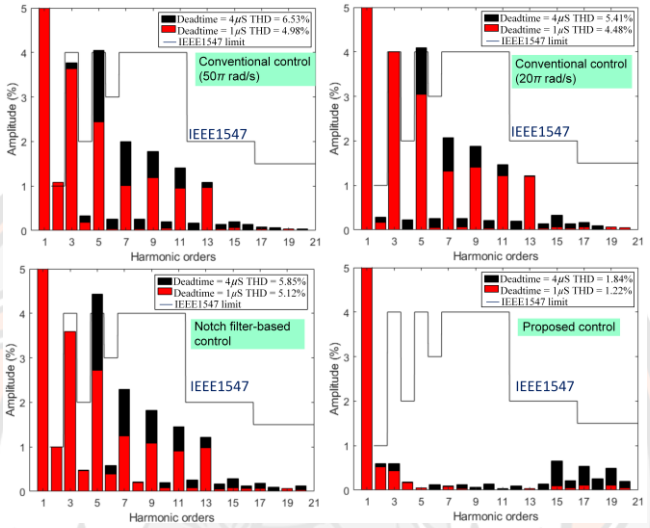


Figure 39 Harmonic components of the VSC current with the output power of 2 kW under the distorted grid voltage with $\boldsymbol{T_{DT}}$ =1 μs, and $\boldsymbol{T_{DT}}$ =4 μs

Figure 40 compares Total Harmonic Distortion of current (THD_i) values under sinusoidal and distorted PCC voltages with dead times of T_{DT} =1 μs and T_{DT} = 4 μs and an output power of ±2 kW. The proposed bus control system exhibits the lowest THD_i values, a difference particularly noticeable under PCC voltage harmonics and significant dead time. Additionally, Figure 40 compares current distortion under sinusoidal voltage and T_{DT} =1 μs with an output power of 2 kW, considering the allowable frequency range of 47-52 Hz for Thailand's grid. The proposed control system inherently adapts to frequency variations. THD_i varies with the grid frequency due to the detuned notch frequency, while the conventional control scheme with a bandwidth of 20π rad/s, significantly lower than 2ω, has minimal impact on grid frequency variation compared to the 50π-rad/s bandwidth.

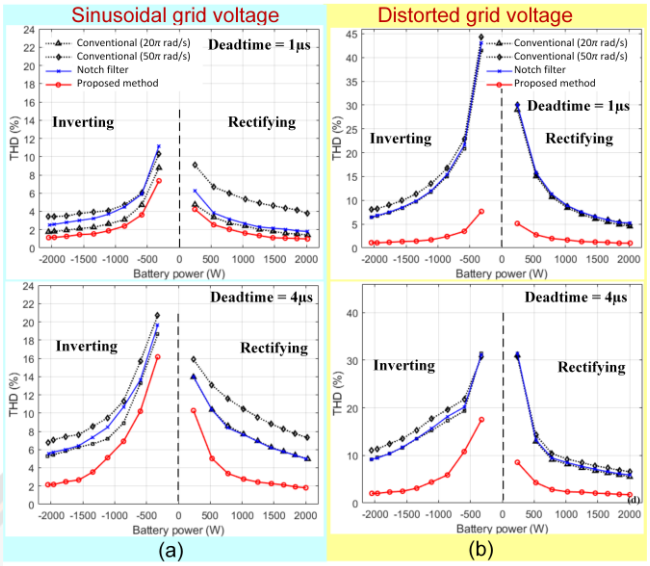


Figure 40 THDi values of the grid current with the output power under: (a) sinusoidal PCC voltage, and (b) distorted PCC voltage).

CHAPTER IV

CONTROL OF DUAL ACTIVE BRIDGE DC-DC CONVERTER

Introduction

The Dual Active Bridge (DAB) DC-DC converter marks a significant leap in power conversion technology, providing an efficient and adaptable method for transferring electrical energy between power domains with differing voltage levels. Its versatility has garnered considerable interest in applications such as renewable energy systems, electric vehicle charging stations, and grid energy storage due to its superior performance compared to conventional converters. Notably, the DAB converter's ability to manage bidirectional power flow, its compact design, and precise power transfer control make it indispensable in today's power electronics landscape.

Understanding how the DAB DC-DC converter functions is crucial not just for its technical prowess but also for its pivotal role in facilitating the integration of renewable energy sources into the power grid. By enabling efficient power conversion, the DAB converter maximizes the utilization of renewable energy, aligning with global initiatives to curb carbon emissions and promote sustainable energy solutions.

A key operational feature of the DAB converter is its capacity to modulate power transfer through phase shift control between the gate signals of the H-bridges. This simple yet effective method streamlines the converter's design while enhancing its efficiency and responsiveness to changing load or input conditions, negating the need for complex feedback control systems or additional circuitry.

At its essence, the DAB DC-DC converter operates on the principles of high-frequency transformer isolation and bidirectional power flow, ensuring safety through galvanic isolation and facilitating efficient power transfer across a wide range of voltages. The converter comprises two H-bridge inverters positioned on either side of a high-frequency transformer, with sophisticated control strategies enabling precise regulation of power flow, making it adaptable to various load conditions and input sources.

This chapter aims to elucidate the fundamental operational principles of the DAB DC-DC converter, exploring its design considerations, control strategies, and the technological innovations driving its adoption across diverse sectors. By providing a comprehensive overview of its operation, the paper underscores the converter's crucial role in modern power electronics and its contribution to advancing energy efficiency and sustainability in electrical systems.

Basic operation of the DAB DC-DC converter

Figure 42 depicts the fundamental operational waveforms of the Dual Active Bridge (DAB) DC-DC converter in the SPS modulation mode, where $\omega_{sw} = 2\pi f_{sw}$ and $\theta_{sw} = \omega_{sw} t$. In this mode, the voltage $v_P(\theta_{sw})$ of the Low Voltage (LV) bridge leads the voltag $v_s(\theta_{sw})$ of the High Voltage (HV) bridge by a phase angle δ, facilitating power transfer from the battery to the bus voltage. Conversely, power is transferred from the bus voltage to the battery with a phase angle of $-\delta$. As a result, the transferred power P_{DAB} of the DAB DC-DC converter is modulated by adjusting the angle δ through the expression:

$$P_{DAB} = \frac{V_D\left(\frac{N_s}{N_p}\right)V_B}{\omega_{sw} L_a}\delta\left(1 - \frac{|\delta|}{\pi}\right). \quad (4\text{-}1)$$

Disregarding losses in the DAB DC-DC converter, the average LV bridge input current I_{LVB} and the average battery current I_B can be obtained from P_{DAB}through the following expressions:

$$I_B = I_{LVB} = \frac{P_{DAB}}{V_B} = \left(\frac{N_s}{N_p}\right)\frac{V_D}{\omega_{sw} L_a}\delta\left(1 - \frac{|\delta|}{\pi}\right). \quad (4\text{-}2)$$

Therefore, the phase angle δ serves as the controlled variable for the battery current control loop, as depicted in Figure 41. The theoretical range of δ is $\pm\pi/2$. The DAB DC-DC converter demonstrates Zero Voltage Switching (ZVS) operation when the voltage ratio between the two DC sides closely aligns with the transformer’s turn ratio(De Doncker et al., 1991). This ZVS range widens with increasing phase shift angle (Kheraluwala et al., 1992). Conversely, the root mean square (RMS) values of the Medium Frequency (MF) transformer's currents rise as the phase shift angle increases (Somkun et al., 2021).

The flux density $B(t)$ is a crucial parameter in the design of the Medium Frequency (MF) transformer and series inductor. In accordance with the circuit configuration depicted in Figure 41, the primary winding of the transformer is directly linked to the LV bridge. Hence, the peak flux density $\hat{B}_T$ of the transformer is directly proportional to the battery voltage, represented as:

$$\hat{B}_T = \frac{1}{2N_p A_c}\int_0^{T_{sw}/2} v_p dt = \frac{V_B T_{sw}}{4N_p A_c} \tag{4-3}$$

The cross-sectional area of the transformer core, denoted by $\hat{B}_L$ of the series inductor. This peak flux density is determined by the voltage across the inductor $v_{La}(\theta_{sw})$ in Figure 22, and it is expressed as:

$$\hat{B}_L = \frac{1}{2N_L A_c}\int_0^{T_{sw}/2} v_{La} dt = \frac{T_{sw}}{4N_L A_c}\left\{\pi \frac{N_s}{N_p} V_B + (2\delta - \pi)V_D\right\} \tag{4-4}$$

The winding turn number of the inductor is denoted by N_L It's essential to ensure that the peak flux densities $\hat{B}_T$ and $\hat{B}_L$ remain below the saturation flux density $\hat{B}_{sat}$ of the core material.

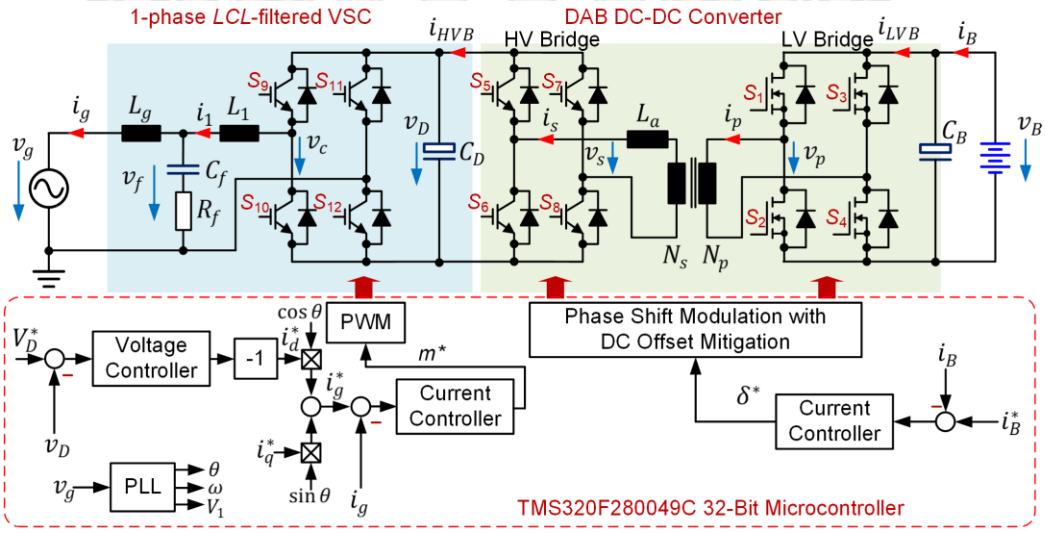


Figure 41 Diagram and simplified control system of the inverter utilized in this study.

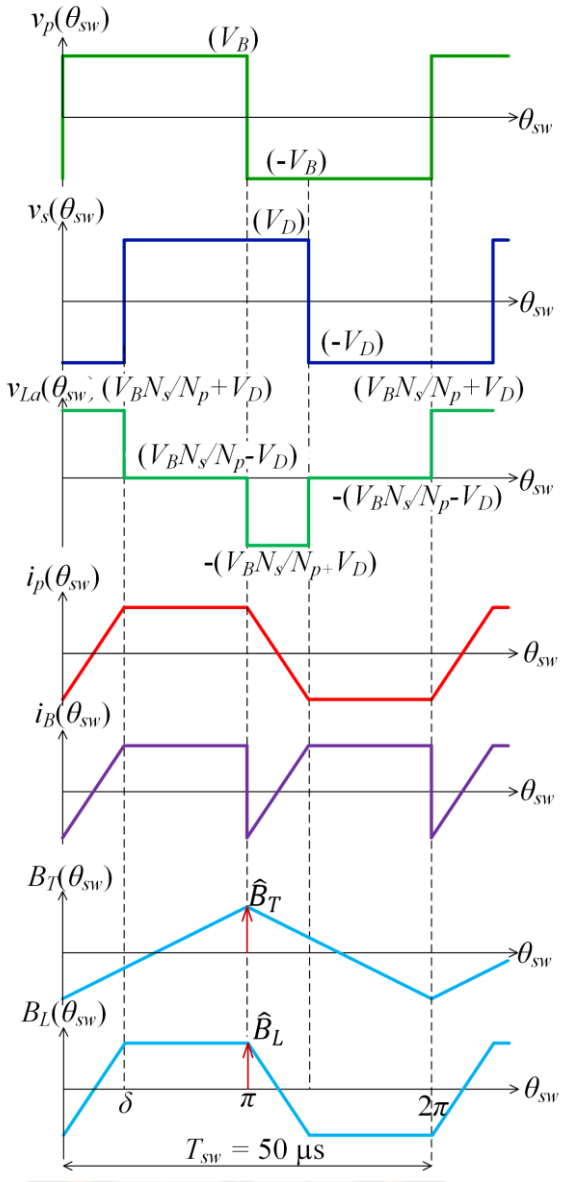


Figure 42 Voltage, current and flux density waveforms of the DAB DC-DC converter with the SPS modulation strategy (De Doncker et al., 1991).

Design of the transformer and series inductor

The control systems and switching signal generation for the VSC and the DAB DC-DC converter were executed on a TMS320F280049C 32-bit microcontroller from Texas Instruments (Dallas, TX, USA) (*TMS320F28004x Real-Time Microcontrollers-Technical Reference Manual*, 2022). The primary specifications of the battery inverter are summarized in Table 3. It's worth noting that for simplicity, the symbols

representing the winding resistance R_1, R_a and R_g of the inductors L_1, L_a and L_g are not depicted in Figure 41. Table 4 provides the parameters of the battery inverter.

Table 3 Specification of the battery inverter.

Parameters	**Value**
Maximum grid power	3 kW
Nominal grid voltage	220 Vrms
DC bus voltage	400 V
Nominal grid frequency	50 Hz
Battery nominal voltage, V_{Bn}	51.2 V
Battery voltage range	40 – 60 V
Maximum battery current	60 A

Table 4 Parameters of the battery inverter.

Parameters	**Value**
Inductor L_1	0.8 mH
Winding resistance R_1 of L_1	0.07 Ω
Inductor L_2	0.4 mH
Winding resistance R_2 of L_2	0.06 Ω
Filter capacitor C_f	2 μF
Damping resistor R_f	1.1 Ω
DC bus capacitor C_D	800 μF
Series inductor L_a	230 μH
MF transformer's turn ratio N_s/N_p	7.81
Battery-side capacitor C_B	9.9 mF
Switching frequency f_{sw}	20 kHz
Control sampling frequency f_s	20 kHz

The Medium Frequency (MF) transformer within the DAB DC-DC converter is a crucial component for power transfer and voltage conversion between the two DC sides. Meanwhile, the series inductor L_a serves to limit the maximum power transfer. For the switching frequency of 20 kHz utilized in this study, both MnZn ferrite and nanocrystalline materials are suitable. In this application, the battery voltage fluctuates with the state of charge and battery current, while the bus voltage remains constant. Therefore, to maximize the ZVS range at rated power and achieve precise battery current resolution, the maximum allowable phase shift angle is set at $\pm\pi/3$ ensuring acceptable RMS values of the transformer currents. Previous studies have shown that nanocrystalline materials exhibit superior power density and efficiency compared to MnZn ferrite material (Somkun et al., 2021). However, the magnetic properties of ribbon-wound nanocrystalline cores degrade during the cutting process (Somkun et al., 2021). Consequently, N87 MnZn ferrite cores were chosen due to their consistent magnetic properties and availability in the market (*Ferrites and accessories SIFERRIT material N87*, 2006). his core material boasts a saturation flux density of 0.39 T at 100°C and is available in various core shapes.

The generalized Steinmetz equation describes the core loss P_{fe} as a function of the core peak flux density $\hat{B}$. Meanwhile, the copper loss P_{cu} is determined by the RMS values of the transformer's currents and the winding resistance. Consequently, the resistance of the windings is derived from the core geometry, which is expressed as a function of the core peak flux density $\hat{B}$. Setting $P_{fe} = P_{cu}$ leads to the optimal peak flux density $\hat{B}_{opt}$, from which the minimum core size can be determined. An actual core size should be chosen close to the optimal one.

The MF transformer and the inductor were designed for the nominal battery voltage V_{Bn} of 51.2 V using the peak flux densities given in (4-3) and (4-4). The transformer turn ratio is selected to be close to:

$$\frac{N_s}{N_p} = \frac{V_D}{V_{Bn}} = \frac{400\ \text{V}}{51.2\ \text{V}} = 7.81. \tag{4-4}$$

The peak flux densities $\hat{B}_T$ and $\hat{B}_L$ were computed at the maximum battery voltage of 60 V to ensure they remained below the core saturation threshold. The core loss coefficient was determined from the manufacturer's specifications at a temperature of 100°C. Enameled Litz wires were utilized to mitigate the skin and

proximity effects resulting from the switching frequency. While the required value of L_a obtained from equation (4-1) was 297 μH., a slightly lower inductance of 280 μH was employed in the design to accommodate the leakage inductance of the MF transformer. Table 5 provides an overview of the key parameters of the MF transformer and series inductor. Actual core sizes were marginally larger than the required sizes, resulting in peak flux densities $\hat{B}_T$ and $\hat{B}_L$ being smaller than their optimal values. Consequently, the estimated core losses were comparatively lower than the copper losses. The anticipated core loss, as per the generalized Steinmetz equation, assumes a sinusoidal induction waveform. Additionally, N87 ferrite material exhibits higher core loss at lower temperatures. In experimental conditions, the core temperature was observed to be below 60°C, consistent with previous studies employing the same design methodology and core material (Somkun et al., 2021). Hence, actual core losses are anticipated to surpass the predicted values.

Table 5 Parameters of the MF transformer and series inductor.

Parameters	**Transformer**	**Inductor**
Material	EPCOS N87 ferrite	EPCOS N87 ferrite
Core structure	2 sets of E65/32/27	1 set of ETD49 with 2 mm gap
Total core area, A_c	10.58 cm2	2.11 cm2
Magnetic length, l_m	14.7 cm	11.4 cm
Primary winding	4 turns 4 Litz wires (500xAWG40)	55 turns 2 Litz wires (128xAWG40)
Secondary winding	31 turns 2 Litz wires (128xAWG40)	-
$\hat{B}$ at 51.2 V/60 V	0.20 T / 0.24 T	0.28 T / 0.36 T
Est. P_{cu} at 51.2V V	9.1 W	4.0 W
Est. P_{fe} at 51.2V V	8.7 W	2.2 W
Est. P_{tot} at 51.2V V	17.8 W	6.2 W

Control system implementation of the DAB DC-DC converter

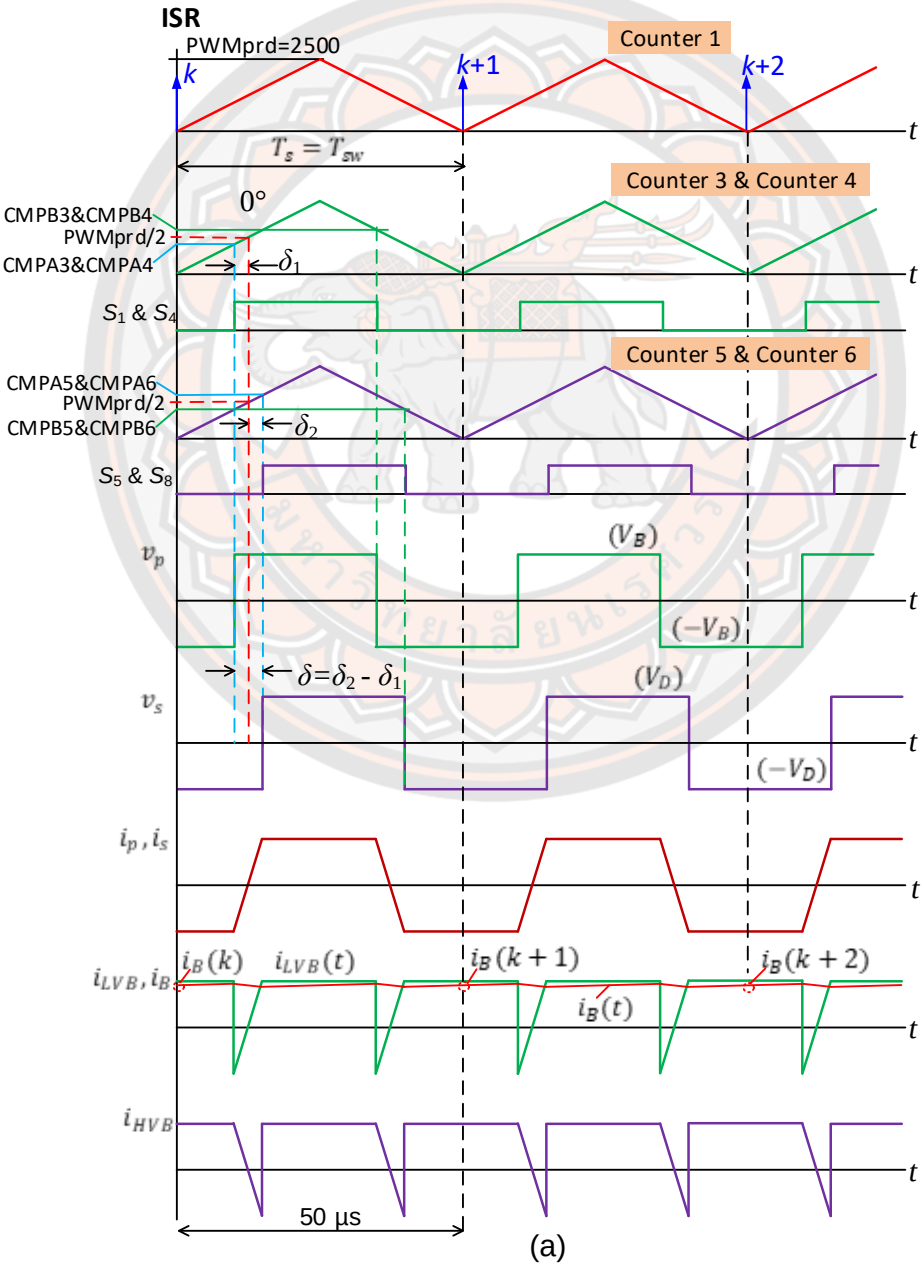
Figure 44 illustrates the steady-state timing diagram of the DAB DC-DC converter, integrated into the same Interrupt Service Routine (ISR) utilized by the VSC control scheme. Counters 3-6 are employed in the up-down mode to generate switching signals for the DAB DC-DC converter. The phase angles of counters 3-6 are synchronized with counter 1. Adjustment of the phase shift modulation is achieved by manipulating the CMPA3 to CMPA6 and CMPB3 to CMPB6 registers of counters 3-6 (Gierczynski et al., 2021). During the rising period of counters 3-6, switches S_1, S_4, S_5 and S_8 are activated when the values of the counters match their CMPA registers. Conversely, during the falling period, switches S_1, S_4, S_5 and S_8 are deactivated when the values of the counters match their CMPB registers. Consequently, this modulation strategy accommodates a maximum phase shift angle of $\pm\pi/2$. It's important to note that switches S_2, S_3, S_6 and S_7 complement switches S_1, S_4, S_5 and S_8 respectively.

The phase shift angle $\delta = 0$ is positioned at $\pi/2$ of each ISR period to sample the average value of the battery current $i_B(t)$. The reference phase angles δ_1^* and δ_4^* for switches S_1 and S_4 of the LV bridge and δ_5^* and δ_8^* for switches S_5 and S_8 of the HV bridge, are derived from:

$$\left.\begin{aligned}\delta_1^* = \delta_4^* = -\frac{\delta^*}{2}\\ \delta_5^* = \delta_8^* = \frac{\delta^*}{2}\end{aligned}\right\} \quad (4\text{-}5)$$

In the given context, δ^* represents the reference phase shift angle. Figure 30 illustrates the implementation diagram of the battery current control. The battery current is sampled at intervals of T_s. The discrete-time Proportional-Integral (PI) controller $G_{CB}(z)$ regulates the battery current $i_B(k)$ at instant k with the reference phase angle $\delta^*(k)$ as the output. The reference angles $\delta_1^*(k)$, $\delta_4(k)$, $\delta_5^*(k)$ and $\delta_8^*(k)$ are derived from equation (4-5) The reference angles $\delta_1^*(k)$ and $\delta_8^*(k)$ are translated into the values of the CMPA3, CMPB3, CMPA6, and CMPB6 registers, as illustrated in Figure 32. Meanwhile, the reference angles $\delta_4(k)$ and $\delta_5^*(k)$ are delayed by one sampling period to prevent a significant DC offset current in the transformer current $i_p(t)$ during transient (Takagi & Fujita, 2018). This approach controls the volt-

seconds applied to the transformer to maintain a small DC offset. Consequently, the values of CMPA4, CMPB4, CMPA5, and CMPB5 are determined accordingly from $\delta_4(k-1)$ and $\delta_5^*(k-1)$. The action qualifier submodule of each module defines the action of the PWMxA output when the CMPAx and CMPBx registers meet their conditions, as indicated by "set" and "clear" in the brackets. Meanwhile, the PWMxB outputs are opposite to their PWMxA outputs, with a dead time of 1.25 µs similar to the VSC (*TMS320F28004x Real-Time Microcontrollers-Technical Reference Manual*, 2022).



(a)

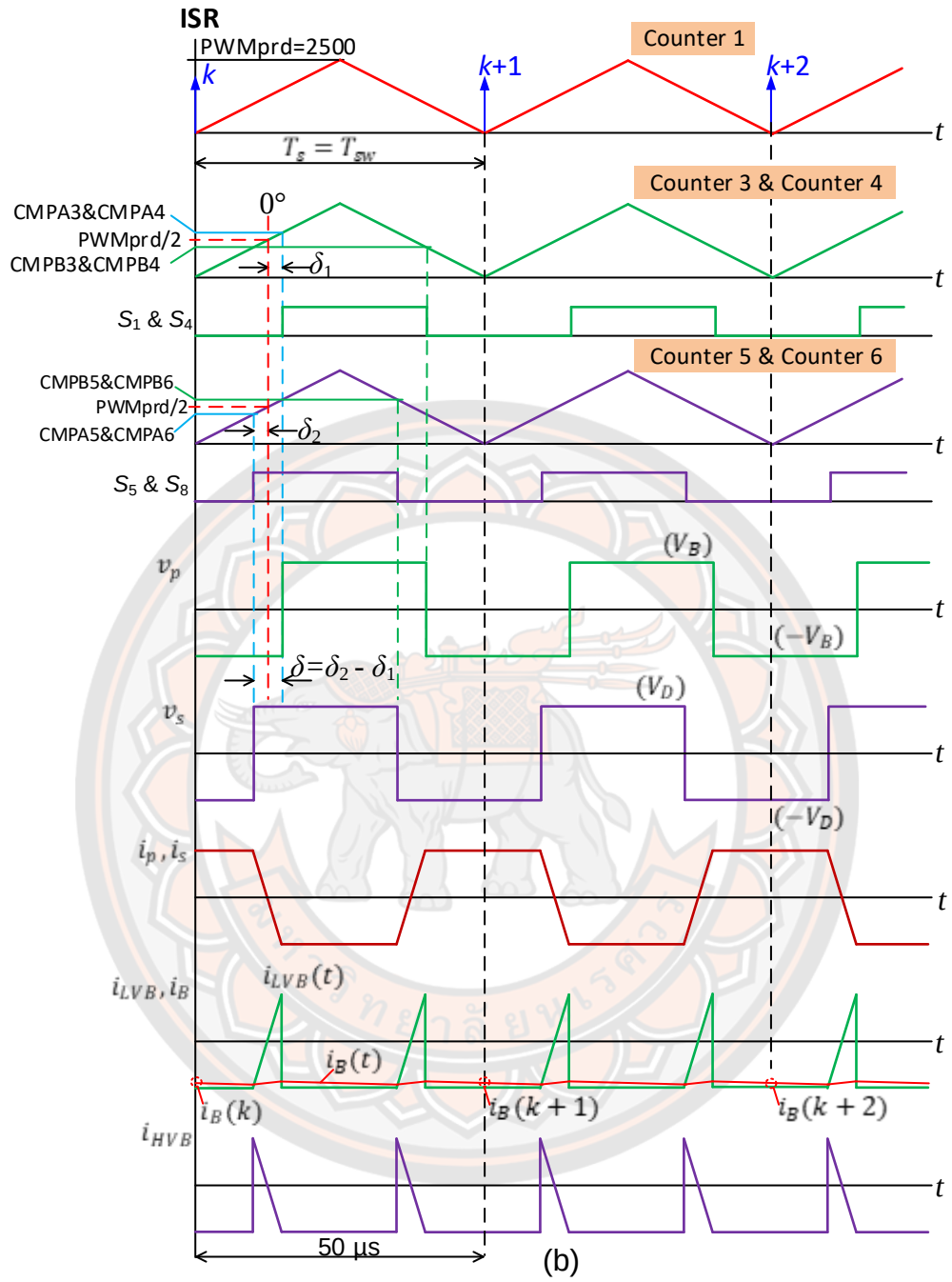


Figure 43 Steady state timing diagram for the DAB DC-DC converter: (a) For $i_B(t) \geq 0$; (b) For $i_B(t) < 0$.

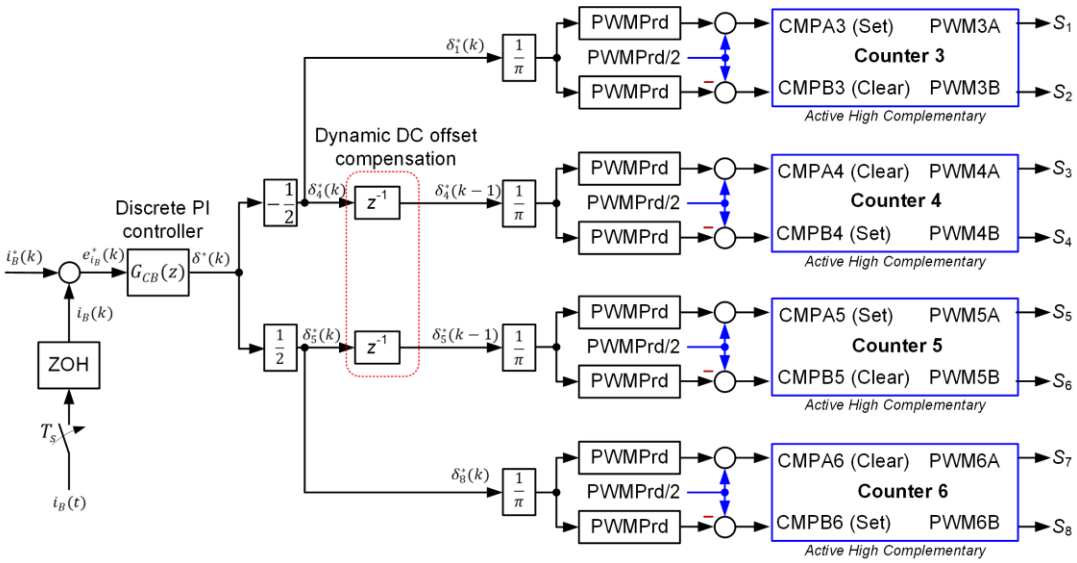


Figure 44 Implementation diagram of the battery current control loop of the DAB DC-DC converter.

Tuning of the battery current control loop

Figure 45 presents the battery side equivalent circuit, where the variables are averaged over a switching period of T_{sw}, indicated by the brackets $\langle\ \rangle$. The average current $\langle i_{LVB} \rangle$ of the DAB DC-DC converter is obtained from Equation (4-2), while the battery is represented with an open-circuit voltage $\langle e_0 \rangle$ and an internal resistance R_i. It's noted that the Thevenin-based equivalent circuit, which incorporates internal series resistance and capacitance paralleled with another resistance, is considered more accurate compared to the simplified version in Figure 45)Tomasov et al., (2019. The Thevenin-based capacitance is much larger than the battery-side capacitance C_B)Sadhukhan et al., (2022. , encompassing the voltage drops in the Thevenin-based capacitance, serves as a disturbance in the battery current control loop.

Figure 34 illustrates the equivalent block diagram of the battery current in the continuous-time domain, wherein a Proportional-Integral (PI) regulator with the constants K_{pb} and K_{ib} governs the battery current. A delay of $T_d = 2T_s$ accounts for the sampling and transport delays, as depicted in Figure 42. The gain K_{DAB} determined from the potential maximum value derived from Equation (4-2), as expressed by:

$$K_{DAB} = \frac{\langle i_{LVB} \rangle}{\delta} = \left(\frac{N_s}{N_p}\right)\frac{V_D}{\omega_{sw} L_a} \quad . \tag{4-6}$$

As per Equation (4-2), the gain (4-2), this gain K_{DAB} diminishes as the angle δ increases, leading to a higher battery current. Nevertheless, the approximated value of K_{DAB} at its peak ensures the preservation of loop stability even at elevated currents.

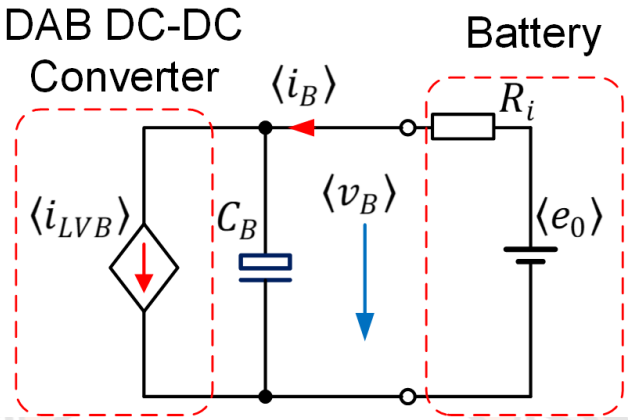


Figure 45 Equivalent circuit on the battery side.

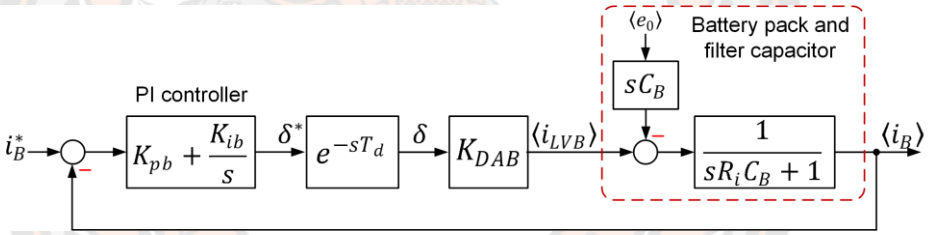


Figure 46 Block diagram of the control of battery current.

The mathematical representation of the open-loop transfer function for the battery current control loop is given by:

$$G_{bol}(s) = \left(K_{pb} + \frac{K_{ib}}{s}\right)\frac{K_{DAB}}{sR_iC_B+1} \tag{4-7}$$

Considering that the delay T_d is typically significantly smaller than the time constant R_iC_B. it is disregarded. The closed-loop transfer function is thus expressed as:

$$G_{bcl}(s) = \frac{\left(\frac{K_{DAB}}{R_iC_B}\right)s+\left(\frac{K_iK_{DAB}}{R_iC_B}\right)}{s^2+\left(\frac{1+K_{pb}K_{DAB}}{R_iC_B}\right)s+\left(\frac{K_iK_{DAB}}{R_iC_B}\right)}. \tag{4-8}$$

Compared to the standard second-order system (Åström & Hägglund, 1995), K_{pb} and K_{ib} can be written as

$$\left.\begin{aligned} K_{ib} &= \omega_0^2 \frac{R_i C_B}{K_{DAB}} \\ K_{pb} &= \frac{2\xi\omega_0 R_i C_B - 1}{K_{DAB}} \end{aligned}\right\} \quad (4\text{-}9)$$

In this equation, ω_0 represents the natural frequency, while ξ enotes the damping factor of the closed-loop system. If R_i is not known, a trial-and-error tuning approach can be utilized by adjusting K_{ib} to target ω_0^2 and K_{pb} to adjust ξ.

Experimental Validation

Figure 47 illustrates the experimental setup employed in the study. A TMS320F280049C microcontroller governed the operations of both the VSC and DAB DC-DC converter, utilizing the parameters detailed in Table 3. A switching dead time of 1.25 μs was implemented in each leg of both the VSC and DAB DC-DC converter. Power to the DAB DC-DC converter was supplied by a 16-cell 100-Ah LFP battery pack, while the VSC was linked to a Chroma 61860 grid simulator. The tuning procedure for the VSC followed the methodology outlined in prior research involving a bus voltage bandwidth of 30π rad/s and the use of current harmonic controllers targeting orders 3rd, 5th, 7th, and 9th to mitigate grid current waveform distortions. The bus voltage was maintained at a regulated level of 400 V. Adjustment of the battery current response was carried out through a trial-and-error approach, guided by the principles outlined in equation (4-9). It's worth noting that the battery management system imposed a maximum current limitation of 30 A, which consequently constrained the maximum system power within the range of ±1.5 kW or 50% of the rated power.

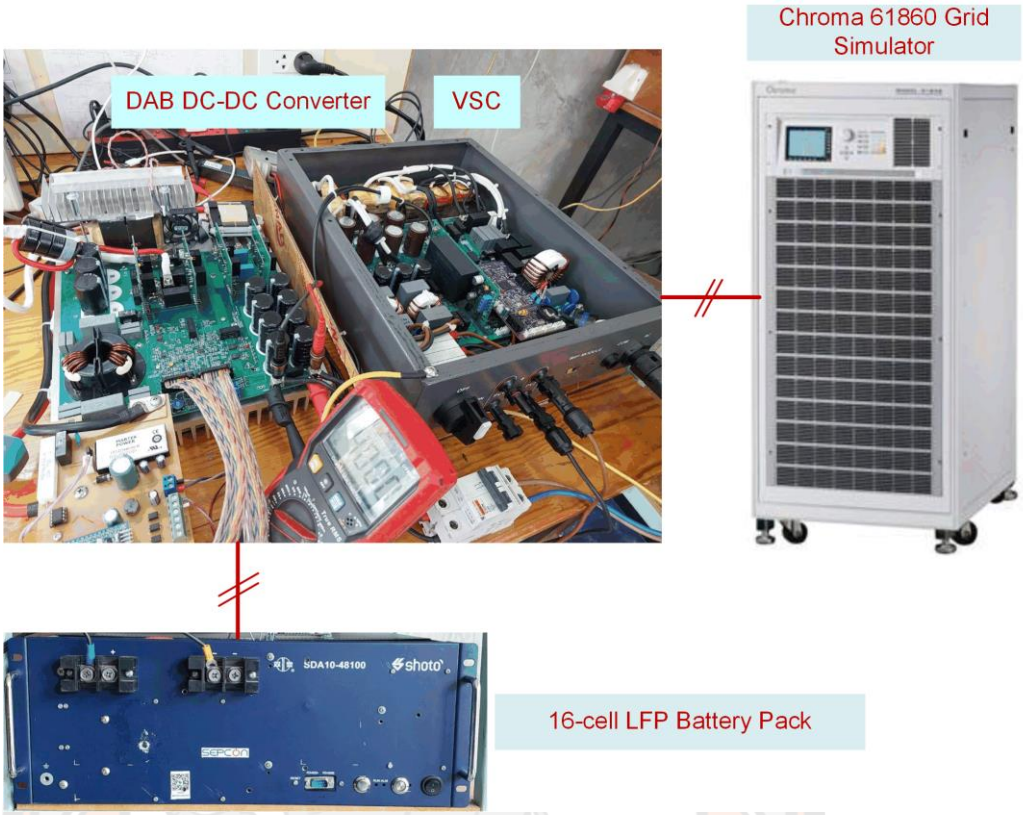


Figure 47 Experimental setup.

Experimental results

Validation of the dynamic DC offset compensation scheme

The grid simulator provided power to the VSC, maintaining the bus voltage at a regulated level of 400 V. Meanwhile, the DAB DC-DC converter operated using the reference phase angle δ^* in its open-loop control. Figure 48 illustrates the transient response of both primary and secondary voltages $v_p(t)$ and $v_s(t)$, the primary current of the transformer $i_p(t)$, and the inverted battery current $-i_B(t)$ in response to a step change in the reference angle δ^* from zero to π/4. Conversely, Figure 49 displays the same waveforms for the reference angle δ^* changing from zero to -π/4. Notably, in the absence of the dynamic DC offset compensation mechanism depicted in Figure 31, $i_p(t)$ exhibits a significant DC offset of around 30 A. Such a large current could potentially saturate the transformer core and even lead to damage to the switching devices. However, the DC offset compensation technique illustrated in Figure 46

proves effective, as the dynamic DC component of $i_p(t)$ noticeably diminishes during changes in the reference angle δ^*. Importantly, this compensation scheme has no impact on the steady waveform of $i_p(t)$, aligns with the behavior predicted by the equivalent circuit shown in Figure 50.

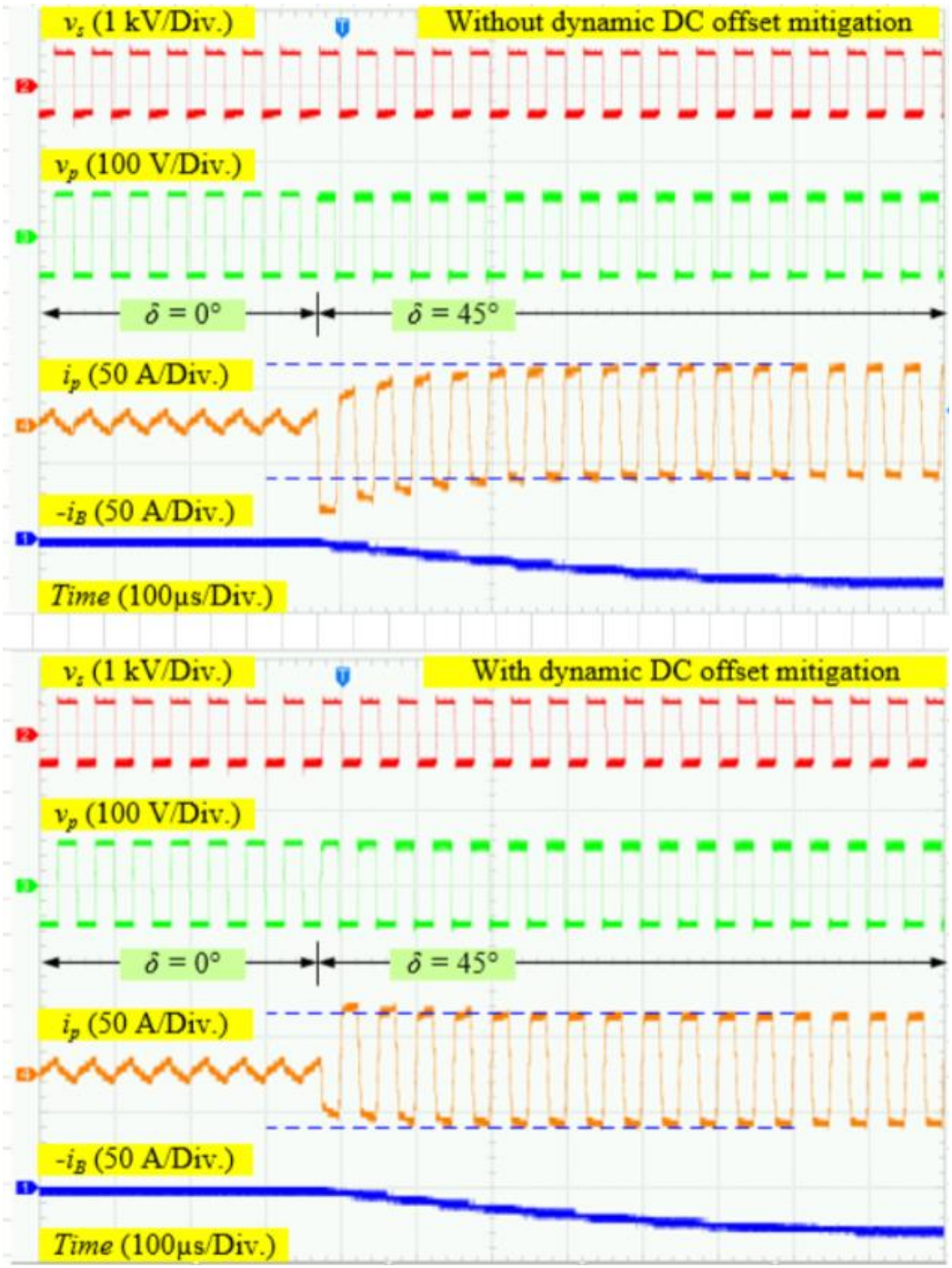


Figure 48 Open-loop transient response of the DAB DC-DC converter with and without the dynamic DC offset compensation scheme: where δ^* changing

from 0 to π/4

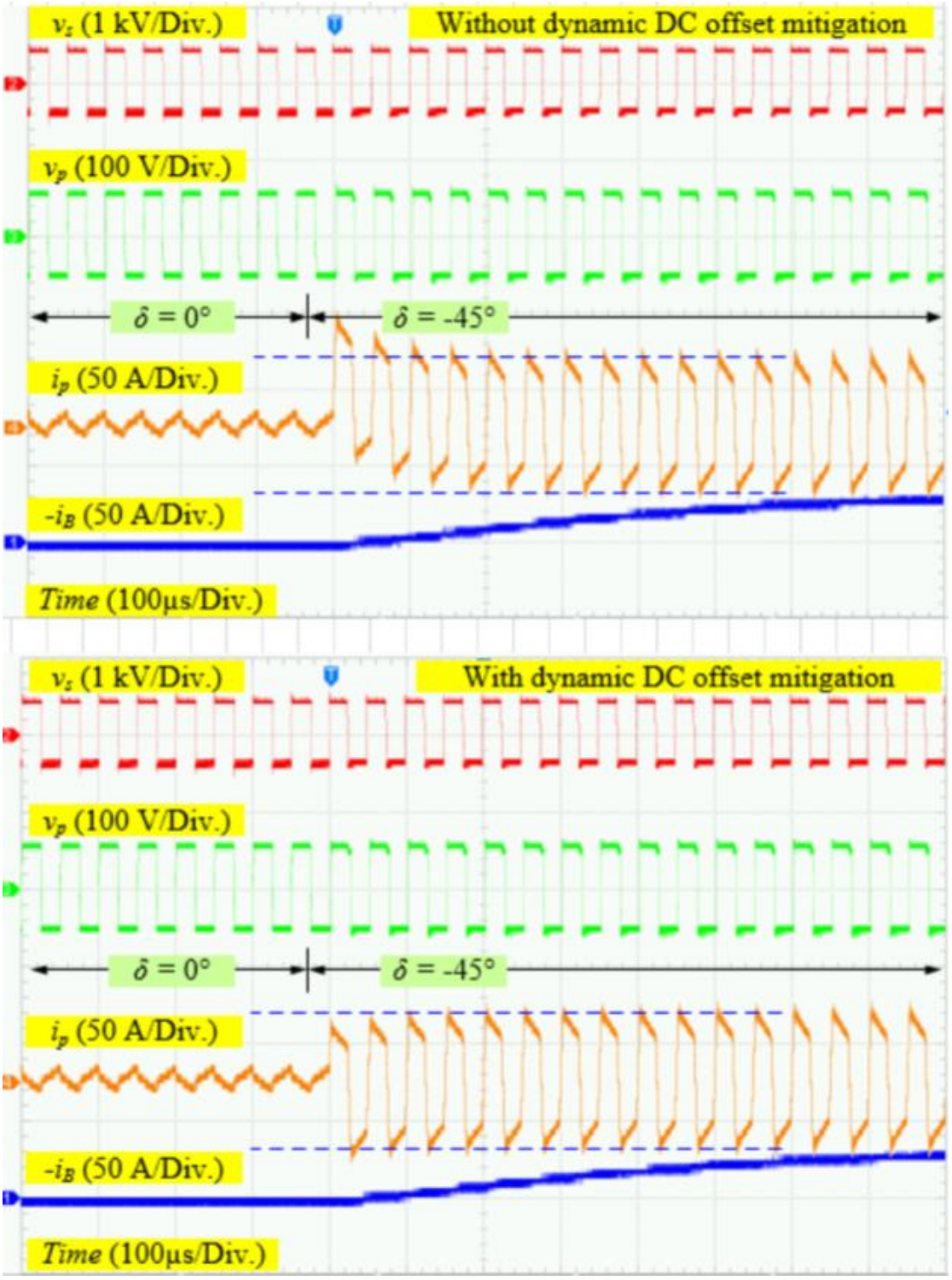


Figure 49 Open-loop transient response of the DAB DC-DC converter with and without the dynamic DC offset compensation scheme: where δ^* changing from 0 to -π/

Validation of the closed-loop control of the battery current

The battery current control loop is optimized to ensure a smooth response, achieving a settling time of approximately 80 ms. The reference battery current, denoted as i_B^* , is configured to maintain the battery power within the range of ±1.5 kW. Figures 50 to 53 present the experimental outcomes in the discharging mode with a battery power of 1.5 kW. Despite the power drawn from the battery leading to an increase in the bus voltage, the bus voltage controller effectively brings it back to the reference level of 400 V within four cycles, as demonstrated in Figure 50. Figure 51 illustrates the steady-state waveforms of $v_D(t)$, $v_g(t)$, and $i_g(t)$. Notably, the grid current waveform appears almost sinusoidal owing to the current harmonic controller, which mitigates the harmonic components in the reference grid current and the VSC terminal voltage induced by the dead time. Additionally, Figure 52 reveals that a step change in the battery reference current i_B^* does not induce a DC offset in the transformer's primary current $i_p(t)$, thanks to the implementation of the DC offset compensation scheme within the SPS modulation system depicted in Figure 44. Meanwhile, the battery current $i_B(t)$ smoothly increases toward its reference value. Furthermore, the steady-state waveforms of $v_p(t)$, $v_s(t)$, and $i_p(t)$ in Figure 53 are consistent with the outlined waveforms in Figure 31. At this operational juncture, the battery voltage measures 51.5 V, closely aligning with the designed value of the MF transformer.

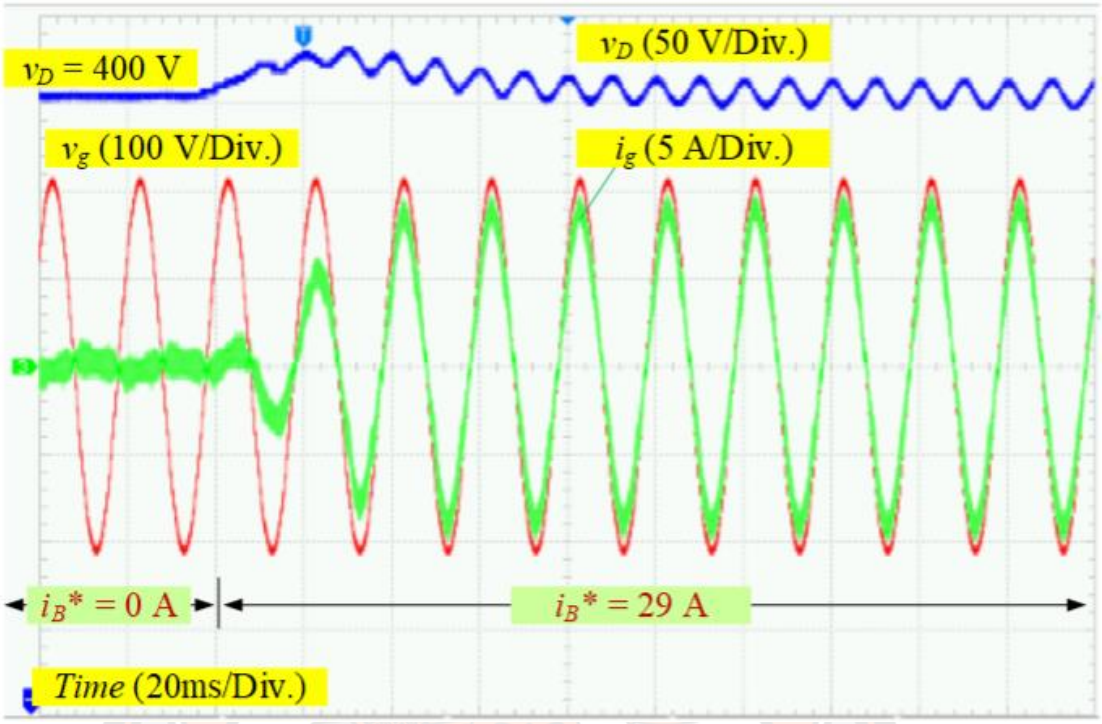


Figure 50 Transient response of the bus voltage $v_D(t)$, grid voltage $v_g(t)$,

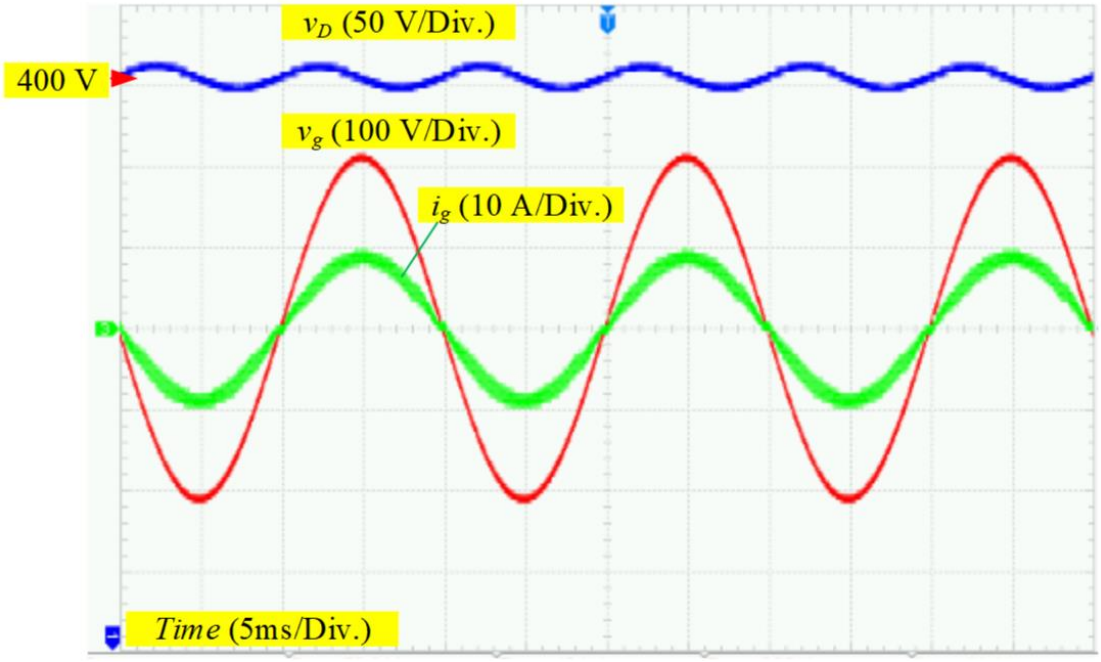


Figure 51 Steady state waveforms of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$

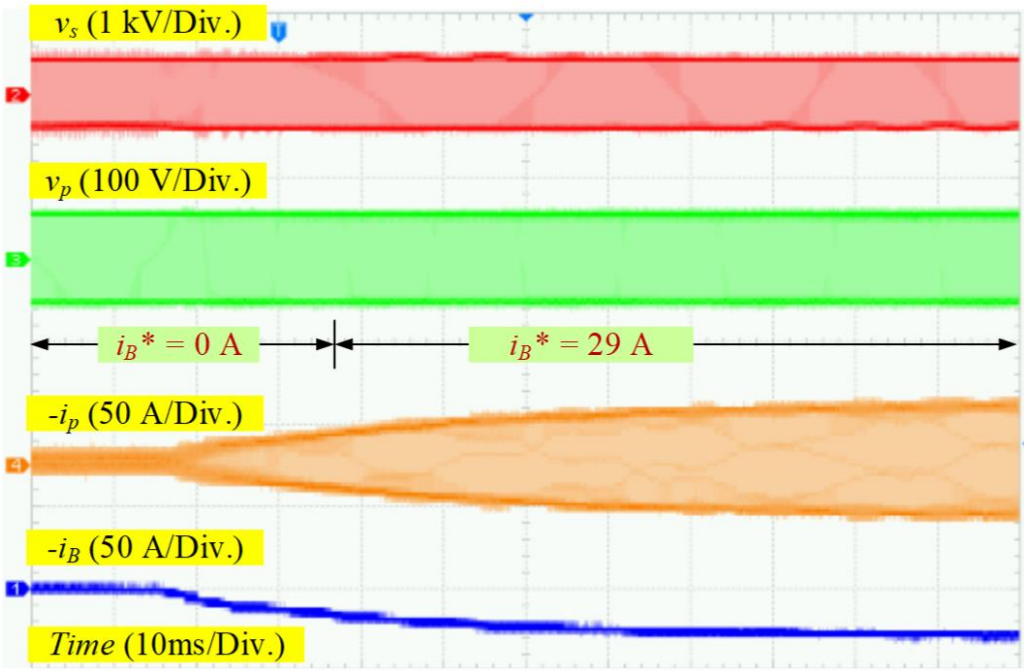


Figure 52 Transient response of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current $-i_B(t)$

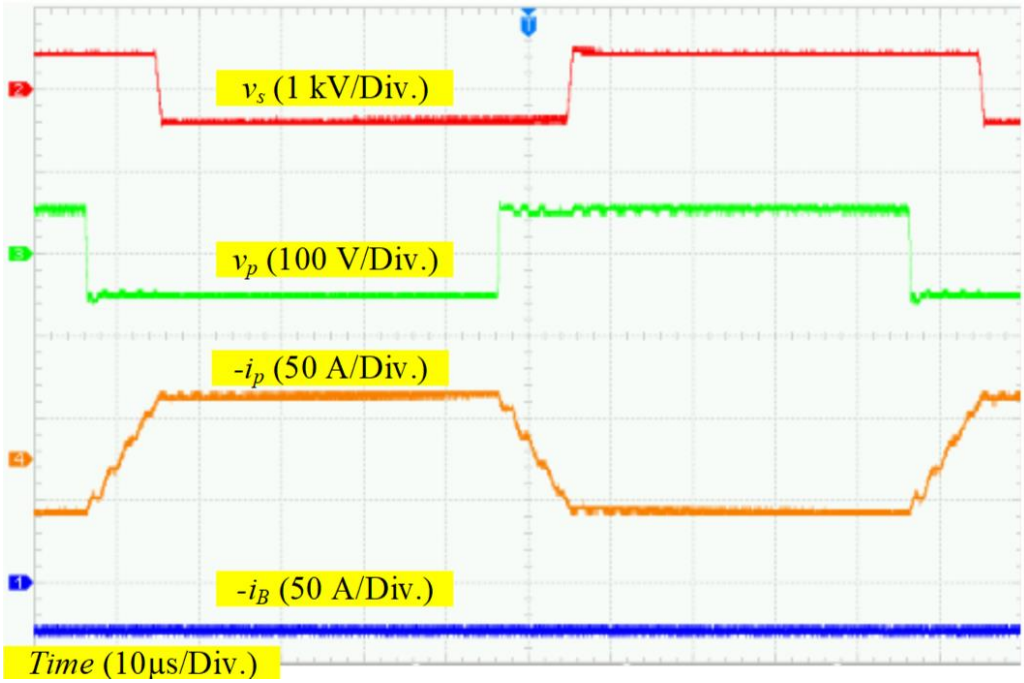


Figure 53 Steady state waveforms of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current $-i_B(t)$.

Figures 54 to 57 exhibit the experimental outcomes in the charging mode with a battery power of -1.5 kW. The response of the bus voltage $v_D(t)$, grid current $i_g(t)$, transformer's primary current $i_p(t)$, and battery current $i_B(t)$ to the battery reference current i_B^* mirrors that observed in the discharging mode but with opposite directions. Despite this reversal, the steady-state grid current waveform remains almost sinusoidal. However, the steady-state waveform $i_p(t)$ suggests that the DAB DC-DC converter operates in the boost mode, where $(N_s/N_p)V_B > V_D$ (Guzmán et al., 2021). At this operational point, the battery voltage was measured at 54.3 V, resulting in $(N_s/N_p)V_B = 424$ V.

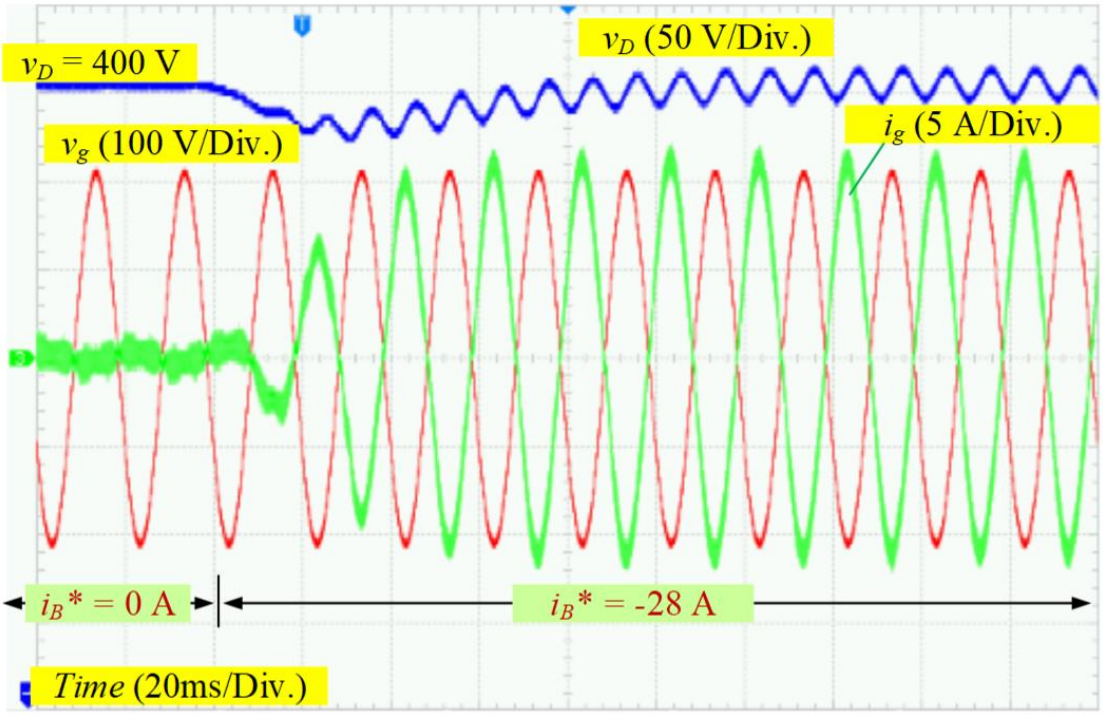


Figure 54 Transient response of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$

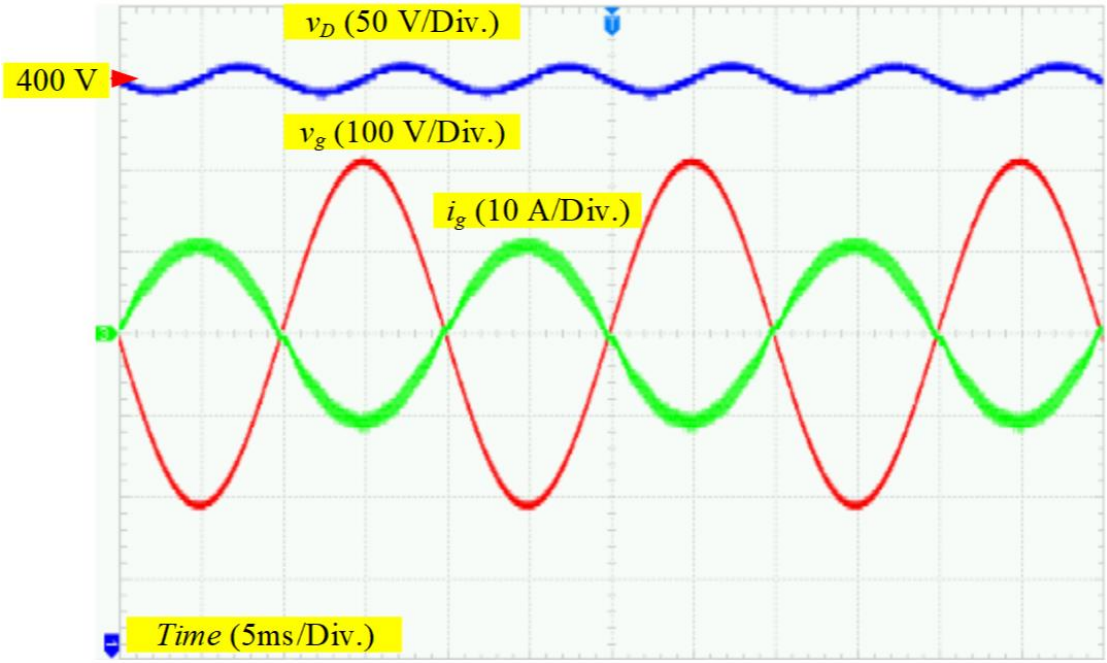


Figure 55 Steady state waveforms of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$

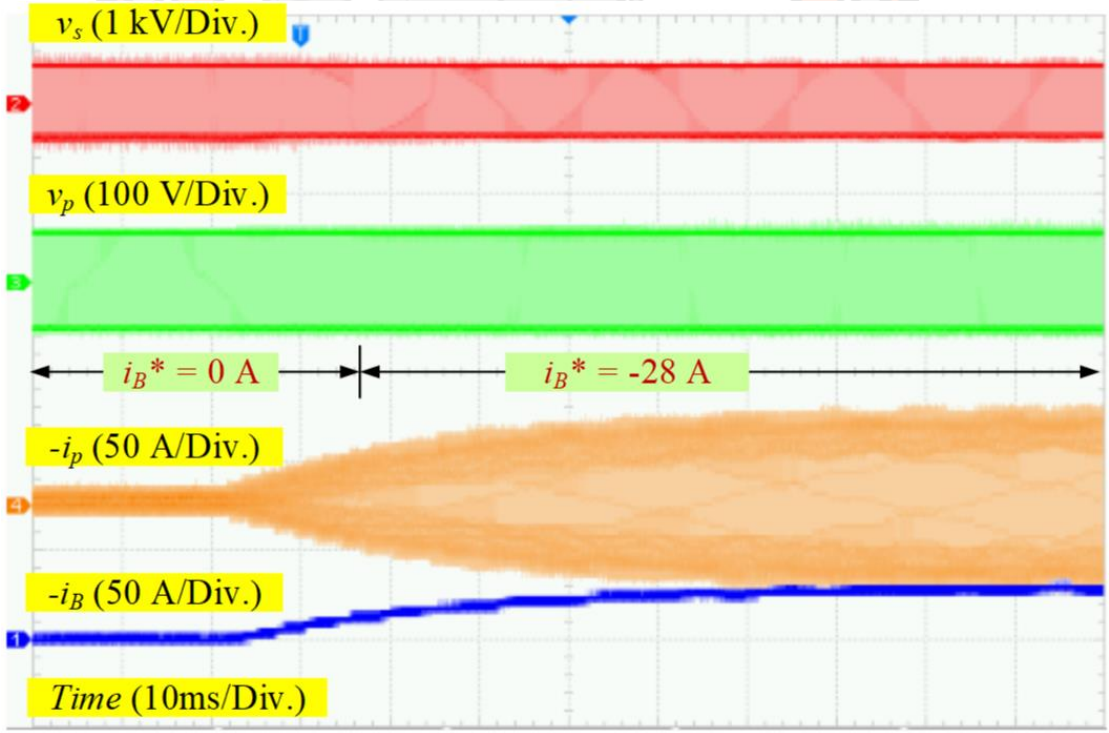


Figure 56 Transient response of the primary and secondary voltages $v_p(t)$ and $v_s(t)$

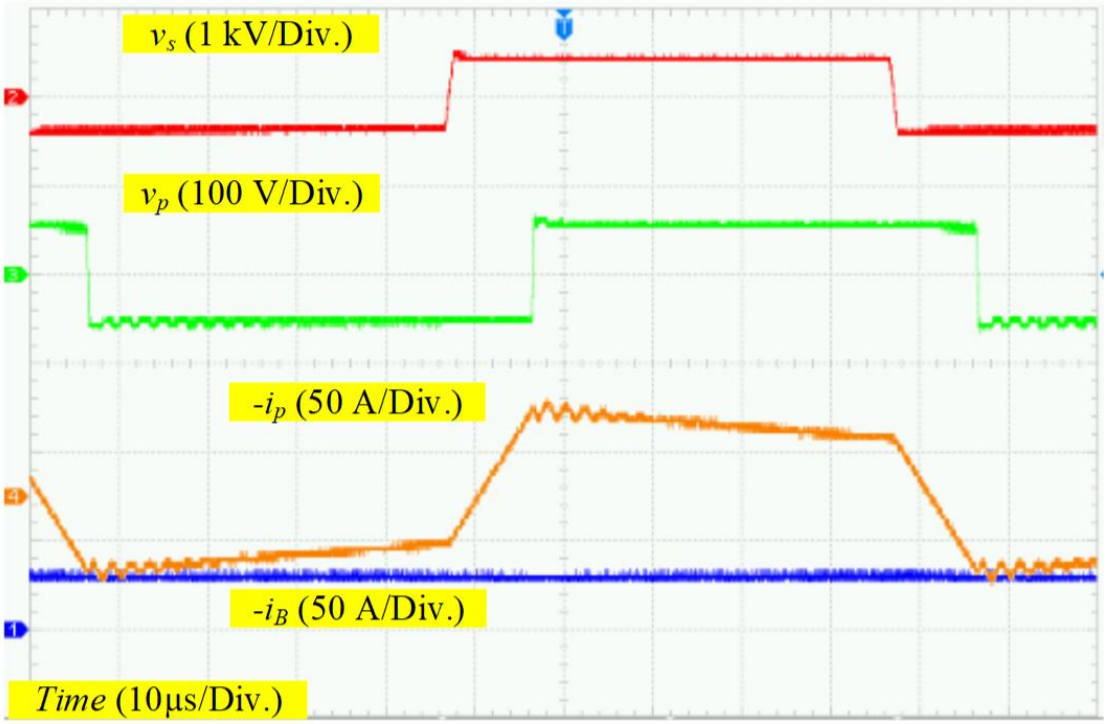


Figure 57 Steady state waveforms of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current

Figure 58 displays the battery voltage of the VSC and the DAB DC-DC converter, while Figure 59 illustrates the total efficiency of both systems. Meanwhile, Figure 60 showcases the total harmonic distribution (THD_i) of the grid current concerning the battery power. As anticipated, the battery voltage is higher in the charging mode compared to the discharging mode. Furthermore, the inverter's efficiency in the charging mode is lower than that in the discharging mode. This discrepancy is attributed, in part, to the mismatched voltage ratio in the MF transformer, which shifts the operating point away from the ZVS region and increases the RMS values in the transformer currents (De Doncker et al., 1991). Therefore, employing a variable DC voltage strategy with the battery voltage and adjusting the duty ratio of the transformer could enhance the inverter's efficiency. The THD_i values at 50% of the rated power are below 1.5%, and it is anticipated that they would be even lower at the full power operation.

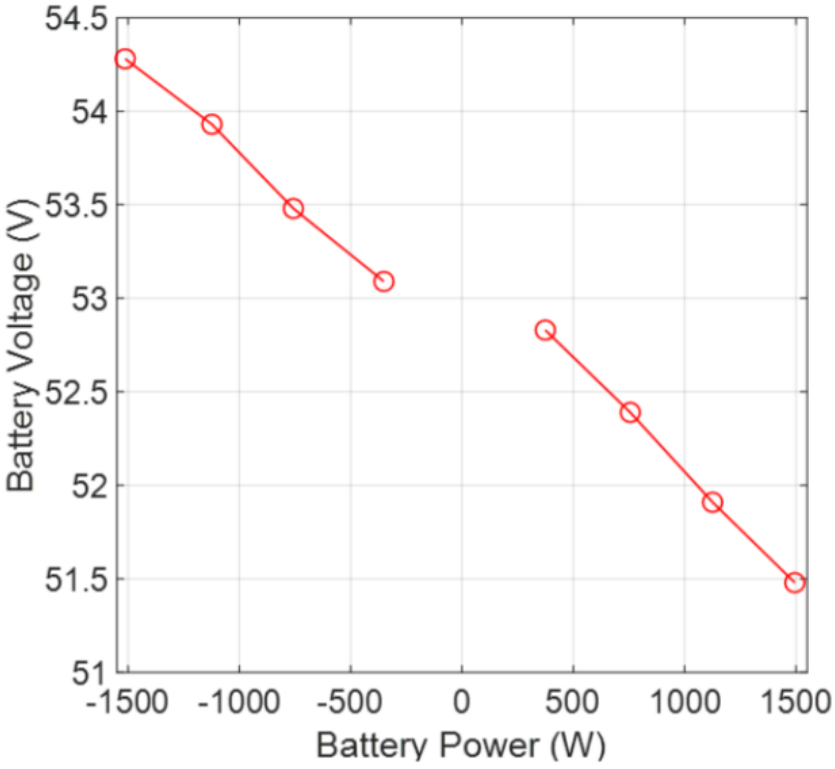


Figure 58 Battery voltage V_B with the battery power.

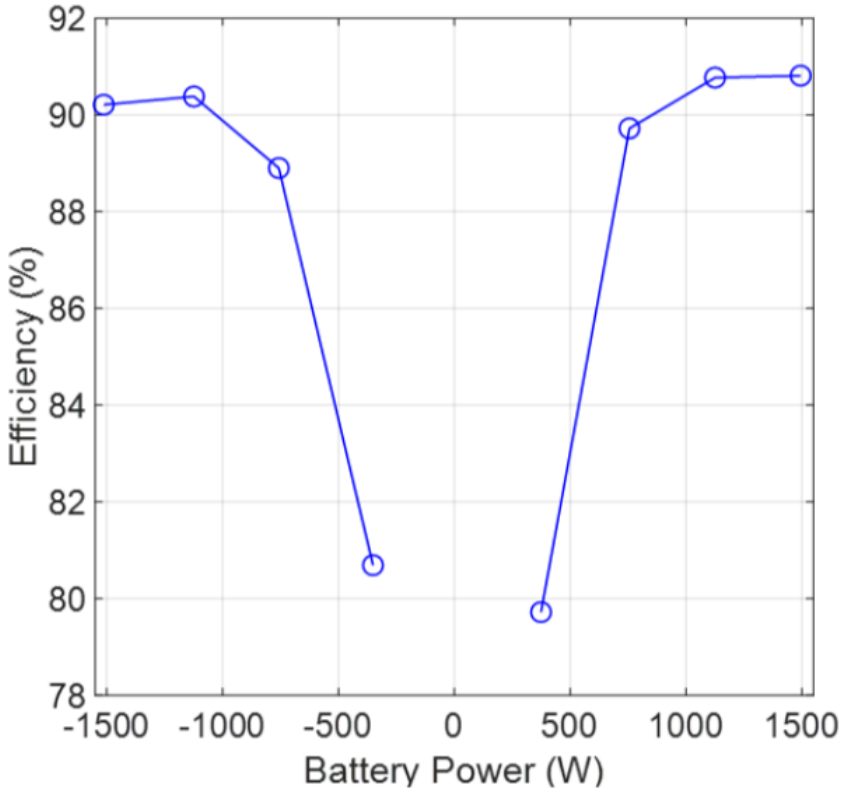


Figure 59 Inverter efficiency with the battery power.

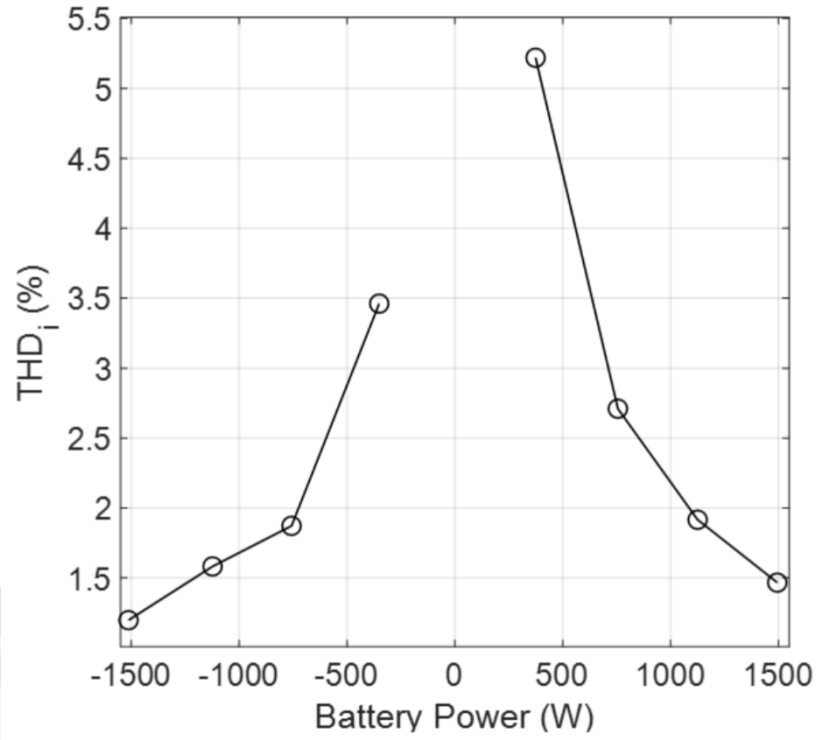


Figure 60 Total harmonic distortion of the grid current with the battery power.

CHAPTER V

DISCUSSION, CONCLUSION, AND FUTURE WORKS

Discussion

The discussion provided outlines the successful construction of a single-phase grid-connected 51.2-V battery inverter, incorporating an LCL-filtered voltage source converter (VSC) and a dual active bridge (DAB) DC-DC converter. Control systems for both converters were implemented on a TMS320F280049C microprocessor, operating at a sampling, and switching frequency of 20 kHz. The DAB DC-DC converter utilized a single-phase shift modulation strategy, facilitated by two separate compare registers synchronized with the time base counters. Additionally, DC offset compensation integrated into the battery current control loop enabled smooth current transitions in response to reference changes. The VSC employed bus voltage control with a unified harmonic mitigation strategy. Experimental validations demonstrated system efficiency exceeding 90% and total harmonic distortion in grid current below 1.5%. However, there are areas for further improvement:

1. Develop advanced battery current control schemes independent of battery impedance parameters.
2. Increase switching frequency and refine modulation strategies of the DAB DC-DC converter to enhance efficiency and power density.
3. Optimize the design of the ripple filter on the battery side.

Conclusion

The improvement and deployment of a single-phase grid-connected 51.2-V battery inverter system signifies a substantial leap forward in the realm of power electronics and energy conversion. This system is characterized by its unique composition, incorporating both an LCL-filtered voltage source converter (VSC) and a dual active bridge (DAB) DC-DC converter, both of which play pivotal roles in achieving heightened efficiency and reliability in the conversion and transmission of electrical energy between the battery and the grid, as well as in the reverse direction.

At the core of this pioneering system lies the combination of control systems for both the VSC and DAB converters into a unified interrupt service routine, expertly managed by the sophisticated TMS320F280049C microprocessor. The selection of this microprocessor is deliberate, owing to its robust processing capability, which is indispensable for orchestrating the intricate control algorithms necessary for efficient energy conversion. Operating at a noteworthy sampling and switching frequency of 20 kHz, the system ensures meticulous and responsive control over the power conversion processes, underscoring its precision and reliability in operation.

A notable feature of the system's design is the synchronization of the time base counters for the switching generation of the DAB DC-DC converter with those of the VSC. This synchronization is crucial for ensuring accurate control and maintenance of the phase shifts, which are essential for the efficient transfer of energy between the DC and AC domains. The implementation of a single-phase shift modulation strategy in the DAB converter is facilitated by adjusting two separate compare registers in conjunction with the time base counters during both the count-up and count-down periods. Implementing this modulation strategy on conventional microcontrollers commonly utilized for power converter control is simple, showcasing the system's efficiency in design and its ability to adapt.

Moreover, the system integrates DC offset compensation into the battery current control loop. This functionality is instrumental in facilitating seamless adjustments in the currents of both the battery and the medium-frequency transformer when there are alterations in the reference current step. Smooth transitions are essential to maintain system stability and prevent abrupt power fluctuations that could harm system components or affect performance.

The VSC utilizes a bus voltage control strategy coupled with a unified method for harmonic mitigation, guaranteeing high-quality power transmission to or from the grid with minimal harmonic distortion. Harmonic distortion poses a substantial risk in power systems, potentially causing inefficiencies and instability. Hence, the system's capability to uphold harmonic distortion in the grid current below 1.5% underscores its efficient design and adept control strategies, affirming its effectiveness in mitigating potential issues associated with harmonic distortion in power systems.

Experimental evaluations of the system have unveiled its exceptional performance, particularly in terms of efficiency and power quality. The system's overall efficiency surpasses 90%, indicating that a significant portion of electrical power is efficiently converted and transmitted with minimal losses. This elevated efficiency level is critical for maximizing energy utilization and reducing operational costs in grid-connected situations, underscoring the system's effectiveness in optimizing energy usage and improving cost-effectiveness across diverse applications.

In conclusion, the created single-phase grid-connected battery inverter system demonstrates the capability of incorporating sophisticated control algorithms, accurate modulation strategies, and effective design principles to enhance the efficiency and dependability of energy conversion systems. The system's impressive efficiency, minimal harmonic distortion, and seamless control mechanisms underscore its appropriateness for diverse applications, making a substantial contribution to the progression of contemporary power electronics and energy systems.

Future Works

There are several areas of potential future work to enhance the performance of the residential battery inverter:

Advanced Battery Current Control Methods:

- Develop sophisticated control algorithms capable of regulating battery currents effectively, irrespective of variations in internal impedance.
- Explore adaptive control strategies like sliding mode control or model predictive control designed to handle dynamic battery impedance.

Increased Switching Frequency and Improved Modulation Techniques:

- Investigate ways to elevate the switching frequency of the DAB DC-DC converter while minimizing electromagnetic interference.
- Experiment with advanced modulation approaches such as phase-shifted control or optimized PWM strategies to enhance converter efficiency and compactness.

Optimization of Battery-Side Ripple Filtering:

- Refine the design of ripple filters on the battery side to reduce unwanted current fluctuations and optimize overall system performance.
- Evaluate different filter configurations, including active and hybrid filters, to effectively mitigate ripples without compromising efficiency.

System Integration and Testing:

- Conduct thorough integration testing across various operational scenarios to validate and refine performance enhancements.
- Gather real-world data to identify areas for improvement and ensure reliability under diverse conditions.

Advanced Control Algorithm Implementation:

- Implement advanced control techniques to optimize system response time, stability, and energy efficiency.
- Investigate adaptive and predictive control strategies tailored to address dynamic system behaviors and disturbances.

Efficiency Improvement and Component Optimization:

- Focus on optimizing system efficiency through careful selection of components, effective thermal management, and efficient circuit layout.
- Explore new materials and technologies to minimize power losses and enhance overall efficiency.

Reliability and Fault Tolerance Enhancements:

- Implement robust fault detection and protection mechanisms to enhance system reliability and safety.
- Incorporate diagnostic features and redundancy strategies to mitigate potential failure modes and ensure continuous operation.

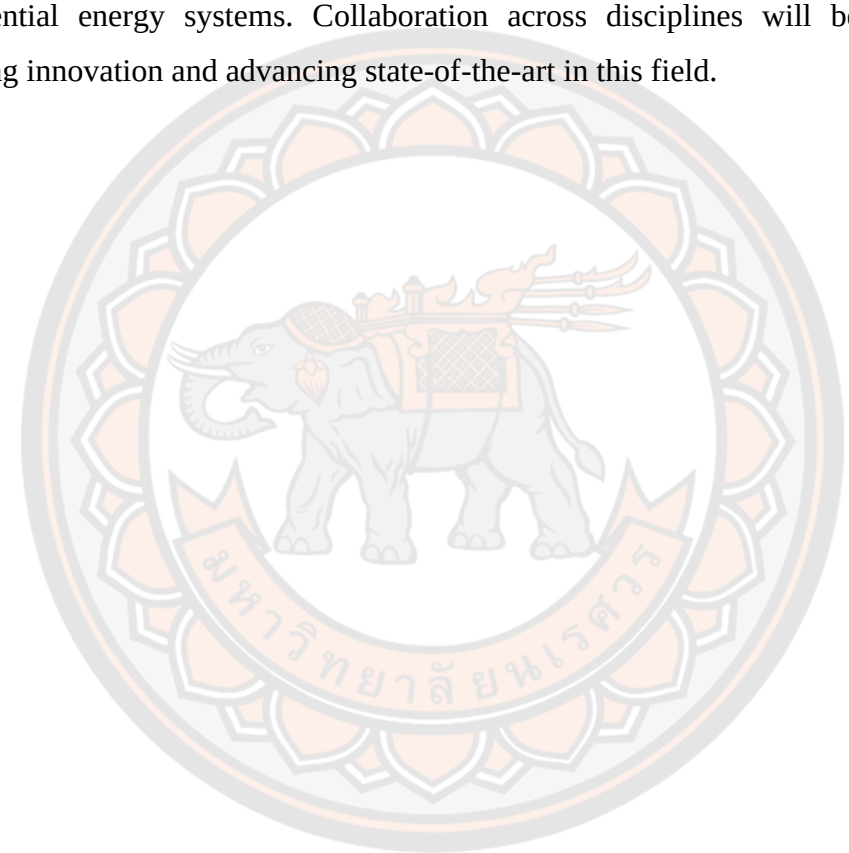
Lifecycle Assessment and Sustainable Design:

- Conduct lifecycle assessments to evaluate environmental impact and identify opportunities for sustainability improvements.
- Explore design strategies focused on recyclability, energy efficiency, and responsible end-of-life management.

User Interface and Monitoring Enhancements:

- Improve user interface and monitoring capabilities to provide users with real-time feedback on system performance and energy usage.
- Develop intuitive interfaces and remote monitoring solutions to enhance user experience and system control.

By pursuing these future directions, the residential battery inverter can be optimized to deliver higher efficiency, reliability, and functionality in grid-connected residential energy systems. Collaboration across disciplines will be essential to driving innovation and advancing state-of-the-art in this field.



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APPENDIX

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Received 29 December 2022, accepted 11 January 2023, date of publication 16 January 2023, date of current version 23 January 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3237039

STANDARDS

Fast Bus Voltage Control of Single-Phase Grid-Connected Converter With Unified Harmonic Mitigation

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This work was supported in part by the Royal Golden Jubilee (RGJ) Ph.D. Program under Grant PHD0228256O, and in part by the National Research Council of Thailand and Sathien Plastic and Fiber Company Ltd. under Grant NR23D650006.

ABSTRACT This paper presents a comprehensive analysis of the harmonic sources of the single-phase grid-connected voltage source converter (VSC), which leads to an alternative approach for DC bus voltage control of the VSC under grid voltage distortion with a significant switching dead time. A selective current harmonic controller with the zero-reference structure plays a vital role in rejecting the harmonic components in the grid reference current created by the bus voltage control loop and the harmonic components in the grid voltage and in the VSC caused by the switching dead time. Therefore, the bus voltage control can adopt a conventional proportional-integral regulator tuned at a fast bandwidth. The proposed control scheme implemented in the multiple unbalanced synchronous reference frames was validated with a bidirectional 2-kVA VSC under grid voltage distortion and a significant dead time. Furthermore, the proposed control scheme exhibited the transient response and grid current quality superior to the conventional bus voltage control methods with a notch filter and a low-pass filter. The proposed control scheme has inherent frequency adaption.

INDEX TERMS Current distortion, dead time, double-frequency ripple, renewable energy.

I. INTRODUCTION

Single-phase voltage source converters (VSCs) are widely used for grid integration of renewable energy sources [1], [2], [3], [4], battery storage systems [5], railway traction systems [6], and on-board battery chargers of plug-in vehicles [7], [8]. Fig. 1 depicts a typical application of the VSC, where the DC bus voltage $v_D(t)$ usually connects to a DC-DC converter or a 3-phase VSC. The control system of such VSCs generally comprises the cascade configuration with the outer DC bus voltage control loop and the inner grid current loop. The main control objectives are to have low bus voltage fluctuation and fast transient response under a sudden change in the bus power, and low grid current distortion. However, the distorted grid reference current $i_g^*(t)$, the distorted voltage $v_{pcc}(t)$ at the point of common coupling (PCC), and the VSC terminal voltage $v_c(t)$ distorted by a dead-time voltage $v_{DT}(t)$, introduce harmonic components in the grid current $i_g(t)$.

The presence of the double-frequency ripple in the DC bus voltage control loop distorts the reference current for the grid current control loop. The distorted reference current is conventionally minimized by tuning the bus voltage at a bandwidth much lower than the double frequency, says 10 Hz [2]. So, bulky aluminum electrolytic capacitors are used to limit large bus voltage transient fluctuation. In addition, active ripple cancellation circuits [9], [10] decoupled the pulsating power from the average power, which resulted in a lower bus capacitance and a higher loop bandwidth. However, these techniques require extra semiconductor switches, additional passive components, and additional control schemes.

The ripple voltage can be permitted to reduce the bus capacitance [11]. Thus, increasing the bandwidth of the bus voltage control loop decreases the transient voltage fluctuation. Furthermore, distortion in the reference

The associate editor coordinating the review of this manuscript and approving it for publication was Qiang Li.

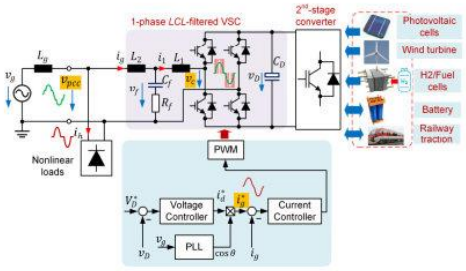

FIGURE 1. Single-phase LCL-filtered VSC and DAB DC-DC converter under this study.

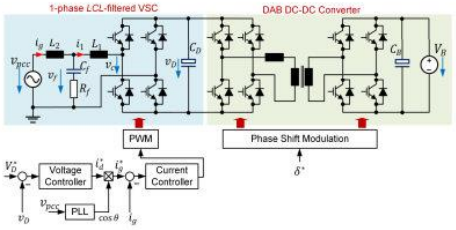

FIGURE 2. Single-phase LCL-filtered VSC and DAB DC-DC converter under this study.

TABLE 1. Parameters of the VSC and DAB DC-DC converter.

Parameters	Values
RMS line voltage	220 V
Nominal frequency	50 Hz
Nominal output DC bus voltage, V_D	400 V
Maximum apparent power	2 kVA
VSC-side and grid-side inductor, L_1 and L_2	1 mH
L_1 and L_2 winding resistance, R_1 and R_2	0.07 Ω
Filter capacitor, C_f	2.2 μF
Damping resistor, R_f	2.2 Ω
Bus capacitor, C_D	680 μF
Transformer ratio	1:1
Nominal DC output voltage, V_B	400 V
Output capacitor, C_B	1,100 μF
Switching and sampling frequencies	20 kHz

current is generally minimized by blocking the ripple voltage into the bus voltage control loop. The most common solution is a notch filter to block the double-frequency ripple [1], [12], [13], [14] [15]. Alternative methods are adaptive bus voltage control [16], ripple voltage estimators [17], [18], nonlinear observers [19], and bus voltage sampling synchronized with the grid frequency [20]. Thus, these approaches create a *clean* reference current with a fast DC bus voltage control.

The harmonic voltages also cause grid current distortion at the PCC and the VSC terminals due to a dead time T_{DT} in each VSC leg [21], [22]. Feedforward of the PCC voltage partly mitigates the grid current distortion [22]. However, a DC offset in the voltage measurement induces an undesirable DC component injecting to the grid [23]. The dead-time effect is highly nonlinear, depending on the VSC current direction. The dead-time voltage can be minimized by the compensated duty ratio calculated from an adaptive algorithm [24] or an immune algorithm [25]. The PCC and dead-time harmonic voltages are the grid current control loop's disturbances, which can be mitigated by using a grid current controller with selective harmonic mitigation. Multi-frequency synchronous reference frame controllers [22], multi-frequency proportional-resonant controllers [22], [26], [27], and repetitive controllers (RC) were proven to be effective solutions [21].

To this end, the grid current problems due to the distorted reference current and the harmonic voltages have yet to be considered simultaneously. The bus voltage control schemes in [12], [13], [14], [16], [17], [18], [19], and [20] were carried out under a sinusoidal voltage with negligible dead time. Meanwhile, a sinusoidal reference was applied to the current control loop under the grid voltage harmonics [21], [22] and the dead-time voltage compensation schemes [21], [22], [24], [25], which do not guarantee a sinusoidal grid current with the bus voltage control loop. Therefore, we present a comprehensive analysis of the current harmonic sources of the single-phase grid-connected VSC, which results in an alternative approach to the VSC bus voltage control under a distorted PCC voltage and a significant VSC dead time. This study adopts the unbalanced synchronous reference frame current controller [28] with the zero-reference configuration of selective harmonic compensators for simultaneous attenuation of the harmonic components in the reference current, PCC voltage, and VSC terminals due to the dead time.

With this current control structure, a conventional proportional-integral (PI) regulator can be applied for the bus voltage control. The proposed control structure allows the bandwidth of the DC bus voltage control loop to increase without sacrificing the grid current quality. The proposed control methodology was validated with a single-phase 2-kVA *LCL*-filtered VSC with a dual active bridge (DAB) DC-DC as the second stage converter, which was compared with the existing control methods under grid frequency variation, distorted grid voltage, and a significant dead time.

II. SYSTEM DESCRIPTION AND ANALYSIS OF HARMONIC SOURCES

A 2-kVA *LCL*-filtered grid-connected VSC shown in Fig. 2 with the parameters summarized in Table 1 is selected in this study. According to the grid current notation, the VSC is operated as the rectifier mode. The DC bus is connected to a DAB DC-DC converter as the second-stage converter for interfacing with a 400-V bidirectional DC source. This

topology can be employed in bidirectional onboard electric vehicle chargers, and locomotive traction transformers. The bidirectional bus power is controlled by the phase shift modulation of the DAB DC-DC converter through the phase angle δ between the primary and secondary voltages of the medium frequency transformer.

A. GRID CURRENT DISTORTION DUE TO VOLTAGE HARMONICS

Fig. 3 shows the VSC's grid current control block diagram in the stationary reference frame. The distorted PCC voltage $v_{pcc}(t)$ is considered in this study, which is written by

$$v_{pcc}(t) = \underbrace{\hat{V}_1 \cos\theta}_{v_1(t)} + \underbrace{\sum_{h=2}^{n} \hat{V}_h \cos(h\theta + \psi_h)}_{v_h(t)} \tag{1}$$

where $\theta = \omega t$, $\hat{V}_1$, and $\hat{V}_h$ are the voltage amplitudes, and ψ_h is the phase angle of each harmonic component. The current controller $G_{ci}(s)$ can be a proportional-resonant (PR) regulator in the stationary reference frame or a PI regulator in the synchronous reference frame, which provides an infinite gain at the grid frequency ω for a zero steady-state error. The LCL filter governs the grid current $i_g(t)$ as follows.

$$L_2 \frac{di_g(t)}{dt} + R_2 i_g(t) = v_{pcc}(t) - v_f(t) \tag{2}$$

$$v_f(t) = v_{cf}(t) + R_f\left(i_g(t) - i_1(t)\right) \tag{3}$$

$$C_f \frac{dv_{cf}(t)}{dt} = i_g(t) - i_1(t) \tag{4}$$

$$L_1 \frac{di_1(t)}{dt} + R_1 i_1(t) = v_f(t) - \underbrace{\left(v_{c1}(t) + v_{DT}(t)\right)}_{v_c(t)} \tag{5}$$

Neglecting the switching frequency components, the VSC ideal output voltage $v_{c1}(t)$ in (5) is controlled through the modulation signal $m^*(t)$ given by

$$v_{c1} \approx V_D m^*(t). \tag{6}$$

Equations (2)-(6) illustrate that the grid current $i_g(t)$ is controlled through the modulation signal $m^*(t)$ with $v_{pcc}(t)$ and $v_{DT}(t)$ as the disturbances, which will introduce low-order harmonics into the grid current. The dead-time voltage $v_{DT}(t)$ in (5) can be approximated by

$$v_{DT}(t) \approx \frac{2T_{DT}}{T_{SW}} \text{sign}\left(i_1(t)\right) v_D(t) \tag{7}$$

where T_{SW} is the switching period. This $v_{DT}(t)$ can be compensated in $m^*(t)$ using (7). However, for the LCL filter with the grid current feedback control used in this study, an additional current sensor is required for the dead time voltage compensation. A feedforward of $v_{pcc}(t)$ mitigates the grid current distortion to some extent [22]. However, there can be a DC offset in the voltage measurement, inducing a DC component in the grid current [23].

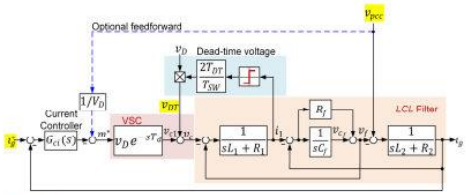

FIGURE 3. Single-phase LCL-filtered VSC and DAB DC-DC converter under this study.

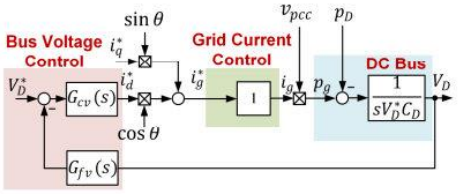

FIGURE 4. Equivalent bus voltage control block diagram.

B. GRID CURRENT DISTORTION DUE TO THE BUS VOLTAGE CONTROL

Fig. 4 depicts the simplified block diagram of the bus voltage control loop, where the grid current control loop is approximated as a unity gain. The bus voltage $v_D(t)$ passes through the bus voltage filter $G_{fv}(s)$ to compare with the reference bus voltage V_D^* for the bus voltage controller $G_{cv}(s)$. The bus voltage filter can be a low-pass filter or a notch filter tuned at 2ω. A PI regulator is normally employed as the bus voltage controller. The bus voltage controller generates the reference current i_d^* representing the required active power drawn from/injected into the grid. The reference current i_q^* is used to set the reactive power. The reference currents i_d^* and i_q^* are multiplied by $\cos\theta$ and $\sin\theta$ templates obtained from a phase-locked loop (PLL), forming the reference signal i_g^* for the inner current control loop.

Let us consider that the grid current $i_g(t)$ initially consists of a DC component I_{g0} and the AC fundamental component AC $i_{g1}(t)$ in this analysis. The grid current $i_g(t)$ is given as

$$i_g(t) = I_{g0} + \underbrace{\frac{I_1 \cos(\theta + \phi_1)}{i_{g1}(t)}} \tag{8}$$

where $\hat{I}_1$ and ϕ_1 are the amplitude and phase angle of $i_{g1}(t)$. Asymmetry in semiconductor properties, gate driver delays, and an offset in the grid current measurement cause the DC component current I_{g0} [29]. The grid current $i_{g1}(t)$ can be decomposed into the active and reactive power-producing components $i_d(t)$ and $i_q(t)$, as given by

$$i_{g1}(t) = \underbrace{\hat{I}_1 \cos\phi_1}_{i_d} \cos\theta - \underbrace{\hat{I}_1 \sin\phi_1}_{i_q} \sin\theta. \tag{9}$$

With the fundamental component of the PCC voltage, the instantaneous grid power can be written as follows

$$\left.\begin{aligned} p_g(t) &= v_{pcc}(t)\cdot i_g(t) \\ p_g(t) &= \underbrace{\frac{\hat{V}_1}{2}\hat{I}_1\cos\phi_1}_{P_{g1}} + \underbrace{\frac{\hat{V}_1}{2}\hat{I}_1\cos(2\theta+\phi_1)}_{\tilde{p}_{g1}(t)} \\ &\quad + \underbrace{\hat{V}_1 I_{DC_g}\cos\theta}_{\tilde{p}_o} \\ p_g(t) &= \underbrace{\frac{\hat{V}_1}{2}i_d}_{P_{g1}} + \underbrace{\frac{\hat{V}_1}{2}i_d\cos 2\theta}_{\tilde{p}_{g1}(t)} - \underbrace{\frac{\hat{V}_1}{2}i_q}_{Q_{g1}}\sin 2\theta \\ &\quad + \underbrace{\hat{V}_1 I_{DC_g}\cos\theta}_{\tilde{p}_o} \end{aligned}\right\} \quad (10)$$

The instantaneous grid power consists of the average power P_{g1} and the oscillating power components $\tilde{p}_{g1}(t)$ and $\tilde{p}_0(t)$ due to the AC and DC components of the grid current. Neglecting losses in the LCL filter and VSC, the power balance at the DC bus can be written as

$$v_D(t)\left(C_D\frac{dv_D(t)}{dt}\right) = p_g(t) - P_D(t) \quad (11)$$

where $P_D(t)$ is the bus output power feeding the DAB DC-DC converter. Assume $v_D(t)$ is tightly regulated around the reference value V_D^* [19]. Therefore, the linearization of (11) yields

$$V_D^*\left(C_D\frac{dv_D(t)}{dt}\right) \approx p_g(t) - P_D(t) \quad (12)$$

The bus voltage $v_D(t)$ consists of the average value $V_D(t)$ and the ripple component $\tilde{v}_D(t)$ as given by

$$v_D(t) = V_D(t) + \tilde{v}_D(t). \quad (13)$$

Thus, substitution of (10) and (13) into (12) results in the average and oscillating components as follows.

$$V_D^* C_D\frac{dV_D(t)}{dt} \cong \frac{\hat{V}_1}{2}i_d - P_D(t). \quad (14)$$

$$V_D^* C_D\frac{d\tilde{v}_D(t)}{dt} \cong \tilde{p}_{g1}(t) + \tilde{p}_0(t). \quad (15)$$

Note that the dynamic of the average bus voltage (14) is accurate when the loop bandwidth is less than the oscillating frequency components. The oscillating powers $\tilde{p}_{g1}(t)$ and $\tilde{p}_0(t)$ lead to an approximation of the bus voltage ripple as

$$\left.\begin{aligned} \tilde{v}_D(t) &\approx \tfrac{1}{V_D^* C_D}\int\left(\tilde{p}_{g1}(t)+\tilde{p}_0(t)\right)dt \\ \tilde{V}_D(t) &\approx \underbrace{\frac{\hat{\nabla}_1 I_1}{4\omega C_D V_D^*}\sin(2\theta+\phi_1)}_{\tilde{v}_{D2\omega}} + \underbrace{\frac{\bar{\nabla}_1 I_D C_g}{\omega C_D V_D^*}\sin\theta}_{\tilde{v}_{D\omega}} \end{aligned}\right\}. \quad (16)$$

The oscillating power component $\tilde{p}_{g1}(t)$ causes the 2ω ripple component $\tilde{v}_{D2\omega}(t)$, and the ω component $\tilde{v}_{D\omega}(t)$ is due to I_{g0}. These two ripple components pass through the bus voltage control loop. Then, the bus voltage controller $G_{cv}(s)$ creates the reference current $i_d^*(t)$ as

$$i_d^*(t) = \hat{I}_1\cos\phi_1 + \underbrace{\hat{I}_{rp2}\cos(2\theta+\psi_2)}_{i_{d2\omega}^*(t)} + \underbrace{\hat{I}_{rp1}\cos(\theta+\psi_1)}_{i_{d\omega}^*(t)} \quad (17)$$

where the ripple components $\tilde{i}_{d\omega}^*(t)$ and $\tilde{i}_{d2\omega}^*(t)$ in $i_d^*(t)$ are the residues from the bus voltage regulator. The bus voltage control loop governs the amplitudes $\hat{I}_{rp2}$ and $\hat{I}_{rp1}$, and phase angles ψ_2 and ψ_1. The reference grid current is given by

$$i_g^*(t) = i_d^*(t)\cos\theta + i_q^*(t)\sin\theta. \quad (18)$$

Substitution of (17) into (18) results in

$$\begin{aligned} i_g^*(t) &= \underbrace{\hat{I}_1\cos\phi\cos\theta}_{Active power} - \underbrace{i_q^*\sin\theta}_{Reactive power} \\ &\quad + \underbrace{\frac{I_{rp2}}{2}\cos(\theta+\psi_2)}_{Additional reactive power} + \underbrace{\frac{I_{rp2}}{2}\cos(3\theta+\psi_2)}_{i_{g3}^*(t)} \\ &\quad + \underbrace{\hat{I}_{rp1}\cos\psi_1 + \hat{I}_{rp1}\cos(2\theta+\psi_1)}_{Caused by I_{g0}}. \end{aligned} \quad (19)$$

The desired components of $i_g^*(t)$ are the first two terms in (19). The 2ω ripple component creates the 3rd harmonic and additional reactive power components, which are generally attenuated by a low-bandwidth bus voltage control loop [2] or by a notch filter. The DC component I_{g0} of the grid current causes the DC and 2nd harmonic components in $i_g^*(t)$. This DC component I_{g0} can be minimized by carefully calibrating of the grid measurement. Suppression techniques with additional circuits provide an online adjustment of the DC component [29].

III. ANALYSIS OF HARMONIC MITIGATION TECHNIQUES

A. HARMONIC REJECTION ANALYSIS OF THE GRID CURRENT CONTROL LOOP

Fig. 5 shows the equivalent grid current control block diagram in the stationary reference frame. The *LCL* filter's transfer functions $G_{LCL}(s)$ and $G_{FW}(s)$ are given by

$$G_{LCL}(t) = \frac{sC_f R_f + 1}{C_f L_1 L_2 s^3 + C_f(L_1+L_2)R_f s^2 + C_f(L_1+L_2)s} \quad (20)$$

$$G_{FW}(s) = \left(\frac{L_1 C_f s^2}{C_f R_f s + 1} + 1\right) \quad (21)$$

where L_1, L_2, C_f, and R_f are the *LCL* filter parameters. The VSC's ideal voltage $v_{c1}(t)$ is obtained from the pulse width modulation (PWM) with the modulation signal m^* from the current controller output. The transfer function of the PWM process is modeled as

$$G_{PWM}(s) = \frac{v_{c1}(s)}{m^*(s)} = V_D e^{-sT_d} \quad (22)$$

TABLE 2. Harmonic rejection characteristics of the grid current control structures.

Transfer functions	Parallel HC structure in Fig. 6		Zero-reference HC structure in Fig. 7	
$G_{ci}(s)=\frac{i_g(s)}{i_g^*(s)}$	$\frac{[G_{ci}(s)+G_{cih}(s)]G_{PWM}(s)G_{LCL}(s)}{1+[G_{ci}(s)+G_{cih}(s)]G_{PWM}(s)G_{LCL}(s)}$	(29)	$\frac{G_{ci}(s)G_{PWM}(s)G_{LCL}(s)}{1+[G_{ci}(s)+G_{cih}(s)]G_{PWM}(s)G_{LCL}(s)}$	(32)
$Y_{DT}(s)=\frac{i_g(s)}{v_{DT}(s)}$	$\frac{-G_{LCL}(s)}{1+G_{ci}(s)G_{PWM}(s)G_{LCL}(s)}$	(30)	$\frac{-G_{LCL}(s)}{1+G_{ci}(s)G_{PWM}(s)G_{LCL}(s)}$	(33)
$Y_{pcc}(s)=\frac{i_g(s)}{v_{pcc}(s)}$	$\frac{G_{FW}(s)G_{LCL}(s)}{1+[G_{ci}(s)+G_{cih}(s)]G_{PWM}(s)G_{LCL}(s)}$	(31)	$\frac{G_{FW}(s)G_{LCL}(s)}{1+[G_{ci}(s)+G_{cih}(s)]G_{PWM}(s)G_{LCL}(s)}$	(34)

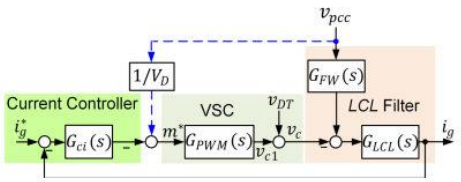

FIGURE 5. Equivalent grid current control block diagram in the stationary reference frame.

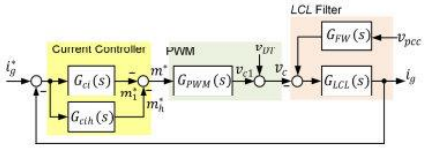

FIGURE 6. Grid current control with parallel HC scheme.

where $T_d = 2T_s$ is the delay time caused by the sampling process and transport delay [30], with T_s as the sampling period. The current controller $G_{ci}(s)$ can be a proportional-resonant (PR) regulator in the stationary reference framer or a proportional-integral (PI) regulator in the synchronous reference frame,

$$G_{ci}(s) = K_{pi} + \frac{K_{ii}s}{s^2+\omega^2} \tag{23}$$

where K_{pi} and K_{ii} are the controller gains. The closed-loop transfer function of the grid current control is given by

$$G_{ci}(s) = \frac{i_g(s)}{i_g^*(s)} = \frac{G_{ci}(s)\,G_{PWM}(s)\,G_{LCL}(s}{1+G_{ci}(s)\,G_{PWM}(s)\,G_{LCL}(s)}. \tag{24}$$

The current controller $G_{ci}(s)$ in (23) has an infinite gain at the grid frequency ω, which forces $|G_{ci}(j\omega)| \approx 1$. Meanwhile, the controller's finite gain at the frequencies 2ω and 3ω still partly tracks the 2ω and 3ω components of $i_g^*(t)$ in (19). The admittances $Y_{DT}(s)$ and $Y_{pcc}(s)$ represents the influence of the dead-time and PCC voltages on the grid current as follows

$$Y_{DT}(s) = \frac{i_g(s)}{v_{DT}(s)} = \frac{-G_{LCL}(s)}{1+G_{ci}(s)\,G_{PWM}(s)\,G_{LCL}(s)} \tag{25}$$

$$Y_{pcc}(s) = \frac{i_g(s)}{v_{pcc}(s)} = \frac{G_{FW}(s)G_{LCL}(s)}{1+G_{ci}(s)\,G_{PWM}(s)\,G_{LCL}(s)}. \tag{26}$$

Equations (25) and (26) indicate that $G_{ci}(s)$ in (23) can reject only the fundamental components of $v_{DT}(t)$ and $v_{pcc}(t)$. A feedforward of the PCC voltage optionally improves the dynamic performance and mitigation of the PCC voltage harmonics [22], as given by

$$Y_{pcc}(s) = \frac{i_g(s)}{v_{pcc}(s)} \approx \frac{(G_{FW}(s)-1)\,G_{LCL}(s)}{1+G_{ci}(s)\,G_{PWM}(s)\,G_{LCL}(s)}$$

$$= \frac{\left(\frac{L_1C_fs^2}{C_fR_fs+1}\right)G_{LCL}(s)}{1+G_{ci}(s)\,G_{PWM}(s)\,G_{LCL}(s)}. \tag{27}$$

B. UNIFIED HARMONIC MITIGATION STRUCTURE

Mitigation of the voltage harmonics typically adopts a plugged-in harmonic compensator (HC) $G_{cih}(s)$, of which transfer function in the stationary reference frame is given by

$$G_{cih}(s) = \sum_{h=3}^{n} \frac{K_{ih}s}{s^2+(h\omega)^2} \tag{28}$$

where K_{ih} is the controller gain at the harmonic order h. This HC $G_{cih}(s)$ can be realized from PI controllers in the multiple-synchronous reference frame, proportional-multi-resonant (PMR) regulators, and repetitive controllers, which exhibit sufficient large gains at the selected frequencies. Fig. 6 shows the typical parallel HC structure of the grid current control with a harmonic controller in the stationary reference frame. The outputs m_1^* and m_h^* of the fundamental and harmonic controllers form the modulation signal m^*. Equations (29)-(31) in Table 2 summarize the harmonic responses of this parallel structure. Equation 29 indicates that this structure tracks the harmonic components of the reference current $i_g^*(t)$ at the selected frequencies thanks to the HC's large gains. The large gains of HC attenuate the harmonic components of the PCC and dead-time voltages, as indicated in (30) and (31) [22].

Fig. 7(a) depicts an alternative grid current control structure. This control structure is equivalent to Fig. 7(b), where the reference signal for the selective harmonic controller is zero. The transfer functions of this zero-reference HC structure are summarized in (32)-(34) in Table 2. The large gains of HC at the selected frequencies simultaneously attenuate the harmonic components in $i_g^*(t)$, $v_{DT}(t)$, and $v_{pcc}(t)$. Furthermore, the parallel and zero-reference HC schemes

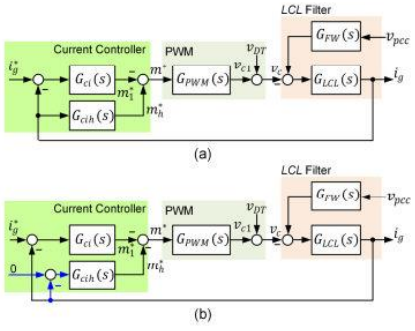

FIGURE 7. (a) Proposed grid current control with zero-reference HC scheme. (b) Equivalence of the grid current control with zero-reference HC scheme.

have identical rejection characteristics of the dead-time and PCC voltages, as indicated in (30) and (33), and (31) and (34). According to (32), the zero-reference HC scheme can increase the bandwidth of the conventional bus voltage control to improve the dynamic response and reduce the bus capacitance without restriction in grid current distortion. On the other hand, the existing bus voltage control schemes only focused on creating a *clean* reference for the grid current control loop.

IV. PROPOSED VSC CONTROL SCHEME

A. UNBALANCED SYNCHRONOUS REFERENCE FRAME CONTROL

The unbalanced synchronous reference frame control [28] is chosen for the fundamental and harmonic component current control. Fig. 8 depicts the stationary frame representation of the transfer function $H_{DC}(s)$ implemented on the synchronous reference frame at $h\omega t$ [31]. The error signals in the stationary reference frame $e_\alpha(t)$ and $e_\beta(t)$ derive from

$$\begin{bmatrix} e_\alpha(t) \\ e_\beta(t) \end{bmatrix} = \begin{bmatrix} x_{\alpha ref}(t) \\ x_{\beta ref}(t) \end{bmatrix} - \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} \tag{35}$$

where $x_\alpha(t)$ and $x_\beta(t)$ are the controlled signals, and $x_{\alpha ref}(t)$ and $x_{\beta ref}(t)$ are the reference signals in the $\alpha\beta-$ axes. The error signals $e_\alpha(t)$ and $e_\beta(t)$ are transformed to the error signals $e_d(t)$ and $e_q(t)$ in the synchronous reference frame using the Park transformation as

$$e_d(t) + je_q(t) = \left(e_\alpha(t) + je_\beta(t)\right) e^{-jh\omega t}. \tag{36}$$

For the single-phase application, the α-component output $y_\alpha(t)$ is only considered. According to [31], the α-component output $y_\alpha(s)$ is derived from the convolution and modulation properties of the Laplace transformation, which yields

$$y_\alpha(s) = \frac{1}{2}\left\{H_{DC}(s+jh\omega) + H_{DC}(s-jh\omega)\right\} e_\alpha(s) - \frac{1}{2}j\left\{H_{DC}(s+jh\omega) - H_{DC}(s-jh\omega)\right\} e_\beta(s). \tag{37}$$

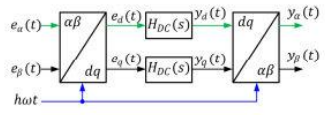

FIGURE 8. Stationary frame representation of the synchronous reference frame control.

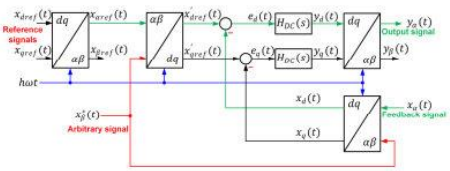

FIGURE 9. Unified structure of the unbalanced synchronous reference frame.

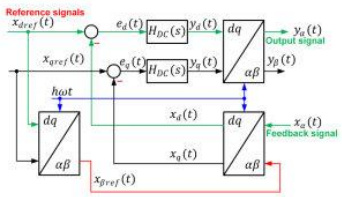

FIGURE 10. Unbalanced synchronous reference frame control with the references in the dq−axes.

Thus, substituting $H_{DC}(s) = K_{ih}/s$ and $e_\beta(t) = 0$ into (37), the equivalent transfer function in the stationary reference frame $H_{AC}(s)$ becomes

$$H_{AC}(s) = \frac{Y_\alpha(s)}{e_\alpha(s)} = \frac{K_{ih}s}{s^2 + (h\omega)^2}. \tag{38}$$

This so-called *unbalanced synchronous reference frame control* is equivalent to the resonant controller [28]. There are different control structures to make the error in the $\beta-$ axis zero $e_\beta(t) = 0$ with identical performance. Fig. 9 depicts the unified structure of the unbalanced synchronous reference control. The arbitrary signal $x^*_\beta(t)$ is used for the Park transformations on the reference and feedback sides, which causes $e_\beta(t) = 0$. Fig. 10 portrays an implementation structure of the unbalanced synchronous reference frame control with the reference signals in the $dq-$ axes, where the reference signal in the $\beta-$ axis $x_{\beta ref}(t)$ is used as the orthogonal signal for the axis transformation of the feedback signal $x_\alpha(t)$. The signal $x_d(t)$ and $x_q(t)$ in Fig. 10 are identical to those of the conventional synchronous reference frame control in the steady state [28]. Meanwhile, Fig. 11 shows another implementation configuration of the unbalanced synchronous reference frame control with $x_{\alpha ref}(t)$ as the reference signal, where $e_\beta(t) = 0$. This structure is suitable for an AC reference signal such as

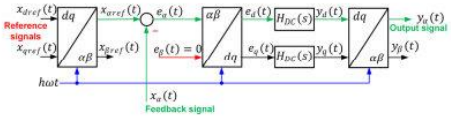

FIGURE 11. Unbalanced synchronous reference frame control with the reference in the $\alpha-$axis.

HCs. It has been proven that the error signals $e_d(t)$ and $e_q(t)$ in Fig. 9 are identical to those in Fig. 10 and Fig. 11, which yields a similar performance [28].

B. PROPOSED BUS VOLTAGE CONTROL SCHEME

The existing bus voltage control methodologies of the single-phase VSC try to create a *clean* reference for the grid current control loop [12], [13], [15], [18], [20], [32]. This study proposes an alternative approach using a conventional bus voltage control system tuned at a fast bandwidth. However, this makes the grid reference current $i_g^*(t)$ distorted. So instead, we employ the current control with zero-reference HC scheme in Fig. 7(a) as the main mechanism for simultaneous attenuation of the harmonic components in the grid reference current $i_g^*(t)$, PCC voltage $v_{pcc}(t)$, and VSC's dead-time voltage $v_{DT}(t)$.

Fig. 12 shows the proposed bus voltage control scheme of the VSC. The bus voltage control loop applies a conventional PI regulator. The bus voltage passes through the low-pass filter $G_{fv}(s)$ given by

$$G_{fv}(s) = \frac{1}{T_f s + 1}. \tag{39}$$

Note that $G_{fv}(s)$ is used for loop shaping, not for attenuating the ripple component, which is explained in the controller design. The fundamental current control system $G_{ci}(s)$ adopts the unbalanced synchronous reference frame with the reference current in the β-axis $i_\beta^*(t)$ as the orthogonal signal for the Park transformation, which is simplified from Fig. 10. This configuration results in the virtual β-axis current error signal $e_{i\beta}(t) = 0$. According to (37), the equivalent transfer function of the fundamental current control loop in the stationary reference frame is identical to (23). Moreover, this unbalanced synchronous reference frame control configuration has intrinsic frequency adaptation and power extraction capabilities.

The harmonic current controller $G_{cih}(s)$ is plugged into the fundamental current control $G_{ci}(s)$. This current control structure is equivalent to Fig. 7(a). Fig. 13 illustrates the implementation of $G_{cih}(s)$, where each harmonic component is simplified from the unbalanced synchronous reference frame control in Fig. 11. The transfer function of each harmonic order is equivalent to (28). Therefore, the proposed fundamental and harmonic current controllers in Fig. 12 are equivalent to the stationary reference frame current control system in Fig. 7(a). Note that this configuration of $G_{cih}(s)$ also exhibits inherent frequency adaptability. The

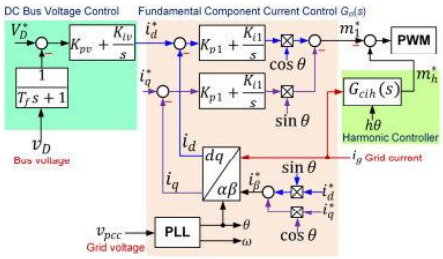

FIGURE 12. Proposed DC bus voltage control system with unified current harmonic mitigation.

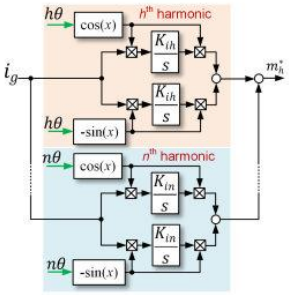

FIGURE 13. Harmonic controller $G_{cih}(s)$ in the unbalanced synchronous reference frame.

harmonic controllers, orders 3rd, 5th, 7th, 9th, 11th, and 13th were adopted. The second-order harmonic controller was also added to suppress the 2ω component of $i_g^*(t)$ caused by the DC component of the grid current as demonstrated in (19). Furthermore, multiple-resonant regulators with frequency adaptation can be employed as the harmonic controller to reduce the computational effort [22]. The inverse Park transformation PLL is used in this study [33].

The proposed control scheme is compared with the conventional control scheme as shown in Fig. 14 and the notch filter-based control as shown in Fig. 15, where only the fundamental component controller is adopted for the grid current control. Meanwhile, for the notch filter-based control scheme, the low-pass filter is replaced by the notch filter $G_{NF}(s)$ given by

$$G_{NF}(s) = \frac{s^2 + 4\omega^2}{s^2 + 2\omega_d s + 4\omega^2} \tag{40}$$

where ω_d is the damping frequency. This notch filter blocks the 2ω component of the bus voltage.

V. CONTROLLER DESIGN AND HARMONIC REJECTION ANALYSIS

A. GRID CURRENT CONTROLLER DESIGN

The *LCL* filter with the parameters listed in Table 1 has a resonant frequency f_r of 5.03 kHz, and the control system operates

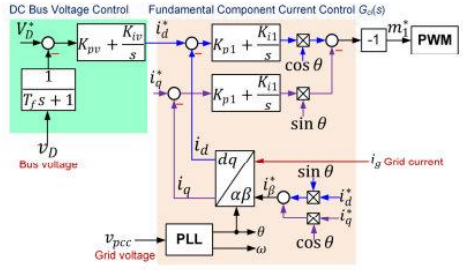

FIGURE 14. Conventional bus voltage control of the single-phase grid-connected VSC.

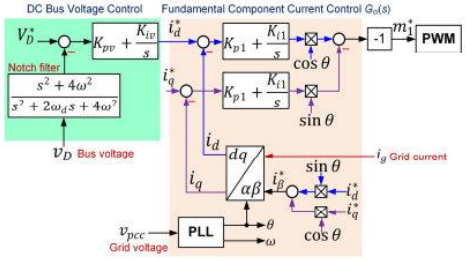

FIGURE 15. Notch filter-based bus voltage control of the single-phase grid-connected VSC.

at the sampling frequency of $f_s = 20$ kHz. This resonant frequency f_r satisfies the stability criterion of $f_s/6 < f_r < f_s/2$ for the grid current feedback [34]. First, the fundamental component current controller is designed in the stationary reference frame. The loop bandwidth must be chosen to be lower than f_r. The LCL filter can be simplified at such a frequency range as an L filter with $L_t = L_1 + L_2$ and $R_t = R_1 + R_2$ [35]. The stationary reference frame equivalence of the open-loop grid current control system is given by

$$G_{oi}(s) = \underbrace{K_{p1}\left(1 + \frac{K_{i1}}{K_{p1}} \cdot \frac{s}{s^2+\omega^2}\right)}_{Current\,controller} \underbrace{V_D e^{-sT_d}}_{PWM} \underbrace{\frac{1}{S_L + R_t}}_{LCL\,filter}. \tag{41}$$

The maximum cross-over frequency $\omega_{ci,max}$ is obtained from [30]

$$\omega_{ci,max} = \frac{\pi/2 - \phi_{mi}}{T_d} \tag{42}$$

where ϕ_{mi} is the chosen phase margin. This $\omega_{ci,max}$ leads to K_{p1} approximated as

$$K_{p1} = \frac{\omega_{c,max} L_t}{V_D}. \tag{43}$$

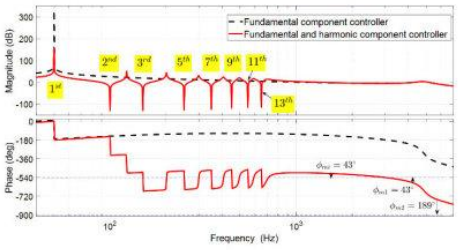

FIGURE 16. Open-loop frequency response of the grid current control systems.

The value of K_{i1} is then determined from

$$K_{i1} = \frac{\omega_{c,max}}{10 K_{p1}} \tag{44}$$

at which $\tan^{-1}\left(\omega_{ci,max} K_{p1}/K_{i1}\right) = 85°$. A conservative phase margin of $\phi_{mi} = 60°$ was selected. With the parameters in Table 1 and $T_d = 2T_s$, K_{p1} and K_{i1} were calculated from (43) and (44) with $\omega_{ci,max} = 2,222\pi$ rad/s. The integral gains K_{ih} of the harmonic controller should be selected lower or equal to (44) to create the corresponding negligible magnitude contributions at the cross-over frequency [27]. Thus, the integral gains were set as follows

$$\left.\begin{aligned} K_{i2} = K_{i3} = K_{i5} = K_{i7} = \tfrac{K_{i1}}{3} \\ K_{i9} = K_{i11} = K_{i13} = \tfrac{K_{i1}}{5} \end{aligned}\right\}. \tag{45}$$

With this set of harmonic gains, the phase margin reduces to $\phi_{mi} = 43°$ at the chosen cross-over frequency ω_{ci}, still large enough to guarantee stability, as shown in Fig. 16. The open-loop gains at the selected frequencies are lower than -100 dB, which attenuates the current error signal at such frequencies. Although the harmonic controller decreases the first harmonic gain, it is still large enough to track the fundamental component current with a zero steady-state error. The open-loop system has multiple gain cross-over frequencies with the harmonic controller at the selected frequencies. However, the system stability is measured at the highest gain cross-over frequency [36]. Moreover, the two gain cross-over frequencies around the resonant frequency of the LCL filter with the phase margins $\phi_{m1} = 43°$ and $\phi_{m2} = 189°$ shown in Fig. 16 guarantee the stability criteria for the grid current feedback.

B. BUS VOLTAGE CONTROLLER DESIGN

Fig. 17 depicts the block diagram of the bus voltage control, simplified from Fig. 4. The grid current control loop is approximated as a unity gain, and the grid oscillating powers $\tilde{p}_{g1}(t)$ and $\tilde{p}_0(t)$ are considered the disturbances. The extended symmetrical optimum method [37] is adopted, which is proven to have a better transient response and lower grid current distortion [38] than the method in [2]. With this tuning method, the phase angle of the forward path reaches

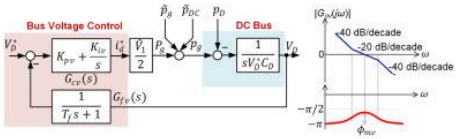

FIGURE 17. Equivalent bus voltage control block diagram and its open-loop frequency response.

the maximum at the cross-over frequency ω_{cv}. The phase margin ϕ_{mv} is chosen from a constant β as

$$\phi_{mv} = tan^{-1}\left(\frac{\beta - 1}{2\beta^{1/2}}\right). \tag{46}$$

The recommended values of β are from 4 to 16, which relates to ϕ_{mv} of 36° to 60°. The PI controller parameters K_{pv} and K_{iv} and the low-pass filter time constant T_f are co-designed from the desired bandwidth ω_{bv} as follows

$$\left.\begin{aligned} T_f &= \left(\sqrt{\beta}\omega_{cv}\right)^{-1} \\ K_{iv} &= \frac{\omega_{cv}^2}{\sqrt{\beta}}\left(\frac{2V_D^* C_D}{\hat{V}_1}\right) \\ K_{pv} &= \omega_{cv}\left(\frac{2V_D^* C_D}{\hat{V}_1}\right) \end{aligned}\right\}. \tag{47}$$

The parameters obtained from (47) yield the closed-loop transfer function given by

$$\frac{V_D(s)}{V_D^*(s)} = \frac{\beta^{1/2}s/\omega_{cv} + 1}{s^3/\omega_{cv}^3 + \beta^{1/2}s^2/\omega_{cv}^2 + \beta^{1/2}s/\omega_{cv} + 1}. \tag{48}$$

The bus voltage control loop was designed at $\omega_{cv} = 50\pi$ rad/s and $\beta = 5.83$ with $\phi_{mv} = 45^\circ$. This study compares the proposed control method with the conventional bus voltage control in Fig. 14 with $\omega_{cv} = 20\pi$ rad/s and $\omega_{cv} = 50\pi$ rad/s. The notch filter in Fig. 15 is simplified as the low-pass filter with $T_f = \omega_d/(2\omega^2)$ so that so that the above design method of the bus voltage control can be adopted. The notch filter $G_{NF}(s)$ tuned at 2ω with $\omega_d = 140\pi$ rad/s has a frequency response below 2ω close to a low-pass filter for $\omega_{cv} = 50\pi$ rad/s. Thus, K_{pv} and K_{iv} for the notch filter-based control can be adopted from the conventional control with $\omega_{cv} = 50\pi$ rad/s.

C. HARMONIC REJECTION ANALYSIS

Fig. 18 shows the closed-loop frequency response of the grid current control with the reference current plotted from (32). The closed-loop grid current system exhibits a unity gain with a zero-phase angle at the grid frequency, which provides a zero steady-state error. Meanwhile, the harmonic controller rejects the reference current at the selected frequencies. Fig. 19 illustrates the frequency responses of the admittances $Y_{DT}(j\omega)$ in (33) and $Y_{pcc}(j\omega)$ in (34). The proposed grid current control scheme with the harmonic controller $G_{cih}(s)$ rejects the disturbances from the dead-time voltage v_{DT} and grid voltage v_{pcc} at the fundamental and selected harmonic frequencies. On the other hand, the harmonic components of

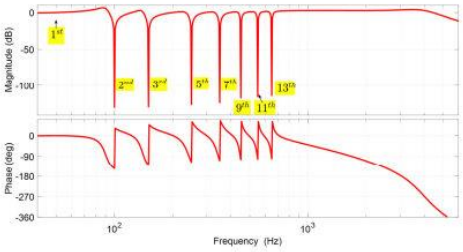

FIGURE 18. Frequency response OF the grid current to the reference current $G_d(j\omega)$ in (33).

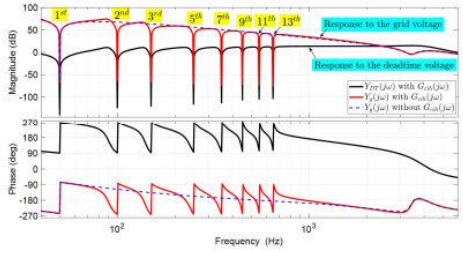

FIGURE 19. Frequency response of the grid current to the deadtime voltage $Y_{DT}(j\omega)$ in (34) the grid voltage $Y_{pcc}(j\omega)$ in (35).

the grid voltage are even amplified if the fundamental current controller is only adopted.

VI. SIMULATION

A switched-circuit model of the VSC was developed in MATLAB/Simulink. Voltage harmonic orders 3rd of 5%, order 5th of 2%, and orders 7th, 9th, 11th 13th of 1% to the fundamental component of the PCC voltage were added. The added harmonics resulted in a total harmonic distortion (THD) of 5.74%. The dead-time voltage $v_{DT}(t)$ determined from (7) with $T_{DT} = 4\mu$s was added to the VSC terminal voltage $v_c(t)$. The bus voltage control loop was tuned at a bandwidth of 50π rad/s with a PLL bandwidth of 20π rad/s. The VSC was simulated to operate in mode with the nominal bus power of $P_D = 2$ kW and $i_q^* = 0$ for a unity power factor.

Fig. 20 compares the steady state performance of the conventional control and the proposed control schemes under the sinusoidal PCC voltage in Fig. 20(a), the sinusoidal PCC voltage and the dead-time voltage in Fig. 20(b), the distorted PCC voltage in Fig. 20(c), and the distorted PCC and dead-time voltages in Fig. 20(d). The conventional control scheme's grid current $i_g(t)$ under the sinusoidal PCC alone still distorts. Meanwhile, the proposed control method with HC rejects the harmonic contents in the reference current $i_g^*(t)$, as shown in Fig. 20(a). As a result, the disported PCC and dead-time voltages heavily affect the grid current waveform with the conventional control scheme, as depicted in Fig. 20(b) to

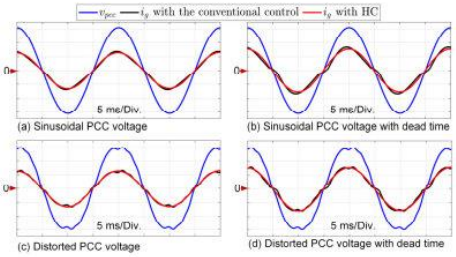

FIGURE 20. Simulation results of the VSC in the rectifier mode supplying the bus power of 2 kW ($v_{pcc}(t)$: 100 V/division, $i_g(t)$: 10 A/division): (a) Sinusoidal PCC voltage, (b) Sinusoidal PCC with the dead-time voltages, (c) Distorted PCC voltage, (d) Distorted PCC with the dead-time voltages.

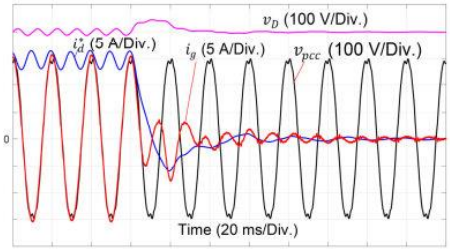

FIGURE 21. Simulation results of the VSC with the proposed bus voltage control in the rectifier mode when the bus power changes from 2 kW to zero under the PCC voltage distortion and dead-time voltages.

Fig. 20(d). On the other hand, the proposed control method with HC forces the grid current to be near sinusoidal with the simultaneous presence of the dead-time voltage and PCC harmonic voltage $v_h(t)$.

Fig. 21 depicts the transient response of the proposed bus voltage control system under the distorted grid voltage and dead-time voltage $v_{DT}(t)$. The DC bus initially supplies a power of $P_D = 2$ kW. Although there is a 2ω ripple component in the reference current $i_d^*(t)$, the grid current $i_g(t)$ remains sinusoidal similar to that in Fig. 20. At $t = 0.2$ s, P_D is removed, which behaves as a step load change. The bus voltage $v_D(t)$ increases by approximately 50 V and recovers to $V_D^* = 400$ V within 50 ms.

VII. EXPERIMENTAL VALIDATION

A. EXPERIMENTAL SETUP

Fig. 22 illustrates the experimental setup of this study. The VSC and DAB DC-DC converter were assembled from Infineon FF50R12RT4 insulated-gate bipolar transistor (IGBT) modules with the control schemes implemented on a 32-bit TMS320F28379D microcontroller. Dead times of $T_{DT} = 1\mu$s and $T_{DT} = 4\mu$s in each VSC leg were adjusted on the

FIGURE 22. Experimental setup of the VSC.

microcontroller's PWM outputs. A Chroma 61860 60-kVA grid simulator emulated the PCC voltage. The DC output voltage V_B for the DAB DC-DC converter was set at a constant voltage of 400 V using a Chroma 17020 bidirectional DC source. The output power was controlled in the range of ± 2 kW through the angle δ^* of the single phase-shift modulation implemented on the same microcontroller. The q-axis reference current was set at $i_q^* = 0$ for a unity power factor.

B. EXPERIMENTAL RESULTS

Fig. 23 shows the transient response of the $v_D(t)$ and $i_g(t)$ under the distorted PCC voltage and $T_{DT} = 1\ \mu$s when the output power changes from 2 kW to zero. The reference current $i_d^*(t)$ in the discrete-time control system was sent to an embedded 12-bit digital to analog converter of the microcontroller with appropriate scaling. The proposed bus voltage control system compares the conventional control schemes tuned at $\omega_{cv} = 20\pi$ rad/s and $\omega_{cv} = 50\pi$ rad/s and the notch filter-based control system tuned at $\omega_{cv} = 50\pi$ rad/s. The proposed control, 50π-rad/s conventional and notch filter-based control schemes, have voltage fluctuations of approximately 50 V and recover to the 400-V reference within two cycles. The experimental transient response agrees with the simulation result in Fig. 21. However, the 20π-rad/s conventional control gives rise to $v_D(t)$ to 540 V. It takes ten cycles to go back to the 400-V reference, which temporarily forces the grid current control into the unstable range. Thus, the bus capacitance C_D should be increased for this 20π-rad/s conventional control scheme.

Fig. 24 compares the steady-state waveforms of $v_{pcc}(t)$, $v_D(t)$, $i_g(t)$ and $i_d^*(t)$ of different control schemes when the VSC operates in the rectifier mode with the output power of 2 kW under the sinusoidal PCC voltage and $T_{DT} = 1\ \mu$s. Although the reference current $i_d^*(t)$ of the proposed control system contains ripple components, the grid current waveform is still near sinusoidal. Meanwhile, $i_g(t)$ under the 50π-rad/s conventional control scheme under the sinusoidal voltage is slightly distorted due to the ripple component of $i_d^*(t)$. The 20π-rad/s conventional and notch filter-based control systems under the sinusoidal voltage create the clean reference current $i_d^*(t)$, which also results in near sinusoidal grid currents.

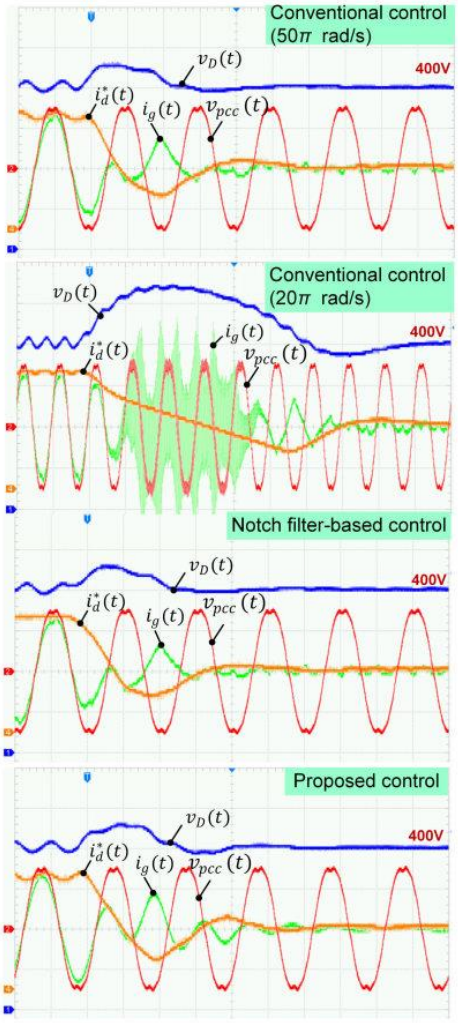

FIGURE 23. Transient response of the VSC when the output power changing from 2 kW to zero under the distorted PCC voltage and T_{DT} = 1 μs (v_{pcc}(t) and v_D(t): 100 V/division, i_g(t) and i_d^*(t): 10 A/division).

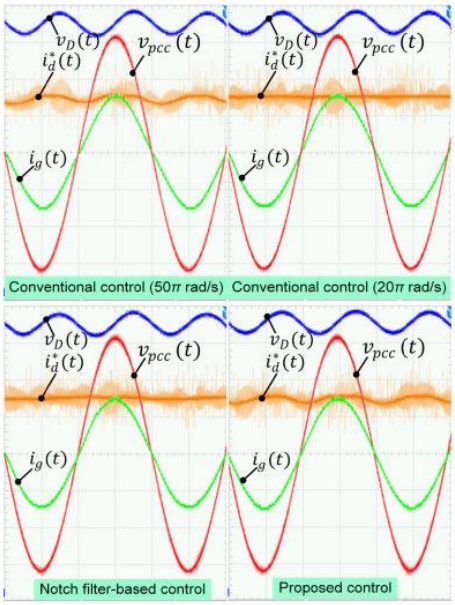

FIGURE 24. Steady state waveforms of the VSC with the output power of 2 kW under the sinusoidal PCC voltage and T_{DT}=1 μs, (v_g(t) and v_D(t): 100 V/division, i_g(t) and i_d^*(t): 10 A/division).

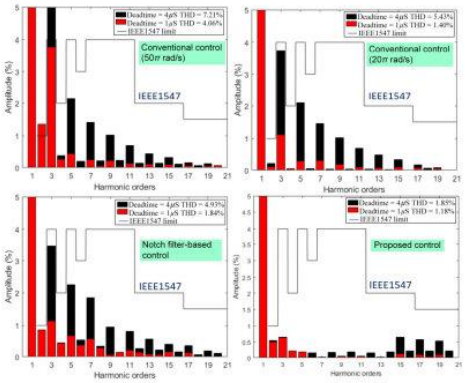

FIGURE 25. Harmonic components of the VSC current with the output power of 2 kW under the sinusoidal PCC voltage with T_{DT}=1 μs, and T_{DT}=4 μs).

Fig. 25 compares the resultant harmonic components of the grid current under the sinusoidal PCC voltage with T_{DT} =1 μs and T_{DT} = 4 μs. The proposed bus voltage system effectively mitigates the grid current harmonics caused by the large dead time T_{DT} =4 μs with THD_i = 1.85% compared with THD_i = 1.18% for the short dead time T_{DT} =1 μs. The current harmonics components under the two dead-time values are within the IEEE1547 standard. Although the 20π-rad/s conventional and notch filter-based control systems regulate the grid current with THD_i = 1.40%

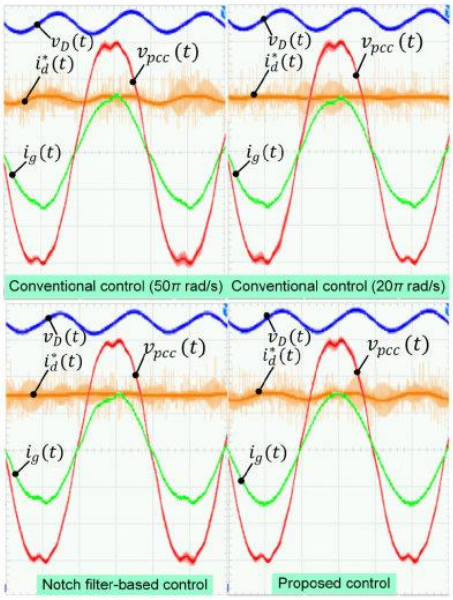

FIGURE 26. Steady state waveforms of the VSC with the output power of 2 kW under the sinusoidal PCC voltage and T_{DT}=1 μs, (v_g(t) and v_D(t): 100 V/division, i_g(t) and i_d^*(t): 10 A/division).

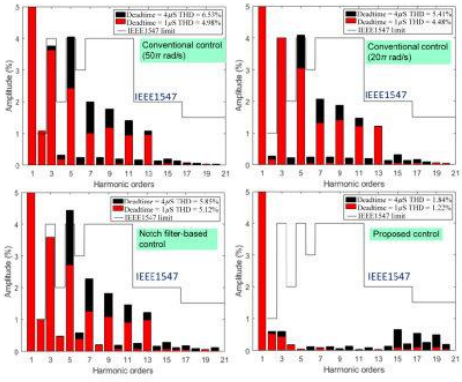

FIGURE 27. Harmonic components of the VSC current with the output power of 2 kW under the distorted grid voltage with T_{DT}=1 μs, and T_{DT}=4 μs.

and $\text{THD}_i = 1.84\%$, for $T_{DT} = 1\ \mu$s, the two control schemes are affected by the dead-time voltage harmonics with the THD_iapproximately of 5% for $T_{DT} = 4\ \mu$s. A large loop bandwidth does not attenuate the ω component in $v_D(t)$

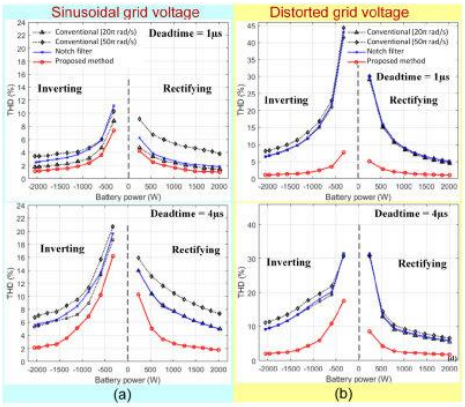

FIGURE 28. THD_i values of the grid current with the output power under: (a) sinusoidal PCC voltage, and (b) distorted PCC voltage.

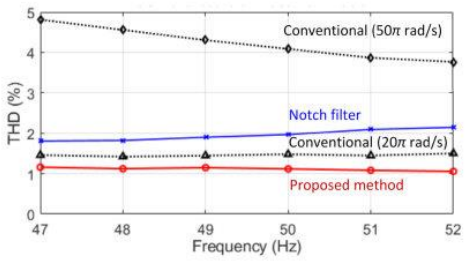

FIGURE 29. THD_i values of the grid current under sinusoidal PCC voltage and T_{DT} =1 μs at the output power of 2 kW with varied grid frequency.

caused by the DC component of $i_g(t)$. Therefore, the 2nd harmonic component of the grid current is noticeable for the 50π-rad/s conventional and notch filter-based control systems compared with the 20π-rad/s conventional system. Meanwhile, the harmonic controller $G_{cih}(s)$ of the proposed control scheme successfully damps the 2nd harmonic current.

For the distorted PCC voltage and the sizeable dead time T_{DT} =4 μs in Fig. 26, grid current distortion can be observed with the conventional and notch filter-based control schemes. The dead time mainly distorts $i_g(t)$ during the zero crossings [21]. The distortion due to the PCC voltage harmonics can be observed during the peaks of the current waveform. The harmonic controller $G_{cih}(s)$ of the proposed control scheme mitigates the harmonic disturbances due to the dead-time effect and PCC voltage. The grid current harmonics with the proposed control system under the distorted PCC voltage in Fig. 27 are very close to those under the sinusoidal voltage in Fig. 25, which confirms the effectiveness of the

TABLE 3. Performance comparison of the proposed control schemes with the existing methods.

Control schemes	Distorted PCC voltage	Large dead time	Fast bus voltage control	Frequency adaptation	Power extraction	2nd harmonic current
Dead-time compensations [24, 25]	×	✓	×	✓	×	×
PCC voltage feedforward [22]	✓	×	×	✓	×	×
Fundamental component + paralleled HC current control [21, 22, 27]	✓	✓	×	✓ only for [22]	✓ only for [22]	×
Conventional bus voltage control and fundamental component current control [2, 11]	×	×	×	×	×	×
Notch filter-based bus voltage control and fundamental component current control [1, 12-15]	×	×	✓	✓ only for [1, 13]	✓ only for [1, 13]	×
Advanced bus voltage control and fundamental component current control [16-20]	×	×	✓	✓ only for [17, 18]	✓ only for [17, 18]	×
Conventional bus voltage control and fundamental component + paralleled HC current control [26]	✓	✓	×	✓	✓	×
DC current mitigation method [23]	×	×	×	×	×	✓
Proposed method in this study	✓	✓	✓	✓	✓	✓

proposed harmonic mitigation structure. Meanwhile, the distorted PCC voltage adversely affects the grid current waveforms under the conventional and notch filter-based control schemes.

Fig. 28 compares the THD_i values under the sinusoidal and distorted PCC voltages and the dead times of $T_{DT} = 1\ \mu s$ and $T_{DT} = 4\ \mu s$ with the output power of ± 2 kW. The proposed bus control system exhibits the lowest THD_i values. The difference is highly noticeable with PCC voltage harmonics and a significant dead time. Fig. 29 compares the current distortion under the sinusoidal voltage and $T_{DT} = 1\ \mu s$ with the output power of 2 kW with the allowable frequency between 47-52 Hz for Thailand's grid. The proposed control system has inherent frequency adaptation. The detuned notch frequency causes THD_i to vary with the grid frequency. The conventional control scheme with a bandwidth of 20π rad/s, far below 2ω, virtually has no impact on the grid frequency variation compared with the 50π-rad/s bandwidth.

Table 3 compares the performance of the proposed bus voltage control scheme with the existing VSC control methods. The power extraction in the table refers to the decomposition capability of the grid current. It indicates that the proposed methodology covers all the performance criteria, which has advantages over the existing methods.

VIII. CONCLUSION

Grid current control with selective harmonic mitigation is proposed for bus voltage control of the single-phase grid-connected VSC. Zero-reference current configuration of the harmonic controller rejects harmonic components in the grid reference current, VSC dead-time harmonics, and PCC voltage harmonics. Thus, a conventional bus voltage control with the proposed selective harmonic mitigation structure tuned at a fast bandwidth minimizes the bus capacitance without sacrificing the grid current quality. The proposed control scheme implemented in the unbalanced synchronous reference frame has superiority over the low-bandwidth conventional and notch filter-based control schemes as follows

1) Simultaneous rejection of harmonic components in the reference current, dead-time voltage, and grid voltage at the selected frequencies.
2) Second harmonic mitigation due to a DC component in the grid current.
3) Inherent frequency adaptation through the axis transformation.

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Article

Design and Implementation of Single-Phase Grid-Connected Low-Voltage Battery Inverter for Residential Applications

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Abstract: Integrating residential energy storage and solar photovoltaic power generation into low-voltage distribution networks is a pathway to energy self-sufficiency. This paper elaborates on designing and implementing a 3 kW single-phase grid-connected battery inverter to integrate a 51.2-V lithium iron phosphate battery pack with a 220 V 50 Hz grid. The prototyped inverter consists of an *LCL*-filtered voltage source converter (VSC) and a dual active bridge (DAB) DC-DC converter, both operated at a switching frequency of 20 kHz. The VSC adopted a fast DC bus voltage control strategy with a unified current harmonic mitigation. Meanwhile, the DAB DC-DC converter employed a proportional-integral regulator to control the average battery current with a dynamic DC offset mitigation of the medium-frequency transformer's currents embedded in the single-phase shift modulation scheme. The control schemes of the two converters were implemented on a 32-bit TMS320F280049C microcontroller in the same interrupt service routine. This work presents a synchronization technique between the switching signal generation of the two converters and the sampling of analog signals for the control system. The prototyped inverter had an efficiency better than 90% and a total harmonic distortion in the grid current smaller than 1.5% at the battery power of ±1.5 kW.

Keywords: battery storage; DC-DC converter; grid-connected inverter; solar photovoltaic

Citation: Pannawan, A.; Kaewchum, T.; Saeseiw, C.; Pachanapan, P.; Hinkkanen, M.; Somkun, S. Design and Implementation of Single-Phase Grid-Connected Low-Voltage Battery Inverter for Residential Applications. *Electronics* **2024**, *13*, 1014. https://doi.org/10.3390/electronics13061014

Academic Editors: Amedeo Andreotti and Bianca Caiazzo

Received: 8 February 2024
Revised: 1 March 2024
Accepted: 5 March 2024
Published: 7 March 2024

1. Introduction

Reduction of CO_2 emissions has been driving shares of renewable energy in electricity generation systems. Solar photovoltaic (PV) technology has been the fastest-growing renewable energy technology since it can be adopted in small-scale to large-scale power generation systems [1]. Grid-connected PV rooftop systems are commonly installed in the residential sector. However, the excess power from the residential PV rooftop systems poses power quality problems for low-voltage (LV) distribution networks. Voltage violation due to the outfeed of PV power is the most common issue for the LV grid [2]. Extensive upgrades of LV distribution networks for supporting solar PV rooftop systems require a large amount of capital investment. Battery storage is an enabling technology for further deployment of variable renewable energy (VRE) technology. Moreover, integrating battery storage with LV grids reduces transmission congestion, improves power quality, and delays investment in upgrading existing networks [3,4].

Solar PV and battery storage integration into LV distribution networks can be implemented in various topologies. Battery storage can be connected to solar PVs on the DC side of the grid inverter, as depicted in Figure 1. These topologies are so-called DC coupling solar PV-battery hybrid inverters. The DC bus voltage is usually greater than the PV voltage, so non-isolated boost DC-DC converters interface the PV strings with the

DC bus voltage. Maximum power point tracking (MPPT) is embedded with the control system of the boost DC-DC converter [5,6]. A high voltage (HV) battery pack can be directly connected to the DC bus of the grid inverter, as shown in Figure 1a [7]. The battery voltage must be greater than the minimum requirement of the grid inverter, i.e., the peak value of the grid voltage for a single-phase system, and the peak value of the line-line voltage of a three-phase system. An HV battery pack can be connected to the DC bus via a non-isolated DC-DC converter, as shown in Figure 1b. Typically, a bidirectional buck-boost DC-DC converter allows a wide battery voltage range (200–500 V). Meanwhile, the DC bus voltage is regulated above the minimum requirement of the grid-interfaced inverter. A battery back requires an electronic battery management system (BMS) for voltage balancing, management, and protection of the galvanic cells [8]. Thus, HV battery storage with complex BMS may only be viable for some residential systems. Low-voltage battery storage (less than 100 V) with a less complicated and cheaper BMS can be a suitable option for a small household (less than 5 kW), as illustrated in Figure 1c [7]. The LV battery pack is interfaced with the DC bus through a bidirectional isolated DC-DC converter, which employs a medium frequency (MF) (20–150 kHz) transformer for voltage matching the LV battery pack with the DC bus [9,10]. Battery storage can be integrated with the LV network by the AC coupling topologies shown in Figure 2. A grid-interfaced inverter is dedicated to the battery systems of the DC coupling topologies in Figure 1. PV power P_{PV}, battery power P_{Batt}, load power P_L, and grid power P_g are exchanged at the AC point of common coupling (PCC). The AC coupling topologies have a lower efficiency than the DC coupling systems due to an increased conversion stage [11]. However, the AC coupling systems can be employed with existing grid-connected PV inverters or without any PV inverter for energy arbitrage or peak load shaving [7]. AC-coupled two-stage LV battery inverters depicted in Figure 2c are common for small residential applications with a power lower than 5 kW. The power conversion stages can be integrated with the battery pack into a single package [12,13].

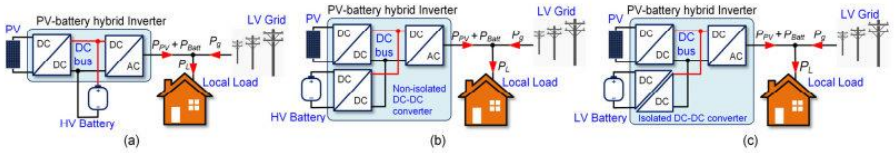

Figure 1. DC coupling grid-connected PV-battery hybrid inverters: (**a**) direct connection of the HV battery to the DC bus; (**b**) HV battery connected to the DC bus via a non-isolated DC-DC converter; (**c**) LV battery connected to the DC bus via an isolated DC-DC converter.

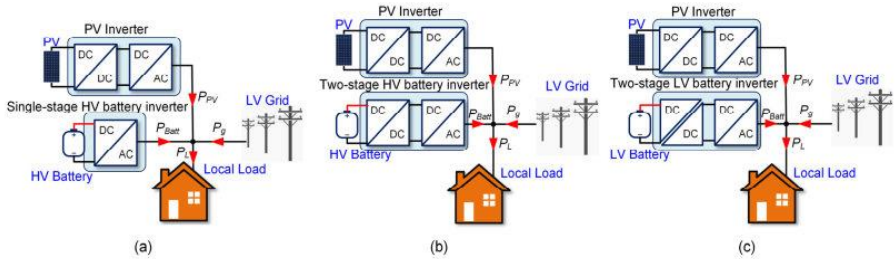

Figure 2. AC coupling grid-connected PV-battery hybrid inverters: (**a**) single-stage HV battery inverter; (**b**) two-stage HV battery inverter; (**c**) two-stage LV battery inverter.

This study focuses on a two-stage single-phase grid-connected LV battery inverter for small residential applications. A dual-active bridge DC-DC converter with phase-shift

modulation strategies is generally employed as the bidirectional isolated DC-DC converter for the LV battery pack. Meanwhile, *LCL*-filtered grid-connected voltage source converters (VSCs) are commonly adopted as the grid-interfaced inverter. However, a limited zero-voltage switching (ZVS) range of the DAB DC-DC converter causes a low efficiency if the voltage ratio between the sides deviates from the nominal value [14]. The efficiency of the DAB DC-DC converter can be enhanced by adding resonant networks to the MF transformer to increase the ZVS range [15,16]. However, power transfer of the resonant DAB DC-DC converter can be controlled by variation of the switching frequency, which is more complicated compared to the fixed frequency operation of the conventional DAB DC-DC converter. The DAB DC-DC converter is sensitive to an imbalance in the voltage-second applied to the MF transformer, which causes a DC offset in the transformer current [17]. The primary and secondary currents of the transformer were sampled 10 times over a switching period to determine the DC offset component, from which the DC offset was compensated through the duty ratios applied to the two active bridges. This method can attenuate the dynamic and static DC offset components [18]. For simplicity, the dynamic DC offset compensation can be embedded into the modulation scheme, where the phase angle of each leg of the DAB DC-DC converter is independently controlled [19,20]. These dynamic DC offset compensation methods require only delay elements.

The bus voltage is controlled through the VSC. The intrinsic double-frequency ripple component in the bus voltage can distort the grid current waveform [21]. A notch filter is usually employed to block the double-frequency ripple component to enter the bus voltage control loop so that the loop bandwidth can be increased with reduced bus capacitance and a near sinusoidal grid current waveform [22,23]. However, low-frequency harmonic components in the grid voltage and VSC terminal caused by the dead time effect can still distort the grid current waveform [24]. Recently, a unified current harmonic mitigation was adopted in a grid-connected VSC [24], which maintained the grid current near sinusoidal with a fast bus voltage control and rejection of voltage harmonic components in the grid and non-ideal switching of the VSC [24].

As mentioned above, the control techniques of the DAB DC-DC converter and grid-connected VSC have been widely presented. However, microcontroller-based implementation techniques of the two converters, with the generation of switching signals and interrupt request and analog signal sampling, have yet to be reported. Thus, this study covers the design and implementation of a single-phase grid-connected low-voltage battery inverter. The battery inverter consists of a DAB DC-DC converter and an *LCL*-filtered VSC thanks to their constant switching frequency application, which eases the implementation of the control system. The control systems of the two converters were implemented in the same microcontroller within the same interrupt service routine (ISR). Synchronous operations of the switching signal generation for the VSC and DAB DC-DC converter and sampling analog signals are highlighted. This work also presents a battery current control strategy with a dynamic DC offset mitigation of the MF transformer. Experimental validation of the proposed inverter is presented.

2. System Description

The main objective of this study is to design a 3 kW bidirectional inverter for interfacing a 16-cell lithium iron phosphate (LFP) battery pack with a single-phase 220 V 50 Hz grid for residential energy storage applications. Figure 3 shows the inverter topology in this study. The grid voltage $v_g(t)$ is converted to a 400 V DC voltage $v_D(t)$ through an *LCL*-filtered VSC. A DAB DC-DC converter well suits the second-stage battery converter as the voltage matching and galvanic isolation are achieved via the MF transformer. Moreover, if properly designed, the DAB DC-DC converter exhibits high efficiency thanks to the ZVS operation [14]. The VSC adopts the cascade control structure with the bus voltage control as the outer loop and the grid current control as the inner loop. The VSC can inject reactive power through the reference current $i_q^*(t)$ for grid support functionality. The inverse Park transformation phase-locked loop (PLL) [25] provides the estimated angle θ of

the grid voltage for synchronization with the grid. The battery current $i_B(t)$ is regulated by a proportional-integral (PI) controller with the reference phase difference δ^* between the primary and secondary voltages $v_p(t)$ and $v_s(t)$ of the transformer, which are generated by the LV and HV bridges with the single-phase shift (SPS) modulation. The DC offset mitigation technique for the transformer currents $i_p(t)$ and $i_s(t)$ is implemented with the SPS modulation. The series inductor L_a limits the maximum charge/discharge current [20]. The VSC and the DAB DC-DC converter's control systems and switching signal generation are implemented on a TMS320F280049C 32-bit microcontroller from Texas Instruments (Dallas, TX, USA) [26]. Table 1 summarizes the main specifications of the battery inverter. Note that the winding resistance symbols R_1, R_a, and R_g of the inductors L_1, L_a, and L_g are not illustrated in Figure 1 for simplicity. Table 2 lists the parameters of the battery inverter.

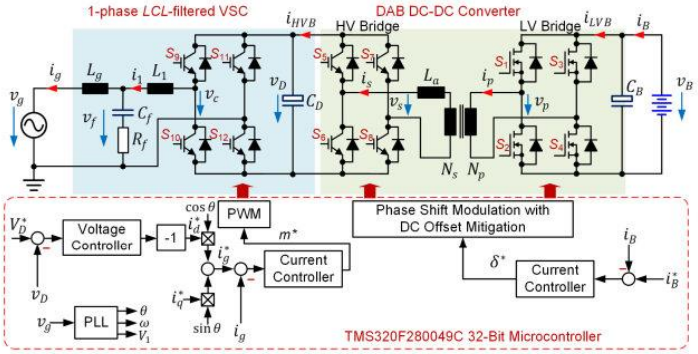

Figure 3. Circuit diagram and its simplified control system of the inverter in this study.

Table 1. Specification of the battery inverter.

Parameters	Value
Maximum grid power	3 kW
Nominal grid voltage	220 Vrms
DC bus voltage	400 V
Nominal grid frequency	50 Hz
Battery nominal voltage, V_{Bn}	51.2 V
Battery voltage range	40–60 V
Maximum battery current	60 A

Table 2. Parameters of the battery inverter.

Parameters	Value
Inductor L_1	0.8 mH
Winding resistance R_1 of L_1	0.07 Ω
Inductor L_2	0.4 mH
Winding resistance R_2 of L_2	0.06 Ω
Filter capacitor C_f	2 µF
Damping resistor R_f	1.1 Ω
DC bus capacitor C_D	800 µF
Series inductor L_a	230 µH
MF transformer's turn ratio N_s/N_p	7.81
Battery-side capacitor C_B	9.9 mF
Switching frequency f_{sw}	20 kHz
Control sampling frequency f_s	20 kHz

3. Implementation of the Grid-Connected VSC

3.1. VSC Modeling

The grid current $i_g(t)$ and bus voltage $v_D(t)$ of the VSC are the controlled variables. Averaging over a switching period T_{sw} yields the governing equations for $i_g(t)$ as follows:

$$L_2\frac{di_g(t)}{dt} + R_2 i_g(t) = v_f(t) - v_g(t)) \tag{1}$$

$$v_f(t) = v_{cf}(t) + R_f\big(i_1(t) - i_g(t)\big) \tag{2}$$

$$C_f\frac{dv_{cf}(t)}{dt} = i_1(t) - i_g(t) \tag{3}$$

$$L_1\frac{di_1(t)}{dt} + R_1 i_1(t) = v_c(t) - v_f(t) \tag{4}$$

$$v_c(t) = \underbrace{(d_1(t) - d_2(t))}_{m(t)} v_D(t) \tag{5}$$

where $v_c(t)$ is the VSC terminal voltage, $d_1(t)$ and $d_2(t)$ are the duty ratios of S_9 and S_{11} ranging from zero to unity, and $m(t)$ is the modulation signal. The grid current typically has a faster response than the bus voltage. Thus, the instantaneous bus voltage $v_D(t)$ in (5) can be approximated with its average value V_D. Equations (1)–(5) lead to the transfer function of the grid current given by

$$i_g(s) = \underbrace{\frac{sC_fR_f + 1}{C_fL_1L_2s^3 + C_f(L_1+L_2)R_fs^2 + C_f(L_1+L_2)s}}_{G_{LCL}(s)} v_c(s) - \underbrace{\left(\frac{L_1C_fs^2}{C_fR_fs+1} + 1\right)}_{G_{iw}(s)} v_g(s) \tag{6}$$

Neglecting power losses in the VSC and the DAB DC-DC converter, the bus voltage is governed by

$$v_D(t)\left(C_D\frac{dv_D(t)}{dt}\right) = p_B(t) - v_c(t)i_1(t) \tag{7}$$

where $p_B(t)$ is the battery power. The instantaneous power in the *LCL* filter is comparatively small, which yields

$$v_c(t)i_1(t) \approx \underbrace{v_g(t)i_g(t)}_{p_g(t)} \tag{8}$$

where $p_g(t)$ is the instantaneous grid power. Substitution of (8) into (7) and linearizing around the average bus voltage setpoint V_D^*, the bus voltage dynamic becomes

$$V_D^*C_D\frac{dv_D(t)}{dt} \approx p_B(t) - p_g(t) \tag{9}$$

The grid voltage is given by

$$v_g(t) = \hat{V}_1\cos\omega t \tag{10}$$

where $\hat{V}_1$ is the amplitude of the fundamental component, and $\omega_1 = 2\pi f_1$ is the fundamental frequency of the grid voltage. The grid current is usually controlled to be sinusoidal with an amplitude of $\hat{I}_1$ and a phase angle of ϕ_1, as given by

$$i_g(t) = \hat{I}_1\cos(\omega t + \phi_1) \tag{11}$$

The grid current in (11) can be decomposed to the $dq-$axes components $i_d(t)$ and $i_q(t)$ in the virtual synchronous reference frame as

$$i_g(t) = \underbrace{\hat{I}_1\cos\phi_1}_{i_d}\cos\omega t - \underbrace{\hat{I}_1\sin\phi_1}_{i_q}\sin\omega t \tag{12}$$

The grid current in (11) leads to the instantaneous grid power expressed by

$$p_g(t) = \underbrace{\frac{\hat{V}_1}{2} i_d}_{P_{g1}} + \underbrace{\underbrace{\frac{\hat{V}_1}{2} i_d \cos 2\omega t}_{P_{g1}} - \underbrace{\frac{\hat{V}_1}{2} i_q \sin 2\omega t}_{Q_{g1}}}_{\tilde{p}_{g1}(t)} \tag{13}$$

where $P_{g1}(t)$ and $Q_{g1}(t)$ are the average active and reactive power components, and $\tilde{p}_{g1}(t)$ is the oscillating power component at the frequency of 2ω. The oscillating power component $\tilde{p}_{g1}(t)$ causes a 2ω ripple component $\tilde{v}_D(t)$ in the bus voltage, while the average power component $P_{g1}(t)$ changes the average component $V_D(t)$ of the bus voltage. By substituting $P_{g1}(t)$ in (13) into (9), $V_D(t)$ can be approximated as

$$V_D^* C_D \frac{dV_D(t)}{dt} \approx P_B(t) - \underbrace{\frac{\hat{V}_1}{2} i_d(t)}_{P_g(t)} \tag{14}$$

where $P_B(t)$ is the average component of the battery power. Note that (14) is accurate for a frequency below 2ω.

3.2. VSC Control System Implementation

Figure 4 shows the VSC control system. A proportional-integral (PI) regulator is employed for the bus voltage control loop with a low-pass filter (LPF) for shaping the loop frequency response. Meanwhile, the grid current controller adopts the unbalanced synchronous reference frame control with PI regulators for the fundamental component. This control technique employs the grid current as the α-component and the orthogonal reference current $i_\beta^*(t)$ as the β-component for the axis transformation. In our previous work [24], the stationary reference frame equivalence $G_{ci1}(s)$ of the unbalanced synchronous reference frame control with the PI regulators was theoretically and experimentally proven to be identical to a proportional-resonant regulator, as given by

$$G_{ci1}(s) = K_{p1} + \frac{K_{i1} s}{s^2 + \omega^2} \tag{15}$$

where K_{p1} and K_{i1} are the proportional and integral gains of the PI controller. Three possible harmonic sources distort the grid current waveforms, which can be suppressed by multiple resonant (MR) controllers given by

$$G_{cih}(s) = \sum_{h=3}^{n} \frac{K_{ih} s}{s^2 + (h\omega)^2} \tag{16}$$

where h is the harmonic order number, and K_{ih} is the resonant gain at order h^{th}.

Figure 5 depicts the stationary reference frame's equivalent grid current control block diagram. The VSC is represented by

$$G_{PWM}(s) = V_D e^{-sT_d} \tag{17}$$

where T_d is the delay time caused by the sampling time of the control system and the transportation time of the pulse width modulation (PWM) process. Undesirable low-frequency harmonic components can be present in the grid voltage $v_g(t)$ and in the VSC terminal voltage $v_c(t)$ due to switching dead times. The 2ω ripple component in the bus voltage control loop with a bandwidth greater than 0.2ω also distorts the reference current

$i_g^*(t)$ [24]. With this current control structure, the transfer functions of the grid current to these three harmonic sources are written as follows [24].

$$G_{cl}(s) = \frac{i_g(s)}{i_g^*(s)} = \frac{G_{ci}(s)G_{PWM}(s)G_{LCL}(s)}{1 + \{G_{ci}(s) + G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)} \tag{18}$$

$$Y_{VSC}(s) = \frac{i_g(s)}{v_c(s)} = \frac{G_{LCL}(s)}{1 + \{G_{ci}(s) + G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)} \tag{19}$$

$$Y_g(s) = \frac{i_g(s)}{v_g(s)} = \frac{-G_{FW}(s)G_{LCL}(s)}{1 + \{G_{ci}(s) + G_{cih}(s)\}G_{PWM}(s)G_{LCL}(s)} \tag{20}$$

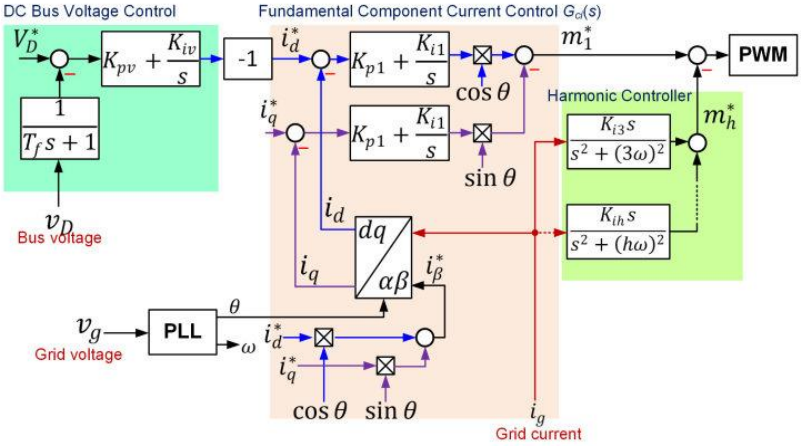

Figure 4. Bust voltage and grid current control block diagram of the VSC.

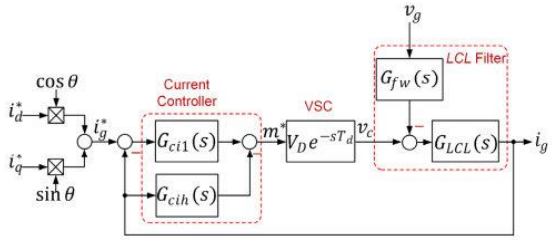

Figure 5. The stationary reference frame's equivalent control block diagram of the grid current in the stationary reference frame.

The MR regulator has infinite gains at selective frequencies, attenuating the harmonic components in $i_g^*(t)$, $v_g(t)$, and $v_c(t)$. Meanwhile, the fundamental component of $i_g^*(t)$ is regulated by the unbalanced synchronous reference frame controller with an infinite gain at ω_1. Figure 6 depicts the equivalent bus voltage control loop. The low-pass filter time constant T_f designed with the PI controller's constants K_{pv} and K_{iv} is used for loop shaping. The grid current control loop is approximated as a unity gain because its bandwidth is far higher than the bus voltage control loop. The rejection of the harmonic components in the

reference current allows the bandwidth of the bus voltage control loop to increase while maintaining the grid current near sinusoidal.

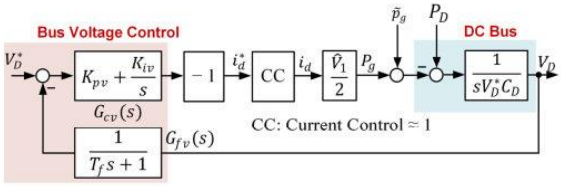

Figure 6. Equivalent control block diagram of the bus voltage.

This study employs the discontinuous PWM techniques shown in Figure 7. The positive half of $m(t)$ is used as the duty ratio reference for switches S_9 and S_{10}, and the positive half of $-m(t)$ for switches S_{11} and S_{12}. This PWM technique has a lower common-mode voltage and switching loss than the unipolar PWM [27]. Meanwhile, the VSC current $i_1(t)$ maintains a small ripple due to the three-level voltage output at the VSC terminal. Figure 8 illustrates the generation of the switching signals and interrupt setting. Time base counter 1 of the microcontroller [26] is set to operate in the up-down mode with the counter maximum value of PWMprd, which generates the interrupt signal when the counter value equals zero. The value of PWMprd is obtained from

$$\text{PWMprd} = \frac{1}{2} \times \frac{f_{clk}}{f_{sw}} \tag{21}$$

where $f_{clk} = 100$ MHz is the microcontroller's clock frequency [26]. Thus, PWMprd = 2500 for a switching frequency of 20 kHz. This interrupt signal simultaneously triggers the selected analog-to-digital converters (ADCs) for voltage and current signal sampling at the time instant k and the interrupt service routine (ISR) of the control algorithm for the VSC and DAB DC-DC converter. The resultant duty ratios are updated at the time instant $k+1$. Each counter consists of two compare registers (CMFAx and CMFBx), independently controlling two PWM outputs (PWMxA and PWMxB). For the VSC control, only CMPAx registers generate the PWMxA outputs, while the PWMxB outputs are opposite to the relevant PWMxA outputs with a switching dead time (active high complementary with a dead time) [26]. Thus, the PWM1A and PWM1B outputs of counter 1 control switches S_9 and S_{10}, and the PWM2A and PWM2B outputs of counter 2 for switches S_{11} and S_{12}. The synchronized operation between the ADC and PWM samples the average value of the grid current in each switching period both for the positive and negative regions of the modulation signal, as illustrated in Figure 8.

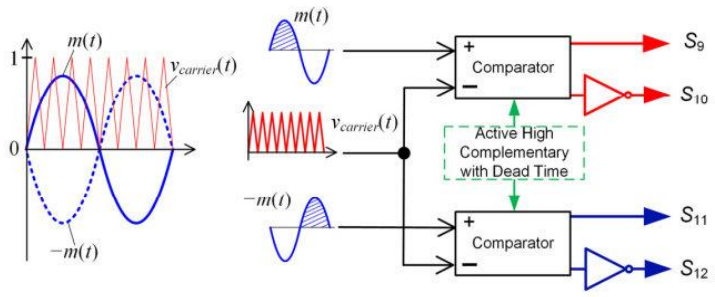

Figure 7. Discontinuous PWM block diagram for the VSC.

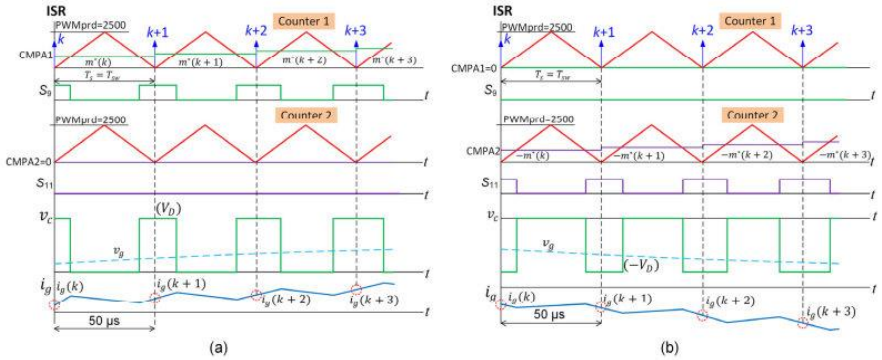

Figure 8. Timing diagram for interrupts, PWM generation, and analog signal samplings of the VSC: (**a**) for $m^*(t) \geq 0$; (**b**) for $m^*(t) < 0$.

4. Implementation of the Battery-Side DAB DC-DC Converter

4.1. Basic Operation of the DAB DC-DC Converter

Figure 9 illustrates the basic operation waveforms of the DAB DC-DC converter in the SPS modulation mode, where $\omega_{sw} = 2\pi f_{sw}$ and $\theta_{sw} = \omega_{sw} t$. The voltage $v_p(\theta_{sw})$ of the LV bridge leads the voltage $v_s(\theta_{sw})$ of the HV bridge by a phase angle of δ, which causes power to flow from the battery to the bus voltage. On the other hand, power transfers from the bus voltage to the battery with a phase angle of $-\delta$. Thus, the transferred power P_{DAB} of the DAB DC-DC converter is controlled by the angle δ by

$$P_{DAB} = \frac{V_D \left(\frac{N_s}{N_p}\right) V_B}{\omega_{sw} L_a} \delta \left(1 - \frac{|\delta|}{\pi}\right) \tag{22}$$

Neglecting losses in the DAB DC-DC converter, the average value I_{LVB} of the LV bridge input current i_{LVB} and the average battery current I_B are derived from P_{DAB} by

$$I_B = I_{LVB} = \frac{P_{DAB}}{V_B} = \left(\frac{N_s}{N_p}\right) \frac{V_D}{\omega_{sw} L_a} \delta \left(1 - \frac{|\delta|}{\pi}\right) \tag{23}$$

Hence, the phase angle δ is used as the controlled variable for the battery current control loop as shown in Figure 3. The theoretical range of the phase angle δ is $\pm\pi/2$. The DAB DC-DC converter exhibits the ZVS operation if the ratio between the voltages of the two DC sides is close to the transformer's turn ratio [28]. This ZVS range gets wider at a higher phase shift angle [14]. On the other hand, the root mean square (RMS) values of the MF transformer's currents increase with the phase shift angle [10].

Flux density $B(t)$ is an essential parameter for the design of the MF transformer and series inductor. According to the circuit topology in Figure 3, the transformer's primary winding is directly connected to the LV bridge. So, the peak flux density $\hat{B}_T$ of the transformer is proportional to the battery voltage, as given by

$$\hat{B}_T = \frac{1}{2N_p A_c} \int_0^{T_{sw}/2} v_p dt = \frac{V_B T_{sw}}{4N_p A_c} \tag{24}$$

where A_c is the cross-sectional area of the transformer core. Meanwhile, the peak flux density $\hat{B}_L$ of the series inductor is determined from the voltage across the inductor $v_{La}(\theta_{sw})$ in Figure 9, as given by

$$\hat{B}_L = \frac{1}{2N_L A_c}\int_0^{T_{sw}/2} v_{La}dt = \frac{T_{sw}}{4N_L A_c}\left\{\pi\frac{N_s}{N_p}V_B + (2\delta - \pi)V_D\right\} \quad (25)$$

where N_L is the winding turn number of the inductor. The peak flux densities $\hat{B}_T$ and $\hat{B}_L$ must be kept below the saturation flux density $\hat{B}_{sat}$ of the core material.

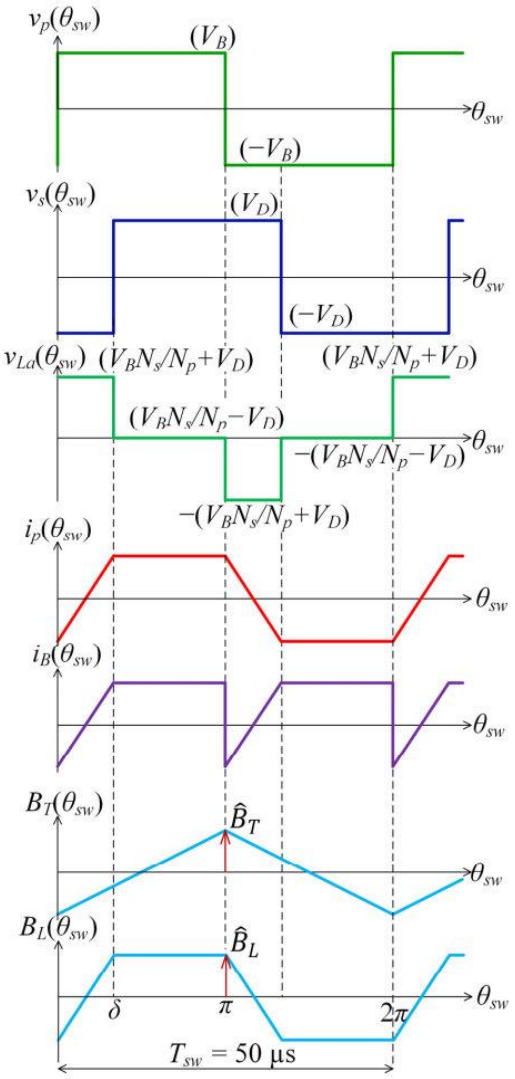

Figure 9. Voltage, current, and flux density waveforms of the DAB DC-DC converter with the SPS modulation strategy [28].

4.2. Design of the Transformer and Series Inductor

The MF transformer of the DAB DC-DC converter is a crucial element for transferring power and voltage conversion between the two DC sides. Meanwhile, the series inductor L_a limits the maximum power transfer. MnZn ferrite and nanocrystalline materials are suitable for the switching frequency of 20 kHz used in this study. For this application, the battery voltage varies with the state of charge and battery current, while the bus voltage is kept constant. Thus, the maximum allowable phase shift angle is $\pm\pi/3$ to exploit a large ZVS range at the rated power and achieve a fine battery current resolution, while the RMS values of the transformer currents are still acceptable. It was reported that nanocrystalline materials exhibited better power density and efficiency than MnZn ferrite material [10]. However, the cutting process of ribbon-wound nanocrystalline cores deteriorated their magnetic properties [10]. Hence, we selected N87 MnZn ferrite cores due to consistency in magnetic properties and market availability [29]. This core material has a saturation flux density of 0.39 T at 100 °C and is available in various core shapes.

An analytical transformer and inductor design method was chosen in this study [30]. The generalized Steinmetz equation expresses the core loss P_{fe} as a function of the core peak flux density $\hat{B}$. Meanwhile, the copper loss P_{cu} is derived from the RMS values of the transformer's currents and the winding resistance. Therefore, the winding resistance is derived from the core geometry, which is expressed as a function of the core peak flux density $\hat{B}$. Setting $P_{fe} = P_{cu}$ leads to the optimal peak flux density $\hat{B}_{opt}$, from which the minimum core size is obtained. An actual core size should be selected close to the optimal one.

The MF transformer and the inductor were designed at the nominal battery voltage V_{Bn} of 51.2 V using the peak flux densities given in (24) and (25). The transformer turn ratio is close to

$$\frac{N_s}{N_p} = \frac{V_D}{V_{Bn}} = \frac{400\ \text{V}}{51.2\ \text{V}} = 7.81 \tag{26}$$

The peak flux densities $\hat{B}_T$ and $\hat{B}_L$ calculated at the maximum battery voltage of 60 V were ensured to be below the core saturation value. The core loss coefficient was identified from the manufacturer's specification at the temperature of 100 °C. Enameled Litz wires were employed to minimize the skin and proximity effects from the switching frequency. The required value of L_a obtained from (23) is 297 µH. However, the inductance of 280 µH was used in the design to account for the leakage inductance of the MF transformer. Table 3 summarizes the key parameters of the MF transformer and series inductor. The actual core sizes are slightly larger than the required sizes. Thus, the peak flux densities $\hat{B}_T$ and $\hat{B}_L$ are smaller than their optimal values. This results in the estimated core losses being comparatively less than the copper losses. The predicted core loss using the generalized Steinmetz equation is based on the sinusoidal induction waveform. Moreover, the N87 ferrite material has a more significant core loss at low temperatures. In experiments, the core temperature was found to be lower than 60 °C, which agrees with our previous work with the same design methodology and core material [10]. Thus, the actual core losses are expected to exceed the predicted values.

Table 3. Parameters of the MF transformer and series inductor.

Parameters	Transformer	Inductor
Material	EPCOS N87 ferrite	EPCOS N87 ferrite
Core structure	2 sets of E65/32/27	1 set of ETD49 with 2 mm gap
Total core area, A_c	10.58 cm^2	2.11 cm^2
Magnetic length, l_m	14.7 cm	11.4 cm
Primary winding	4 turns 4 Litz wires (500 × WG40)	55 turns 2 Litz wires (128 × AWG40)
Secondary winding	31 turns 2 Litz wires (128 × AWG40)	-
$\hat{B}$ at 51.2 V/60 V	0.20 T/0.24 T	0.28 T/0.36 T

Table 3. *Cont.*

Parameters	Transformer	Inductor
Est. P_{cu} at 51.2 V V	9.1 W	4.0 W
Est. P_{fe} at 51.2 V V	8.7 W	2.2 W
Est. P_{tot} at 51.2 V V	17.8 W	6.2 W

4.3. Control System Implementation of the DAB DC-DC Converter

Figure 10 sketches the steady state timing diagram of the DAB DC-DC converter, implemented in the same ISR as the VSC control scheme in Figure 8. Counters 3–6 in the up-down mode generate the switching signals for the DAB DC-DC converter. The phase angles of counters 3–6 are synchronized with counter 1. Instead, the phase shift modulation is obtained by adjusting the CMPA3 to CMPA6 and the CMPB3 to CMPB6 registers of counters 3–6 [31]. During the rising period of counters 3–6, switches S_1, S_4, S_5, and S_8 are turned on when the values of the counters equal their CMPAs registers. For the falling period, switches S_1, S_4, S_5, and S_8 are turned off when the values of the counters equal their CMPBs registers. Thus, this modulation strategy accommodates the maximum phase shift angle of $\pm\pi/2$. Note that switches S_2, S_3, S_6, and S_7 complement switches S_1, S_4, S_5, and S_8 respectively.

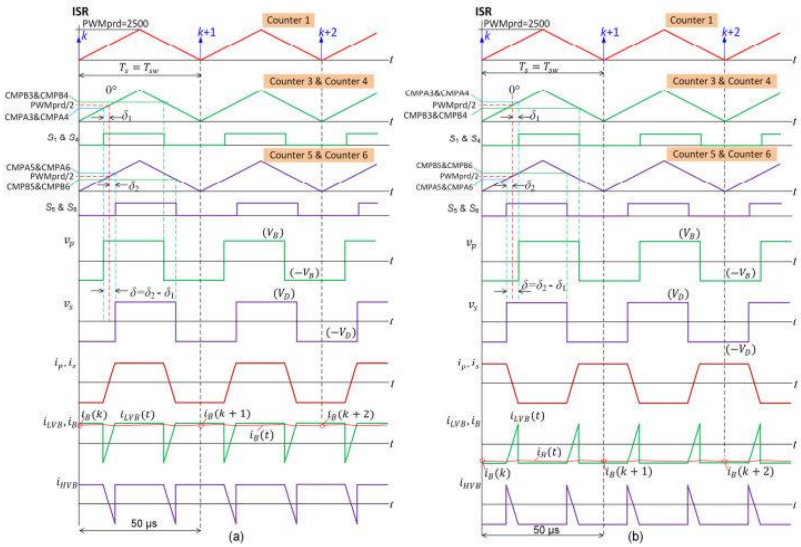

Figure 10. Steady-state timing diagram for the DAB DC-DC converter: (a) for $i_B(t) \geq 0$ (b) for $i_B(t) < 0$.

The phase shift angle $\delta = 0$ is set at $\pi/2$ of each ISR period to sample the average value of the battery current $i_B(t)$. The reference phase angles δ_1^* and δ_4^* for switches S_1 and S_4 of the LV bridge and δ_5^* and δ_8^* for switches S_5 and S_8 of the HV bridge are obtained from

$$\left.\begin{array}{c} \delta_1^* = \delta_4^* = -\frac{\delta^*}{2} \\ \delta_5^* = \delta_8^* = \frac{\delta^*}{2} \end{array}\right\} \tag{27}$$

where δ^* is the reference phase shift angle. Figure 9 shows the implementation diagram of the battery current control. The battery current is sampled every T_s. The discrete-time PI controller $G_{CB}(z)$ regulates the battery current $i_B(k)$ at instant k with the reference phase angle $\delta^*(k)$ as the output. The reference angles $\delta_1^*(k)$, $\delta_4(k)$, $\delta_5^*(k)$, and $\delta_8^*(k)$ are obtained from (27). The reference angles $\delta_1^*(k)$ and $\delta_8^*(k)$ are translated to the values of the CMPA3, CMPB3, CMFA6, and CMPB6 registers as depicted in Figure 11. Meanwhile, the reference angles $\delta_4(k)$ and $\delta_5^*(k)$ are delayed with a sampling period to prevent a large DC offset current in the transformer current $i_p(t)$ during the transient [20]. This method is to control the volt-second applied to the transformer to maintain a small DC offset. So, the values of CMPA4, CMPB4, CMFA5, and CMPB5 are accordingly determined from $\delta_4(k-1)$ and $\delta_5^*(k-1)$. The action qualifier submodule of each module defines the action of the PWMxA output when the CMFAx and CMPBx registers meet their conditions as indicated by "set" and "clear" in the brackets. Meanwhile, the PWMxB outputs are opposite to their PWMxA outputs, with a dead time of 1.25 µs similar to that of the VSC [26].

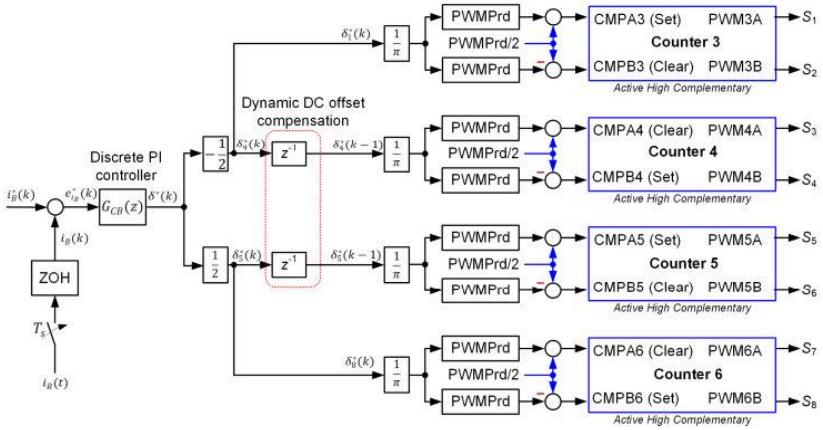

Figure 11. Implementation diagram of the battery current control loop of the DAB DC-DC converter.

4.4. Tuning of the Battery Current Control Loop

Figure 12 depicts the equivalent circuit on the battery side. The variables are averaged over a switching period of T_{sw}, denoted by the brackets $\langle\ \rangle$. Equation (23) yields the average current $\langle i_{LVB} \rangle$ of the DAB DC-DC converter, while the battery is simplified with an open-circuit voltage $\langle e_0 \rangle$ and an internal resistance R_i. The Thevenin-based equivalent circuit consisting of internal series resistance and capacitance paralleled with another resistance is more accurate than that in Figure 12 [32]. The Thevenin-based capacitance is much larger than the battery-side capacitance C_B [33]. From the control point of view, thus, the open-circuit voltage $\langle e_0 \rangle$ in Figure 12 including the voltage drops in the Thevenin-based capacitance is the disturbance of the battery current control loop. Figure 13 depicts the equivalent block diagram of the battery current in the continuous time domain, where a PI regulator with the constants K_{pb} and K_{ib} controls the battery current. A delay of $T_d = 2T_s$ represents the sampling and transport delays, as illustrated in Figure 10. The gain K_{DAB} is derived from the possible maximum value of (23), as given by

$$K_{DAB} = \frac{\langle i_{LVB} \rangle}{\delta} = \left(\frac{N_s}{N_p}\right) \frac{V_D}{\omega_{sw} L_a} \tag{28}$$

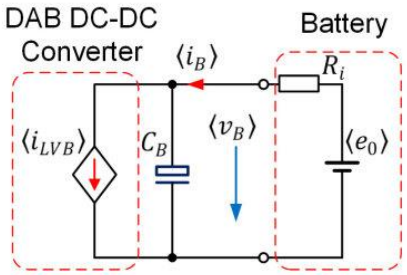

Figure 12. Equivalent circuit on the battery side.

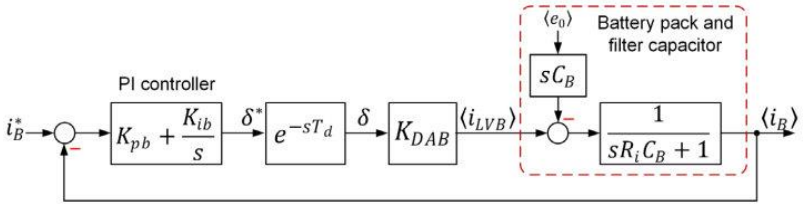

Figure 13. Equivalent control block diagram of the battery current.

According to (23), this gain K_{DAB} decreases with the angle δ for a higher battery current. However, the approximated gain K_{DAB} at its maximum value guarantees the maintenance of loop stability at a high current.

The open loop transfer function of the battery current control loop is written as

$$G_{bol}(s) = \left(K_{pb} + \frac{K_{ib}}{s}\right)\frac{K_{DAB}}{sR_iC_B + 1} \tag{29}$$

where the delay T_d is neglected as it usually is much smaller than the time constant R_iC_B. The closed-loop transfer function is given as

$$G_{bcl}(s) = \frac{\left(\frac{K_{DAB}}{R_iC_B}\right)s + \left(\frac{K_iK_{DAB}}{R_iC_B}\right)}{s^2 + \left(\frac{1+K_{pb}K_{DAB}}{R_iC_B}\right)s + \left(\frac{K_iK_{DAB}}{R_iC_B}\right)} \tag{30}$$

Compared to the standard second-order system [34], K_{pb} and K_{ib} can be written as

$$\left.\begin{aligned} K_{ib} &= \omega_0^2\frac{R_iC_B}{K_{DAB}} \\ K_{pb} &= \frac{2\zeta\omega_0R_iC_B - 1}{K_{DAB}} \end{aligned}\right\} \tag{31}$$

where ω_0 is the natural frequency, and ζ is the damping factor of the closed-loop system. If R_i is unknown, a trial-and-error tuning method can be adopted by adjusting K_{ib} for ω_0^2 and K_{pb} for ζ.

5. Experimental Validation

5.1. Experimental Setup

Figure 14 depicts the experimental setup. A TMS320F280049C microcontroller controlled the VSC and DAB DC-DC converter with the parameters listed in Table 2. A switching dead time of 1.25 µs was applied to each leg of the VSC and DAB DC-DC con-

verter. A 16-cell 100 Ah LFP battery pack supplied the DAB DC-DC converter, while the VSC was connected to a Chroma 61860 grid simulator. We adopted the tuning procedure of the VSC presented in our previous work [24] with a bus voltage bandwidth of 30π rad/s and the current harmonic controllers, orders 3rd, 5th, 7th, and 9th for mitigation of the grid current waveform. The bus voltage was regulated at 400 V. The response of the battery current was tuned by the trial-and-error method with the guidelines given in (31). The battery management system has a maximum current of 30 A, which, unfortunately, limits the maximum system power within ± 1.5 kW or 50% of the rated power.

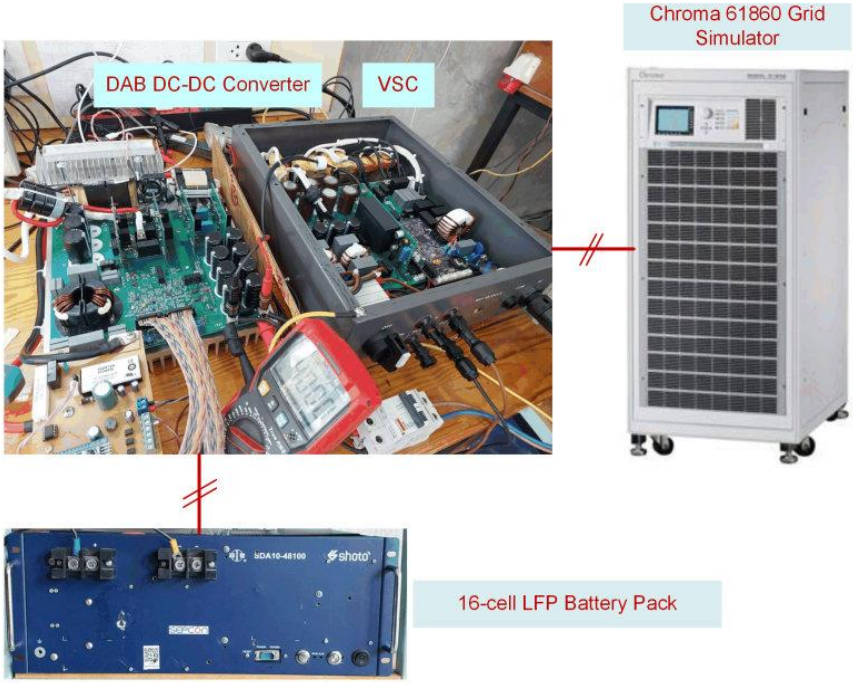

Figure 14. Experimental setup.

5.2. Experimental Results

5.2.1. Validation of the Dynamic DC Offset Compensation Scheme

The grid simulator supplied the VSC, and the bus voltage was regulated at 400 V. The DAB DC-DC converter operated with the reference phase angle δ^* in the open-loop control. Figure 15a depicts the transient response of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's primary current $i_p(t)$, and the inverted battery current $-i_B(t)$ under the step change of the reference angle δ^* changing from zero to $\pi/4$. In contrast, Figure 15b shows those waveforms for the reference angle δ^* changing from zero to $-\pi/4$. Without the dynamic DC offset compensation scheme shown in Figure 11, $i_p(t)$ exhibits a DC offset of approximately 30 A. This large current can cause saturation in the transformer core and may damage the switching devices. The DC offset compensation technique in Figure 11 is effective as the dynamic DC component of $i_p(t)$ is reduced significantly during the changes in the reference angle δ^*. Meanwhile, the DC offset compensation scheme does

not affect the steady waveform of $i_p(t)$. The first-order response of the battery current $i_B(t)$ agrees with the equivalent circuit in Figure 12.

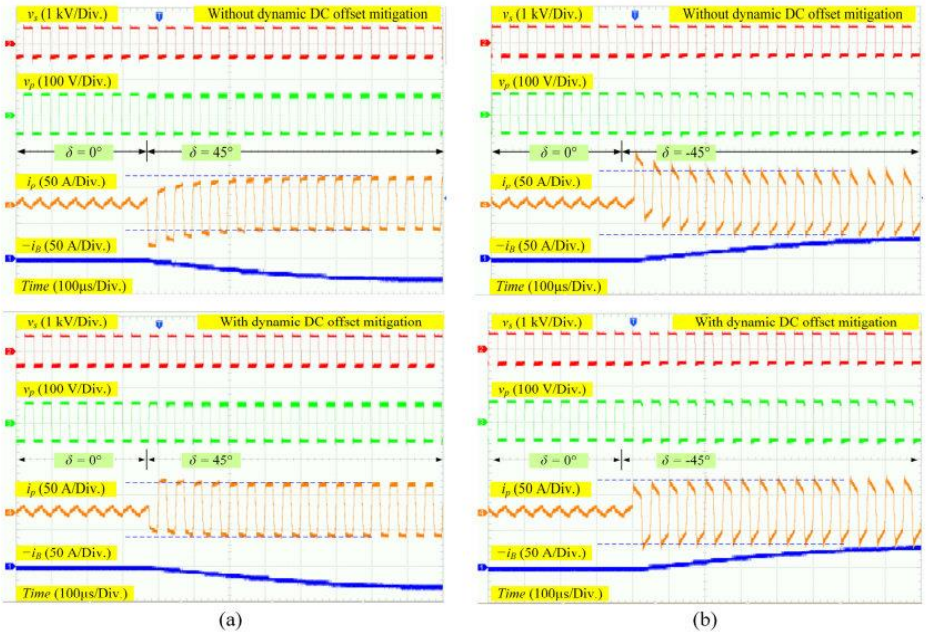

Figure 15. Open-loop transient response of the DAB DC-DC converter with and without the dynamic DC offset compensation scheme: (**a**) δ^* changing from 0 to $\pi/4$; (**b**) δ^* changing from 0 to $-\pi/4$.

5.2.2. Validation of the Closed-Loop Control of the Battery Current

The battery current control loop was tuned for a smooth response with a settling time of approximately 80 ms. The reference battery current i_B^* was set to create the battery power in the range of ±1.5 kW. Figure 16 shows the experimental results in the discharging mode with a battery power of 1.5 kW. Although the discharged power from the battery causes the bus voltage to increase, the bus voltage controller forces the bus voltage to return to the reference of 400 V within four cycles, as shown in Figure 16a. Figure 16b depicts the steady-state waveforms of $v_D(t)$, $v_g(t)$, and $i_g(t)$. The grid current waveform is nearly sinusoidal thanks to the current harmonic current controller, which attenuates the harmonic components in the reference grid current and the VSC terminal voltage caused by the dead time. Figure 16c illustrates that a step change in the battery reference current i_B^* does not create a DC offset in the transformer's primary current $i_p(t)$, thanks to the DC offset compensation scheme implemented in the SPS modulation system in Figure 11. Meanwhile, the battery current $i_B(t)$ smoothly increases toward its reference. The steady-state waveforms of $v_p(t)$, $v_s(t)$, and $i_p(t)$ in Figure 16d agree with the sketched waveforms in Figure 10. At this operating point, the battery voltage was 51.5 V, close to the designed value of the MF transformer.

Figure 17 shows the experimental results in the charging mode with a battery power of −1.5 kW. The bus voltage $v_D(t)$, grid current $i_g(t)$, transformer's primary current $i_p(t)$, and battery current $i_B(t)$ respond to the battery reference current i_B^* in the same fashion as the discharging mode with the opposite direction. The steady-state grid current waveform

remains nearly sinusoidal. However, the steady-state waveform of $i_p(t)$ indicates that the DAB DC-DC converter operates in the boost mode, where $(N_s/N_p)V_B > V_D$ [19]. At this operating point, the battery voltage was 54.3 V, causing $(N_s/N_p)V_B = 424$ V.

Figure 18 shows the battery voltage, total efficiency of the VSC and DAB DC-DC converter, and total harmonic distribution (THD_i) of grid current with battery power. As expected, the battery voltage in the charging mode is greater than that in the discharging mode. The inverter's efficiency in the charging mode is lower than in the discharging mode. Partly, it is believed to be due to the mismatched voltage ratio of the MF transformer, which deviates the operating point out of the ZVS region o and increases RMS values in the transformer currents [28]. Thus, a variable DC voltage strategy with the battery voltage and a duty ratio adjustment of the transformer would improve the inverter's efficiency. The THDi values at 50% of the rated power are less than 1.5%, which are expected to be lower at the rated power of 3 kW.

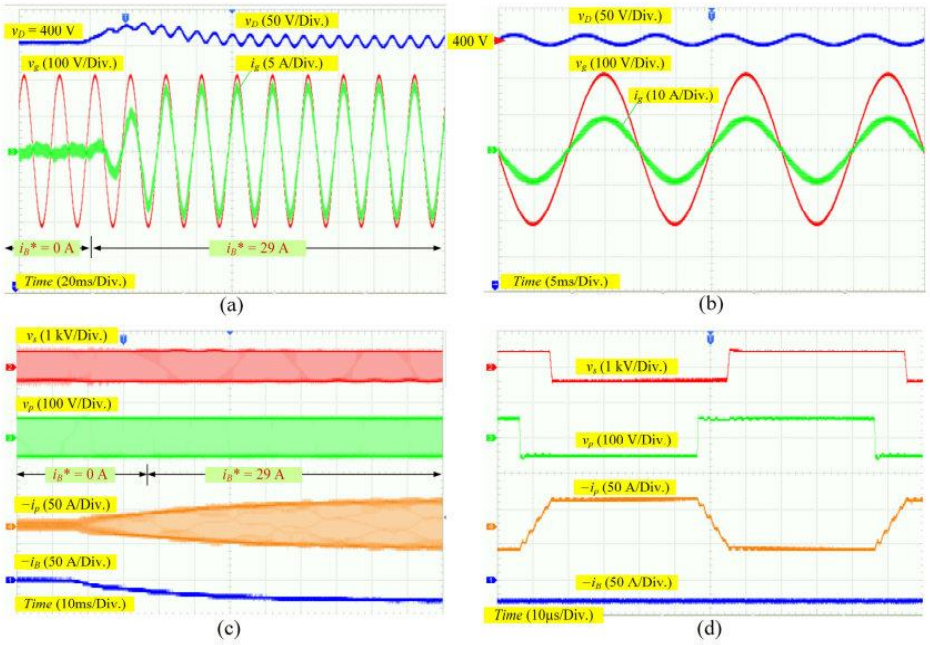

Figure 16. Experimental results of the closed-loop control of the battery current in the discharging mode with the battery power of 1.5 kW: (**a**) transient response of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$; (**b**) steady-state waveforms of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$; (c) transient response of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current $-i_B(t)$; (d) steady-state waveforms of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current $-i_B(t)$.

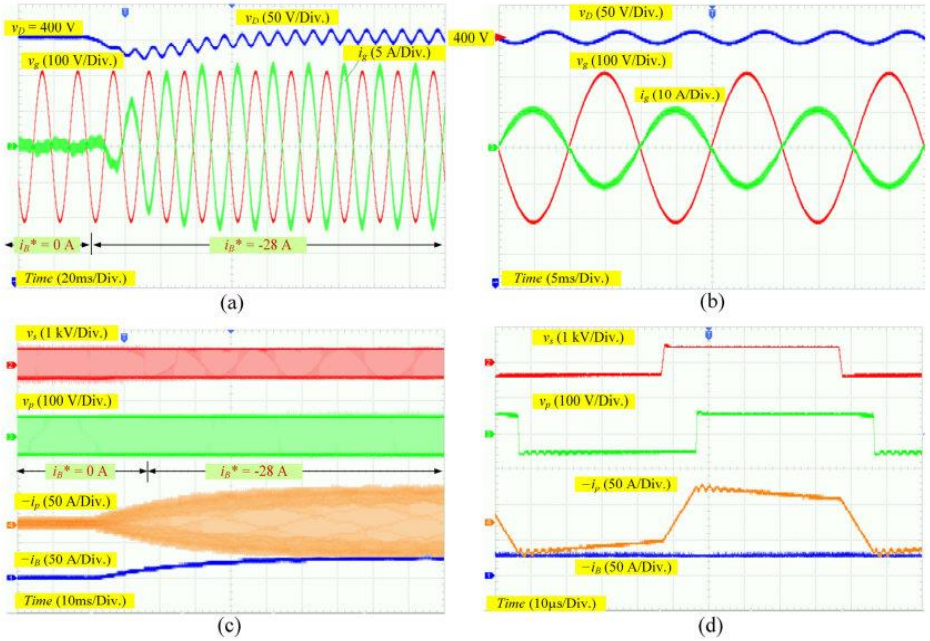

Figure 17. Experimental results of the closed-loop control of the battery current in the charging mode with the battery power of −1.5 kW: (**a**) transient response of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$; (**b**) steady-state waveforms of the bus voltage $v_D(t)$, grid voltage $v_g(t)$, and grid current $i_g(t)$; (**c**) transient response of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current $-i_B(t)$; (**d**) steady state waveforms of the primary and secondary voltages $v_p(t)$ and $v_s(t)$, the transformer's inverted primary current $-i_p(t)$, and the inverted battery current $-i_B(t)$.

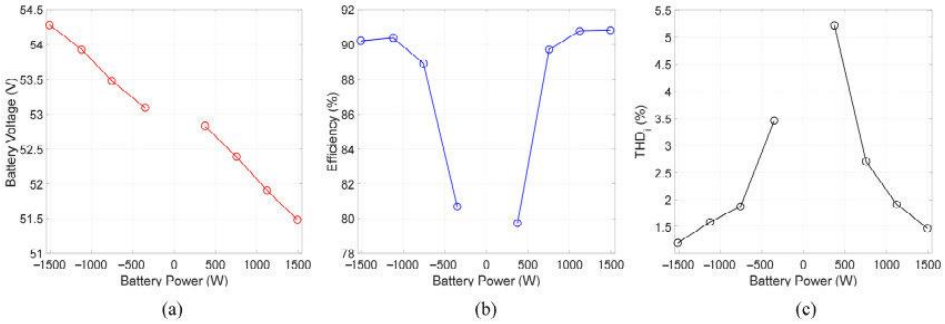

Figure 18. (**a**) Battery voltage V_B with battery power; (**b**) inverter's efficiency with battery power; (**c**) total harmonic distortion of grid current with battery power.

6. Conclusions and Future Outlook

A single-phase grid-connected 51.2-V battery inverter consisting of an *LCL*-filtered voltage source converter (VSC) and a dual active bridge (DAB) DC-DC converter was constructed. The control systems of the two converters were implemented in the same interrupt service routine on a TMS320F280049C microprocessor with a sampling and switching frequency of 20 kHz—the time base counters for switching generation of the DAB DC-DC converter synchronized with those of the VSC. The single-phase shift modulation strategy of the DAB DC-DC converter was adjusted through two separate compare registers with the time base counters during the count-up and count-down periods. This phase shift modulation was easy to implement on a standard microcontroller for power converter control. A DC offset compensation integrated with the battery current control loop allowed a smooth change in the battery and medium-frequency transformer's currents in response to a reference current step. The VSC adopted a bus voltage control with a unified harmonic mitigation strategy. Experimental validations in the charge and discharge operations exhibited a total system efficiency better than 90% and total harmonic distortion in the grid current lower than 1.5%.

However, certain aspects must be studied further to improve the proposed residential battery inverter as follows:

(1) Adoption of advanced battery current control schemes regardless of the battery's internal impedance parameters.
(2) Increasing the switching frequency and improving the modulation strategies of the DAB DC-DC converter to enhance efficiency and power density.
(3) Optimizing the design of the ripple filter on the battery side.

Author Contributions: Conceptualization, A.P. and S.S.; methodology, A.P. and S.S.; software, A.P. and T.K.; validation, A.P., T.K. and C.S.; formal analysis, A.P., S.S., P.P. and M.H.; investigation, A.P. and S.S.; resources, S.S.; data curation, A.P.; writing—original draft preparation, A.P. and S.S.; writing—review and editing, S.S., P.P. and M.H.; visualization, A.P. and T.K.; supervision, S.S.; project administration, S.S.; funding acquisition, S.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research was partially supported by the Royal Golden Jubilee Ph.D. Program, grant number PHD02282560, and the Global and Frontier Research University Fund, Naresuan University, grant number R2567C002.

Data Availability Statement: The data presented in this study is available in the article.

Conflicts of Interest: The authors declare no conflict of interest.

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