INVESTIGATION OF CURRENT HARMONIC MITIGATION TECHNIQUES FOR THREE-PHASE GRID-CONNECTED INVERTER UNDER VOLTAGE DISTORTION

SUPARAK SRITA

A Thesis Submitted to the Graduate School of Naresuan University
in Partial Fulfillment of the Requirements
for the Doctor of Philosophy in Smart Grid Technology
2023

INVESTIGATION OF CURRENT HARMONIC MITIGATION TECHNIQUES FOR THREE-PHASE GRID-CONNECTED INVERTER UNDER VOLTAGE DISTORTION

SUPARAK SRITA

A Thesis Submitted to the Graduate School of Naresuan University
in Partial Fulfillment of the Requirements
for the Doctor of Philosophy in Smart Grid Technology
2023

Thesis entitled "Investigation of Current Harmonic Mitigation Techniques for Three-Phase Grid-Connected Inverter Under Voltage Distortion"

By Suparak Srita

has been approved by the Graduate School as partial fulfillment of the requirements

for the Doctor of Philosophy in Smart Grid Technology of Naresuan University

Oral Defense Committee

..... Chair
(Associate Professor Pisit Liutanakul, Dr.Ing.)

..... Advisor
(Associate Professor Sakda Somkun, Ph.D.)

..... Internal Examiner
(Assistant Professor Sahataya Thongsan, Ph.D.)

..... Internal Examiner
(Associate Professor Pisit Maneechot, Ph.D.)

..... Internal Examiner
(Phatcharin Yaowarat, Ph.D.)

Approved

.....
(Associate Professor Krongkarn Chootip, Ph.D.)
Dean of the Graduate School

Title	INVESTIGATION OF CURRENT HARMONIC MITIGATION TECHNIQUES FOR THREE-PHASE GRID-CONNECTED INVERTER UNDER VOLTAGE DISTORTION
Author	Suparak Srita
Advisor	Associate Professor Sakda Somkun, Ph.D.
Academic Paper	Ph.D. Dissertation in Smart Grid Technology, Naresuan University, 2023
Keywords	Multi-resonant controllers (MR); Multiple synchronous reference frame (MSR) controllers; Harmonic compensators (HCs); Voltage-source converter (VSC); Hardware-in-the-loop (HiL); LCL-filter; discrete-time control; harmonics; grid-connected inverter; modeling; voltage source converter

ABSTRACT

This study presents a novel approach to harmonic compensation in three-phase grid-connected voltage source converters (VSCs), addressing challenges presented by grid voltage distortion and frequency variations. It introduces an advanced simulation method within the MATLAB/Simulink environment that accurately replicates the functionality of discrete-time controlled grid-connected VSCs. This method employs switched-circuit modeling for simulating the power stage in the continuous-time domain, seamlessly integrating with the physical unit scale. The control algorithm, formulated in a MATLAB function on a per-unit scale, is efficiently convertible into C language for deployment on a 32-bit C2000 DSP controller, ensuring uniformity in the parameters of the regulators. Extensive testing of this methodology utilized both a hardware-in-the-loop real-time simulator and a 5-kVA three-phase LCL-filtered grid-connected VSC. This included the application of a discrete-time control scheme within the synchronous reference frame. The study explores the effectiveness of Proportional-Integral plus Multi-Resonant (PIMR) controllers in mitigating high-order harmonic currents by employing harmonic

compensators at the 6th and 12th harmonic orders. This strategy focuses on minimizing grid voltage harmonic orders 5th, 7th, 11th, and 13th, achieving a total harmonic distortion (THD) of 4.69%. Implemented on a TMS320F28379D digital signal processor, the PIMR controller demonstrated enhanced performance over the traditional Multiple Synchronous Reference Frame (PIMSR) controller. It achieved significant harmonic rejection in the grid current, with a THD nearing 1% aligning with the IEEE 1547 standard and realizing a 35% reduction in computational time.

ACKNOWLEDGEMENTS

Completing this doctoral thesis has been an extraordinary journey, one that I could not have navigated without the unwavering support, guidance, and encouragement of several key individuals in my academic and personal life. At the forefront of this journey has been my advisor, Associate Professor Dr. Sakda Somkun, whose expertise, patience, and insightful feedback have been pivotal in shaping my research and academic growth. His dedication to excellence and commitment to fostering a nurturing and challenging academic environment have inspired me to push the boundaries of my understanding and capabilities. I am deeply grateful for his mentorship and unwavering belief in my potential.

Equally, this thesis would not have been possible without the love, encouragement, and sacrifices of my family. To my father and mother, thank you for instilling in me the value of hard work, perseverance, and education from an early age. To my wife, your understanding, encouragement, and love have provided me with the strength and peace of mind needed to focus on my research. Your belief in my abilities has been a constant source of motivation.

I am grateful to the Energy Policy and Planning Office (EPPO), Ministry of Energy, Thailand, for sponsoring my doctoral study. Including my originator, Rajamangala University of Technology Lanna Chiang Mai, who supported me during my PhD studies this time.

This work was supported in part by an International Research Partnership "Electrical Engineering – Thai French Research Center (EE-TFRC)" under the project framework of the Lorraine Université d'Excellence (LUE) in cooperation between Université de Lorraine and King Mongkut's University of Technology North Bangkok, and in part by the National Research Council of Thailand (NRCT) under Senior Research Scholar Program under Grant No. N42A640328

This thesis stands as a testament to the collective support, encouragement, and belief of all those mentioned, and many not named but equally appreciated. I am profoundly grateful to each of you for your part in my journey.

Suparak Srita

TABLE OF CONTENTS

Page

List of tables

Page

List of figures

Page

ABBREVIATIONS

ADC	Analog-to-digital converter
DAC	Digital-to-analog converter
DSP	Digital signal processor
HC	Harmonic controller
HiL	Hardware in the loop
IGBT	Insulated-gate bipolar transistor
ISR	Interrupt service routine
MR	Multiple resonant
PI	Proportional-integral
PIMR	Proportional-integral plus multi-resonant
PLL	Phase-locked loop
PWM	Pulse width modulation
SO	Symmetrical optimum
SVM	Space vector modulation
THD	Total Harmonic Distortion
VSC	Voltage source converter
ZOH	Zero-order hold
$\boldsymbol{d_a}$, $\boldsymbol{d_b}$ and $\boldsymbol{d_c}$	Duty ratios
$\boldsymbol{f_s}$	Sampling frequency
$\boldsymbol{f_{sw}}$	Switching frequency
$\boldsymbol{f_{LCL}}$	Resonant frequency of the LCL filter
$\boldsymbol{i_D}$	VSC DC current
$\boldsymbol{i_{ga}}$, $\boldsymbol{i_{gb}}$, and $\boldsymbol{i_{gc}}$	Grid currents
$\boldsymbol{i_{Ia}}$, $\boldsymbol{i_{Ib}}$, and $\boldsymbol{i_{Ic}}$	VSC currents
$\boldsymbol{i_o}$	DC bus current
$\boldsymbol{S_a}$, $\boldsymbol{S_b}$, and $\boldsymbol{S_c}$	VSC switching signals
$\boldsymbol{T_d}$	PWM delay time
$\boldsymbol{T_s}$	Sampling period
$\boldsymbol{T_{sw}}$	Switching period

v_D	DC bus voltage
v_{Fa}, v_{Fb} and v_{Fc}	LCL filter voltages
v_{ga}, v_{gb} and v_{gc}	Grid voltages
v_{Ia}, v_{Ib} and v_{Ic}	VSC terminal voltages
θ	Angle of the grid voltage
ϕ_{mi}	Phase margin
ω	Grid angular frequency
ω_{ci}	Cross-over frequency
ω_{gn}	Nominal grid angular frequency
ω_{LCL}	Resonant angular
Subscripts	
d and q	Signals in the synchronous reference frame
ref	Refence signals
α and β	Signals in the stationary reference frame
Superscripts	
$'$	Signals in the per unit scale
Symbols	
$\hat{x}$	Peak value or estimated value
$\langle x \rangle$	averaged variables over T_s

CHAPTER I

INTRODUCTION

Background and Motivation

In recent years, research has focused on distributed generation (DG) systems, powered by renewable energy sources, such as micro-hydro turbines, hydrogen fuel cells, photovoltaics, wind turbines, etc., due to the limited fossil fuels. Meanwhile, fossil fuels are the main energy supplier of the worldwide economy, but the recognition of them as being a major cause of environmental problems and also causing climate change problems is caused by greenhouse gas emissions from industry and transportation. Moreover, the increasing demand for energy can create problems for the grid, such as grid stability, power quality, and even outages. The necessity of producing more energy, combined with the interest in clean technologies, yields increased development of power distribution systems using renewable energy [1].

Furthermore, responding to environmental problems in terms of energy consumption, there is a noticeable increase in electric vehicles (EVs), such as plug-in hybrid EVs (PHEVs) and battery EVs (BEVs). It needs charging from the grid, which will result in increased energy consumption [2, 3]. The voltage source converter (VSC) is an important part of bringing different clean energy sources into the power grid. It can convert energy from direct current to alternating power or vice versa. For example, in an application on battery energy storage systems (BESS), a battery inverter can send direct current power from the battery to the grid. On the other hand, it can receive the energy from the grid to flow into the battery. With both modes operating without any changes in hardware components [4, 5].

In Figure 1, a low-voltage power grid system is shown, which consists of a distributed transformer connected between the medium-voltage and low-voltage sides. The nonlinear loads are connected to the point of common coupling (PCC), which injects harmonic current into the grid. Therefore, if the low voltage power grid system

has a high harmonic current, it will affect the voltage, resulting in high distortion. This effect will be more intense if the position of the nonlinear load is very far from the distributed transformer due to the high grid impedance [6, 7].

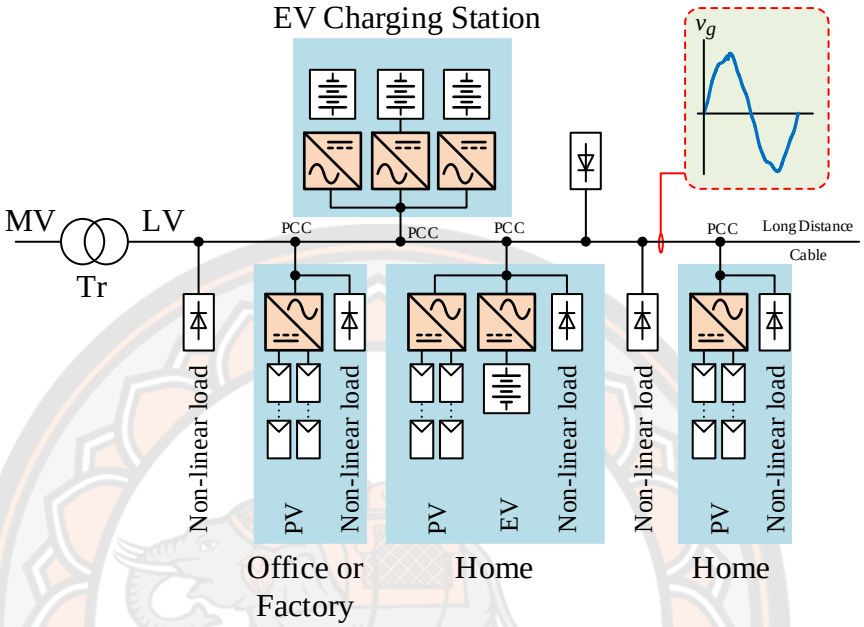


Figure 1 The general structure of the VSC used in the low-voltage grid system.

Together, In the present, the photovoltaic grid-connected inverter is the most commonly used distributed power generation systems [8]. It is used as a part in homes and offices, including the hybrid inverter, which has a battery for backup power. Meanwhile, EVs are becoming increasingly active, resulting in big loads on the power grid. Moreover, level 3 charging stations are DC voltage fast mode charging, which consumes a lot of power in the power grid system [9]. These have a voltage source converter (VSC) as the main component, which can convert power between the power grid and load by maintaining the good properties of AC and DC power.

However, if the power grid has harmonic voltage distortion caused by the nonlinear loads injecting harmonic current into the grid [10]. The VSC without harmonic compensations (HCs) will create a high-order harmonic current when connected to the grid voltage distortion[11]. It is seen in Figure 2. that the grid current is significantly distorted by the grid voltage harmonics. The HCs for the VSC under distorted grid voltage are still essential for research. In order to improve the quality of

the grid current waveform to be consistent with grid standards such as IEEE 1547-2018 [12] which specifies the limit in each harmonic order.

The harmonic compensations (HCs) are controlled by a controlled by a parallel controller in the current control loop. Some research offers methods to solve high-order harmonic current problems. All the same, the aim was to mitigate harmonic current while the VSC was connected to the grid voltage. Moreover, the injected harmonic current is caused by the dead time in the IGBT or MOSFET switch of the VSC [13]. The proportional resonance controller (PR controller) was widely used to eliminate harmonic currents [6, 13-18] where the PR controller was used to attain zero steady-state error [19]. The PR controllers are used for the control of both the single-phase system [20, 21] and the three-phase system [22]. Also, the PR controller was used in parallel on the stationary frame ($\alpha\beta$ – axis) [23] and the synchronous frame or called rotating referent frame (dq-axis) [14]. Meanwhile, the injected harmonic current will be responding to grid frequency adaptability while the current control loop contains the HCs. Therefore, the harmonic current has a high-order harmonic current when the frequency moves away from the nominal grid frequency [23].

As a result, this study explained the VSC's mitigation harmonic current when connected to the grid, as well as analyzed and evaluated the performance of the HCs in each technique under grid voltage distortion. Also, to analyze and construct the prototype of a two-level three-phase VSC using an LCL filter. The goal is to develop a suitable technique for removing harmonic currents. Then this study presented the simulation results and experimental results to confirm the concepts.

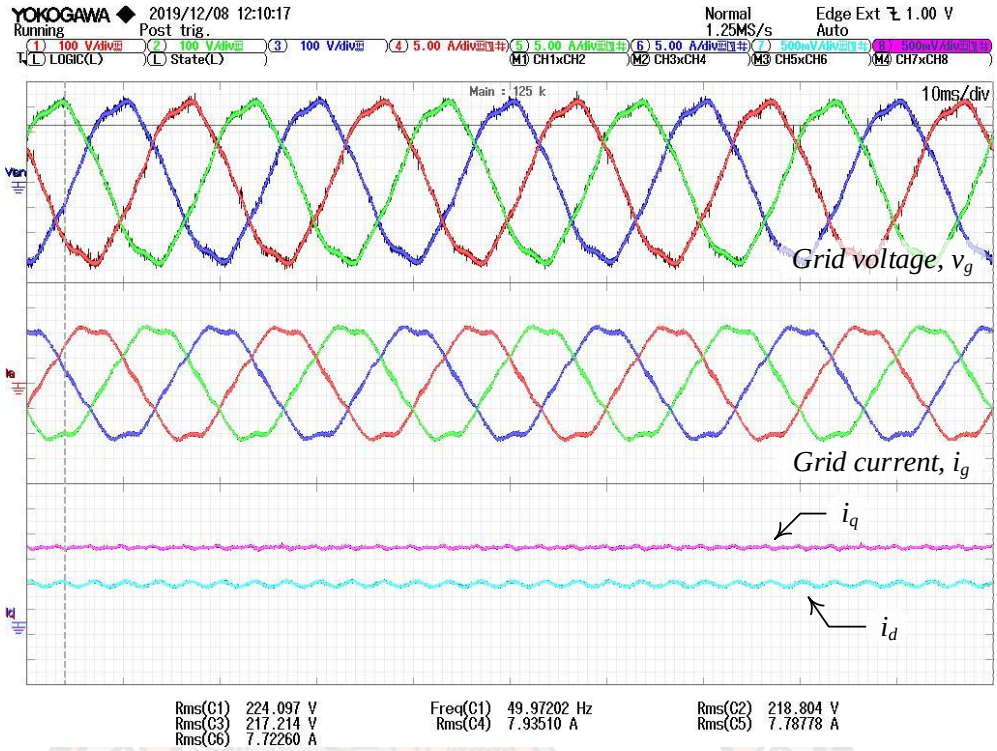


Figure 2 Grid current waveforms under a distorted grid voltage condition.

Objectives of the study

1) Design and construction of a two-level voltage source converter connected to the grid with an LCL filter.
2) To develop a grid current control scheme for harmonic mitigation under grid voltage distortion.
3) To evaluate the harmonic compensations (HCs) in each technique under grid voltage distortion.

Scope of the Study

1) The two-level voltage source converter has the following characteristic as Table 1.
2) The two-level VSC can be maintained when the grid is weak, such as harmonic of grid voltage.
3) The two-level VSC contained harmonic compensations (HCs) in the grid current control loop under IEEE 1547-2018 requirement.
4) The two-level VSC can be controlled the bi-directional power flow.

5) The diagram scope of the two-level voltage source inverter in this research is shown in Figure 3.

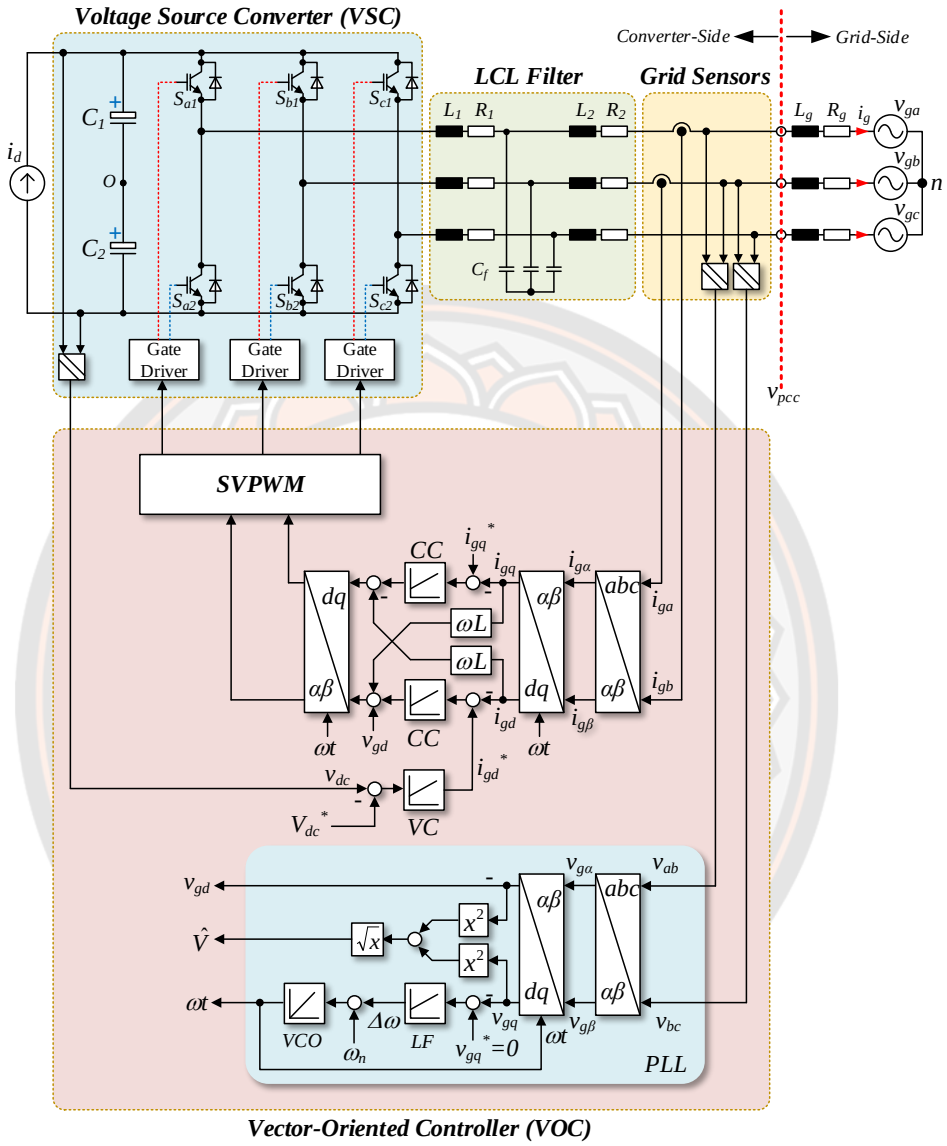


Figure 3 Three-phase grid-connected two-level voltage source converter with an LCL filter and control scheme.

Table 1 The two-level voltage source converter parameter.

Symbol	Parameters	Values
V_g	Nominal Grid Voltage	220/380 V
f_n	Nominal Grid frequency	50 Hz
P_{rated}	Rated Power	5 kW
I_g	Rated AC Current	7.59 A
V_{dc}	Nominal DC Bus Voltage	650 V
f_{sw}	Switching Frequency	10 kHz
f_s	Sampling Frequency	20 kHz
	PWM Technique	Space Vector PWM
	Filter type	LCL

Benefits of the Study

1) The VSC can be maintained when the grid voltage has high distortion, while the grid current has low distortion.
2) In a microgrid system, the grid current distortion remains low even when there is a variation in grid frequency.
3) Active and reactive power can be exchanged from or to the grid according to the necessity of the grid voltage.
4) The grid voltage profile can be improved with the proper injection of active power from renewable energy sources or storage devices, or without anything.
5) Implementing an effective control strategy for VSC and LCL parameters can significantly reduce grid current and grid voltage ripples. This also contributes to enhancing the power factor of the grid.
6) The current and voltage harmonics have been sufficiently decreased within the limitations specified by international standards, resulting in a low total harmonic distortion (THD).
7) The VSC is an important infrastructure of the smart grid system because it can control the grid's power flow to ensure proper energy management.

CHAPTER II

LITERATURE REVIEW

Review of related articles

The VSC is usually controlled to feed currents with low-order harmonics in compliance with standards such as IEEE 1547-2018 [12]. However, grid voltage harmonics are the disturbances of the VSC's grid current control loop, which distort the VSC currents injected into the grid. Furthermore, the grid current harmonics become more pronounced when the frequency deviates from the nominal grid frequency [23, 24]. Thus, harmonic current (HC) controllers with a frequency adaptation capability are essential for the VSC operated under grid voltage distortion. Proportional–integral (PI) regulators implemented on the synchronous reference frame are widely employed in the VSC current control thanks to the zero-steady state error, power decoupled capability, and adaptation with the inherent grid frequency through the axis transformations [15, 17, 25, 26]. However, the grid current waveforms distort when the grid voltages contain harmonic components. Therefore, integral regulators on the multiple synchronous reference frames at selective harmonic frequencies implemented in parallel with the fundamental controller successfully attenuate the grid voltage harmonics [27, 28]. This multiple synchronous reference frame control is herein called the PIMSR control, which has been reported in the active power filter [27, 29-33], grid-forming inverter [34], and grid-connected inverter applications [35, 36]. However, the PIMSR control requires a large number of axis transformations, which poses a heavy computational burden on a digital signal processor (DSP) [27, 35]. Proportional-resonant (PR) regulators implemented on the stationary reference frame are also widely employed in the VSC current control loop, which provides a zero steady-state error [14, 37-39]. The PR controllers are used for the control of both the single-phase system and the three-phase system [6, 14, 23]. This stationary frame PR control demands a low computation resource. The PR regulator has to be implemented with a damping coefficient to maintain the control performance with the variable grid frequency [40]. Therefore, the resonant regulator

with the double integrator structure is adopted to adapt the resonant frequency with the grid frequency employing the estimated frequency from the phased-locked loop (PLL) [41-43]. However, the current components in the stationary frame with the PR control lack the instantaneous active and reactive power extraction capability, which requires an additional power calculation scheme. Selective harmonic mitigation is achieved by adding multiple resonant controllers in parallel with the fundamental component controller, which is herein called the proportional-multiple-resonant (PMR) controller. A repetitive controller (RC) based on the internal model principle is another stationary reference frame controller suitable for periodic signals. The RC controller is equivalent to a set of multiple resonant regulators, which has been applied for the single-phase and three-phase VSCs [13, 23, 44]. However, frequency adaptation capability is the main drawback of the RC regulator. Therefore, complicated measures such as multi-rate sampling techniques or using Lagrange interpolating-polynomial-based filters have been proposed for the RC regulator [23].

Proportional–integral plus multi-resonant (PIMR) controllers implemented on the synchronous reference frame were proposed in [14]. The PI controllers in the dq-frame regulate the fundamental component currents. Meanwhile, the harmonic components ($1\pm h$) in the stationary reference frame are translated to orders $\pm h$ in the synchronous reference frame, where $h = 6, 12, \cdots$. Each resonant controller regulates the input signal both in the positive and negative sequences. Therefore, the PIMR control scheme employs a smaller number of resonant regulators than the PMR scheme on the stationary reference frame. Moreover, the power decoupling property is preserved due to the implementation in the synchronous reference frame. The frequency adaptation capability is also maintained if the resonant controllers are implemented with the double-integrator structure.

Liu et al. have proposed a solution for the weak grid in a micro-grid power system, where the background harmonic voltage (BHV) may distort the injected currents of the grid-tied inverters. They have presented a single-loop current control with the active damping (AD) method, a PR+HC regulator, and a hybrid damper. Liu et al. have proposed a solution for the weak grid in a micro-grid power system, where the background harmonic voltage (BHV) may distort the injected currents of the grid-tied inverters. They have presented a single-loop current control with the active

damping (AD) method, a PR+HC regulator, and a hybrid damper. This scheme is depicted in Figure 4. They have shown their work on single-phase LCL- or LLCL-filter-based grid-tied inverters. Experiments on a 2-kW prototype [16]. But this method is complicated because it adds a notch filter in the current control loop as well as an extra damper inserted to keep the system stable.

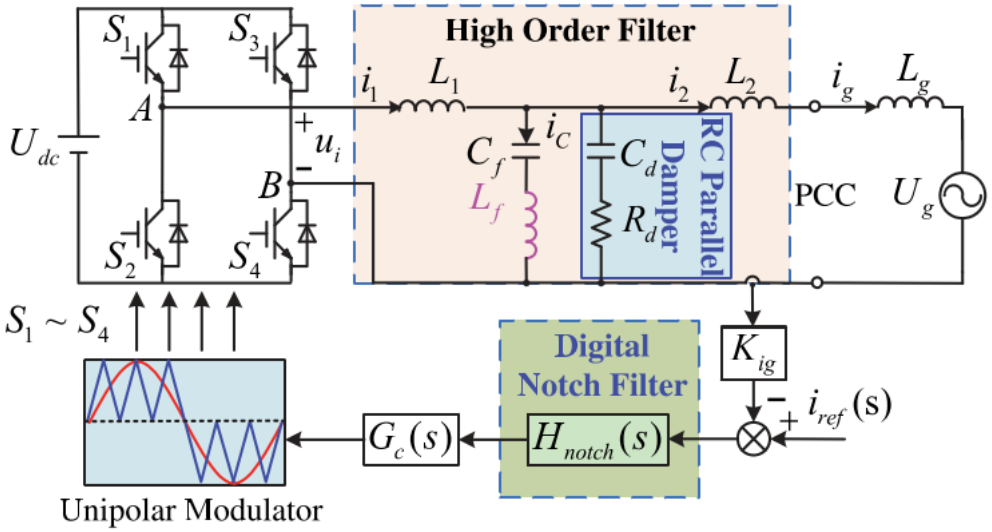


Figure 4 The single-loop current control with active damping (AD) method, PR+HC regulator, and a hybrid damper [16].

Shen et al., have presented a feedback method for PR current control of LCL-filter-based grid-connected inverter that measured the currents of two inductors of the an LCL-filter and the weighted average value of the currents for the current PR regulator. They named this method "*the weighted average of the inverter current and the grid current*" (WAC). Therefore, the control system is reduced from a third-order function to a first-order one. A large proportional control-loop gain can be chosen to obtain a wide control-loop bandwidth, and the system can be optimized easily for minimum current harmonic distortions, as well as system stability. The inverter system with the proposed controller is investigated and compared with those using traditional control methods. Experimental results on a 5-kW fuel-cell inverter is provided [20]. But if used in this method, the current injected into the grid cannot be directly regulated because the current control loop will not receive a direct current signal from the sensor. Which may cause the current to be highly distorted.

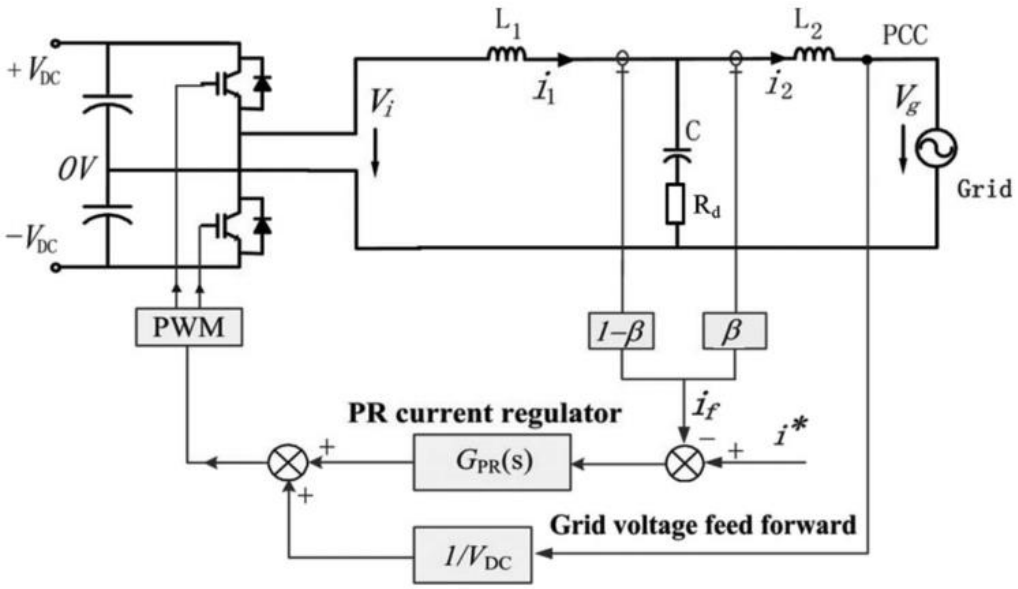


Figure 5 The weighted average of the inverter current and the grid current [20].

Xin et al. have presented mitigation of grid-current distortion for an LCL-filtered voltage-source inverter with inverter-current feedback (ICF) control. With their system consisting of the HCs used as PR controllers, the inverter-current feedback controller is in $\alpha\beta$- frame. The highlight of their work, the capacitor current can be measured via capacitor voltage and controlled by the resonant HCs controllers. To compensate for the current distortion due to the grid-voltage distortion. It is shown in Figure 6. Also, they explained the problems caused by harmonic voltage distortion, which causes high current distortion when used grid current feedback control[11]. This research is complicated due to not possible to eliminate distorted currents directly. Consequently, the grid currents still have minor distortion.

Milczarek et al. have presented effective and simple control of a grid-connected three-phase converter operating at a strongly distorted voltage. They have proposed ways to mitigate grid current distortions caused by grid-voltage harmonics. They used the notch filtered grid voltage as a feedforward to compensate for the output of the current control loop at the stationary frame ($\alpha\beta$- frame) [45]. The scheme of their work has been shown in Figure 7. The following methods can not

eliminate harmonic current cleanly. As it does not eliminate the current directly in the current control loop.

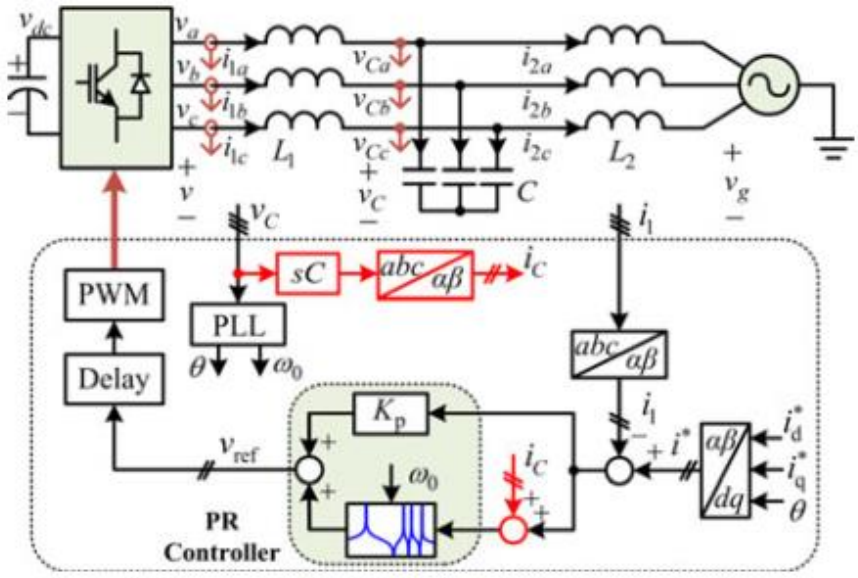


Figure 6 Three-phase VSC with the capacitor current compensation in the resonant HCs controllers[11].

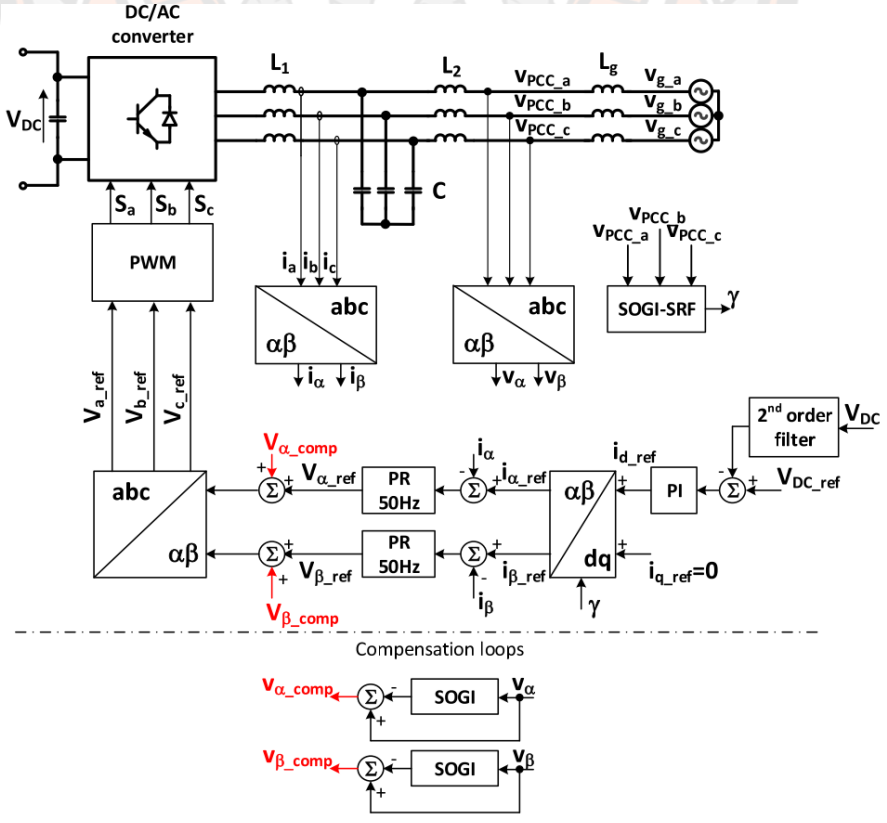


Figure 7 The notch filtered grid voltage feedforward is used to compensate for the output of the current control loop at the stationary frame [45].

This work evaluates the implementation and control performance of the PIMR controllers on the synchronous reference frame for current control of the three-phase grid-connected LCL-filtered VSC under grid voltage distortion and grid frequency variation, as shown in Figure 3. Controller design, stability analysis, and discrete-time implementation are elaborated. The PIMR control scheme was compared with the conventional PIMSR control method. The two control schemes were both implemented on a 32-bit TMS320F28379D microcontroller. The computational burdens of the two control schemes on the TMS320F28379D microcontroller were estimated. A hardware-in-the-loop (HiL) real-time simulator and a 5-kVA insulated-gate bipolar transistor (IGBT) VSC validated the performance of the PIMR and PIMSR control systems.

CHAPTER III

THREE-PHASE GRID-CONNECTED LCL-FILTERED VSC

Modeling of the LCL-filtered VSC

Switched circuit modeling of the power circuit

Figure 8 displays the equivalent circuit of the VSC. Resistors R_1 and R_2 are the winding resistance of the inductors L_1 and L_2. Resistors R_f are the equivalent series resistance of the capacitors C_f plus the series damping resistance of the LCL filter. Resistor R_D is the effective DC bus capacitance of the DC bus voltage sensor and the discharging resistor. The semiconductor switches are represented by switches S_a, S_b, and S_c. The status of each switch is represented by "1" for the closed state and "0" for the opened state. The complementary switches $\bar{S}_a$, $\bar{S}_b$, and $\bar{S}_c$ operate opposite S_a, S_b, and S_c. Therefore, there are 8 possible output states of the VSC. There are 3 reference points: m, n, and o. The DC bus current i_o is supplied or drawn by another converter which is positive for the inverting mode and negative for the rectifying mode.

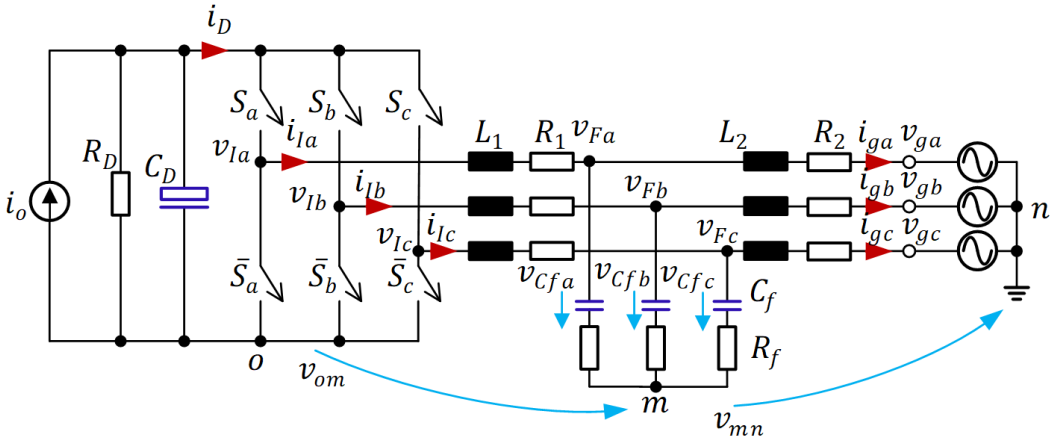


Figure 8 Equivalent circuit of the 3-phase grid-connected VSC with the LCL filter.

The grid currents i_{ga}, i_{gb} and i_{gc} can be written as follows

$$\left.\begin{aligned} L_2\frac{di_{ga}}{dt} &= \left(v_{Fa,m}+v_{mn}\right)-v_{ga,n}-R_2 i_{ga} \\ L_2\frac{di_{gb}}{dt} &= \left(v_{Fb,m}+v_{mn}\right)-v_{gb,n}-R_2 i_{gb} \\ L_2\frac{di_{gc}}{dt} &= \left(v_{Fc,m}+v_{mn}\right)-v_{gc,n}-R_2 i_{gc} \end{aligned}\right\} \quad (1)$$

where $v_{Fa,m}$, $v_{Fb,m}$ and $v_{Fc,m}$ are the voltages across the filter capacitor C_f and the series resistor R_f with respect to point m, which are given by

$$\left.\begin{aligned} v_{Fa,m} &= v_{Cfa}+R_f(i_{ga}-i_{Ia}) \\ v_{Fb,m} &= v_{Cfb}+R_f(i_{gb}-i_{Ib}) \\ v_{Fc,m} &= v_{Cfc}+R_f(i_{gc}-i_{Ic}) \end{aligned}\right\} \quad (2)$$

The voltages across the filter capacitor C_f, v_{Cfa}, v_{Cfb} and v_{Cfc} are determined from

$$\left.\begin{aligned} C_f\frac{dv_{Cfa}}{dt} &= i_{ga}-i_{Ia} \\ C_f\frac{dv_{Cfb}}{dt} &= i_{gb}-i_{Ib} \\ C_f\frac{dv_{Cfc}}{dt} &= i_{gc}-i_{Ic} \end{aligned}\right\} \quad (3)$$

The VSC currents i_{Ia}, i_{Ib} and i_{Ic} are given by

$$\left.\begin{aligned} L_1\frac{di_{Ia}}{dt} &= \underbrace{\left(v_{Ia,o}+v_{om}\right)}_{v_{Ia,m}}-v_{Fa,m}-R_1 i_{Ia} \\ L_1\frac{di_{Ib}}{dt} &= \underbrace{\left(v_{Ib,o}+v_{om}\right)}_{v_{Ib,m}}-v_{Fb,m}-R_1 i_{Ib} \\ L_1\frac{di_{Ic}}{dt} &= \underbrace{\left(v_{Ic,o}+v_{om}\right)}_{v_{Ic,m}}-v_{Fc,m}-R_1 i_{Ic} \end{aligned}\right\} \quad (4)$$

where the VSC voltages $v_{Ia,o}$, $v_{Ib,o}$ and $v_{Ic,o}$ with respect to point o depends on the switching states as follows

$$\left.\begin{aligned} v_{Ia,o} &= S_a v_D \\ v_{Ib,o} &= S_b v_D \\ v_{Ic,o} &= S_c v_D \end{aligned}\right\} \quad (5)$$

For the balanced 3-phase 3-wire system, $v_{ga,n}+v_{gb,n}+v_{gc,n}=0$, $v_{Fa,m}+v_{Fb,m}+v_{Fc,m}=0$, $i_{ga}+i_{gb}+i_{gc}=0$ and $i_{Ia}+i_{Ib}+i_{Ic}=0$, which results in

$$v_{mn}=0 \quad (6)$$

Thus, the grid currents can be written as follows

$$\left.\begin{aligned} L_2\frac{di_{ga}}{dt} &= v_{Fa,m} - v_{ga,n} - R_2 i_{ga} \\ L_2\frac{di_{gb}}{dt} &= v_{Fb,m} - v_{gb,n} - R_2 i_{gb} \\ L_2\frac{di_{gc}}{dt} &= v_{Fc,m} - v_{gc,n} - R_2 i_{gc} \end{aligned}\right\} \tag{7}$$

Adding the sub-equations of (4) together, the common mode voltage v_{om} is expressed as

$$v_{om} = -\frac{v_D}{3}(S_a + S_b + S_c) \tag{8}$$

This common-mode voltage v_{om} intrinsically exists in the 2-level VSC due to limited switching states, which creates a leakage current through the parasitic capacitance between the DC bus and the neutral points of the system. The VSC currents i_{Ia}, i_{Ib}, and i_{Ic} are driven by the differential mode voltages $v_{Ia,m}$, $v_{Ib,m}$, and $v_{Ic,m}$ between the VSC legs and the neutral point m of the capacitor bank, which can be written as

$$\left.\begin{aligned} L_1\frac{di_{Ia}}{dt} &= \underbrace{v_D(2S_a - S_b - S_c)/3}_{v_{Ia,m}} + v_{Fc,m} - R_1 i_{Ia} \\ L_1\frac{di_{Ib}}{dt} &= \underbrace{v_D(2S_b - S_a - S_c)/3}_{v_{Ib,m}} + v_{Fb,m} - R_1 i_{Ib} \\ L_1\frac{di_{Ic}}{dt} &= \underbrace{v_D(2S_c - S_a - S_c)/3}_{v_{Ic,m}} + v_{Fc,m} - R_1 i_{Ic} \end{aligned}\right\}. \tag{9}$$

The VSC DC current i_D is written as

$$i_D = i_{Ia}S_a + i_{Ib}S_b + i_{Ic}S_c. \tag{10}$$

If the DC bus is connected to another converter buffered by the DC bus capacitor C_D, the DC bus voltage v_D is then modeled as

$$C_D\frac{dv_D}{dt} = i_o - i_D - \frac{v_D}{R_D}. \tag{11}$$

Figure 9(a) displays the VSC and LCL filter model developed in the MATLAB/Simulink environment, where (2), (3), (7), (9), and (10) are implemented. This model is valid for the DC bus voltage is greater than the peak value of the line-to-line grid voltage $\hat{V}_{LL}$. The signal EN is used for the enable ($EN = 1$) and disable ($EN = 0$) VSC operation. If the VSC is disabled and $v_D \geq \hat{V}_{LL}$, the VSC currents i_{Ia}, i_{Ib}, and i_{Ic} are kept reset at zero. Meanwhile, the grid currents i_{ga}, i_{gb}, and i_{gc} circulate through L_2, R_2, C_f, and R_f. At the enable time t_{EN}, the switching signals S_a,

S_b, and S_c are enabled and the VSC is fully operated. Figure 9(b) shows the MATLAB/Simulink model of the DC bus voltage v_D in (11), which is kept reset while the VSC is disabled. For the single-stage topology where the VSC is connected to a constant voltage source, the DC bus voltage equation in (10) is neglected.

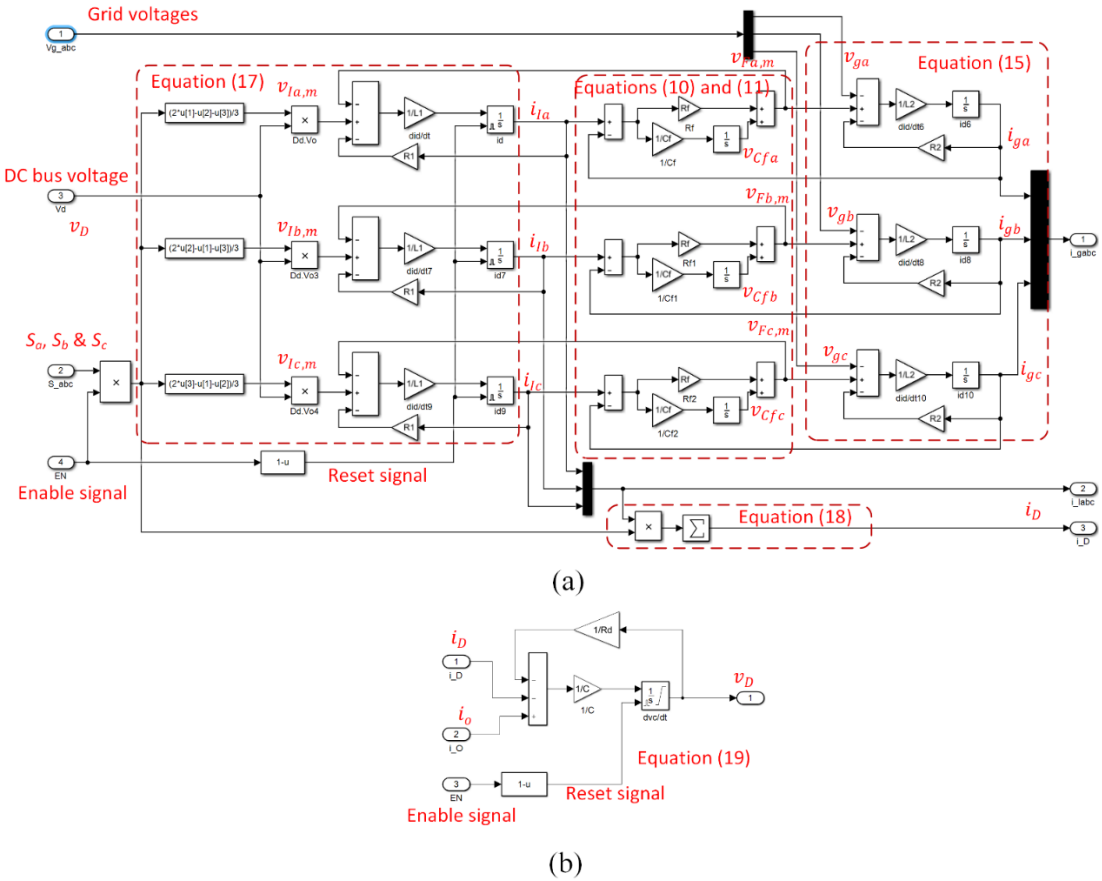


Figure 9 MATLAB/Simulink model: (a) the VSC and LCL filter, (b) the DC bus voltage

Averaged circuit modeling

The frequency response of the LCL filter below its resonant frequency is similar to that of the L filter [46]. Moreover, the control bandwidth is selected below the resonant frequency of the LCL filter. Thus, the LCL filter can be approximated as the L filter for design of the current controller. The grid currents can be simplified as

$$\left.\begin{aligned} L_t\frac{di_{ga}}{dt} + R_t i_{ga} &= v_{Ia,n} - v_{ga,n} \\ L_t\frac{di_{gb}}{dt} + R_t i_{gb} &= v_{Ib,n} - v_{gb,n} \\ L_t\frac{di_{gc}}{dt} + R_t i_{gc} &= v_{Ic,n} - v_{gc,n} \end{aligned}\right\} \quad (12)$$

, where $L_t = L_1 + L_2$, $R_t = R_1 + R_2$. The VSC voltages are written by

$$\begin{bmatrix} v_{Ia,n} \\ v_{Ib,n} \\ v_{Ic,n} \end{bmatrix} = \begin{bmatrix} v_{Ia,m} \\ v_{Ib,m} \\ v_{Ic,m} \end{bmatrix} + v_{mn} \quad (13)$$

According to (6) $v_{mn} = 0$, the grid currents in (12) become

$$\left.\begin{aligned} L_t\frac{di_{ga}}{dt} + R_t i_{ga} &= v_{Ia,m} - v_{ga,n} \\ L_t\frac{di_{gb}}{dt} + R_t i_{gb} &= v_{Ib,m} - v_{gb,n} \\ L_t\frac{di_{gc}}{dt} + R_t i_{gc} &= v_{Ic,m} - v_{gc,n} \end{aligned}\right\}. \quad (14)$$

The variables in (14) are averaged over a sampling period $T_s = f_s$ for continuous-time domain approximation, which becomes

$$\left.\begin{aligned} L_t\frac{d\langle i_{ga}\rangle}{dt} + R_t\langle i_{ga}\rangle &= \langle v_{Ia,m}\rangle - \langle v_{ga,n}\rangle \\ L_t\frac{d\langle i_{gb}\rangle}{dt} + R_t\langle i_{gb}\rangle &= \langle v_{Ib,m}\rangle - \langle v_{gb,n}\rangle \\ L_t\frac{d\langle i_{gc}\rangle}{dt} + R_t\langle i_{gc}\rangle &= \langle v_{Ic,m}\rangle - \langle v_{gc,n}\rangle \end{aligned}\right\} \quad (15)$$

where the brackets '⟨ ⟩' represent the variables averaged over T_s. Equation (15) is scaled into the per-unit scale using the base voltage $V_B = I_B Z_B$ where I_B is the base current and Z_B is the base impedance, which yields

$$\left.\begin{aligned} L'_t\frac{d\langle i'_{ga}\rangle}{dt} + R'_t\langle i'_{ga}\rangle &= \langle v'_{Ia,m}\rangle - \langle v'_{ga,n}\rangle \\ L'_t\frac{d\langle i'_{gb}\rangle}{dt} + R'_t\langle i'_{gb}\rangle &= \langle v'_{Ib,m}\rangle - \langle v'_{gb,n}\rangle \\ L'_t\frac{d\langle i'_{gc}\rangle}{dt} + R'_t\langle i'_{gc}\rangle &= \langle v'_{Ic,m}\rangle - \langle v'_{gc,n}\rangle \end{aligned}\right\} \quad (16)$$

where symbols ' ' denotes variables in the per-unit scale, and $L_t' = L_t/Z_B$ and $R_t' = R_t/Z_B$. The grid currents in (16) are transformed to the synchronous reference frame, dq axes, which results in

$$\left.\begin{aligned} L_t' \frac{d\langle i_{gd}' \rangle}{dt} + R_t' \langle i_{gd}' \rangle &= \langle v_{Id}' \rangle - \hat{V}_g' + \underbrace{\omega L_t'}_{K_{FW}} \langle i_{gq}' \rangle \\ L_t' \frac{d\langle i_{gq}' \rangle}{dt} + R_t' \langle i_{gq}' \rangle &= \langle v_{Iq}' \rangle + \underbrace{\omega L_t'}_{K_{FW}} \langle i_{gd}' \rangle \end{aligned}\right\}. \quad (17)$$

Figure 10 shows the equivalent control block diagram of the grid current in the synchronous reference frame with the per-unit scale. Notes that the cross-coupling terms $K_{FW} = \omega L_t'$ are due to the Park transformation, which can be decoupled in the control scheme. The delay terms e^{-sT_d} represent the sampling delay caused by the digital control scheme and the transport delay caused by the PWM process, where $T_d = T_{sw}$ for the double update rate PWM shown in Figure 16 [47].

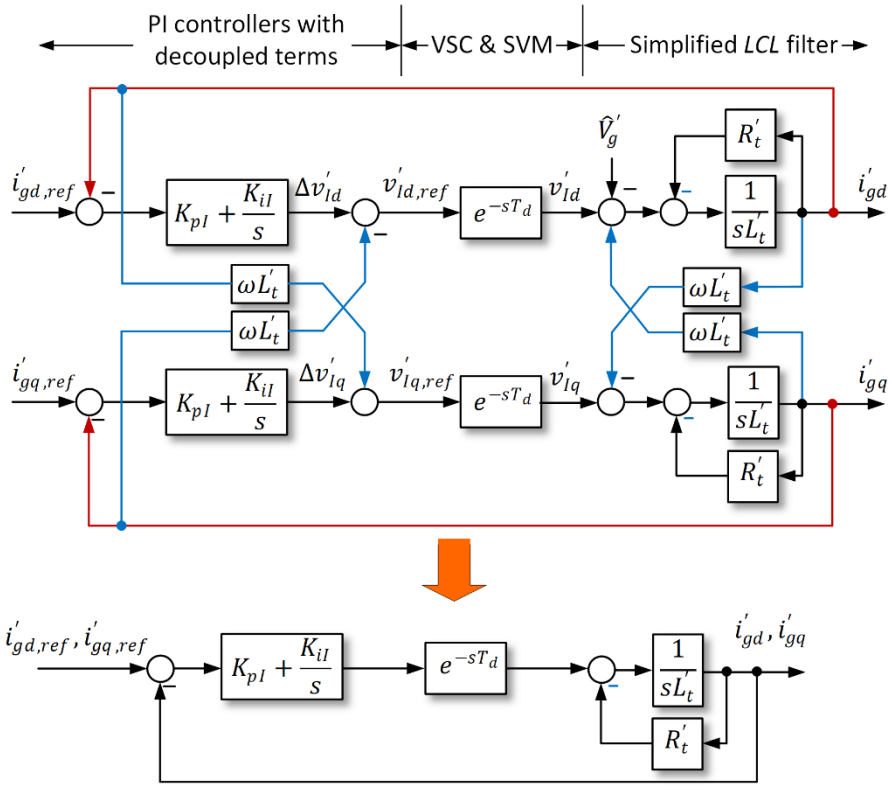


Figure 10 Equivalent block diagram of the grid current in the synchronous reference frame.

Analysis of LCL-filter

The power circuit of a three-phase two-level voltage source converter with an LCL filter is shown in Figure 8. The ac side of the converter is connected to the point of common coupling (PCC) via an LCL filter. Its equivalent single-phase circuit with resistive parasitic is shown in Figure 11(a), where v_c is the converter voltage, v_{pcc} is the PCC voltage and v_g is the grid voltage, i_I is converter current and i_g is grid current. The converter side inductor L_1, grid side inductor L_2 and filter capacitor C_f are components of the LCL filter. Also, R_1, R_2 and R_f are the parasitic resistance of the LCL filter, L_g and R_g are the parasitic impedance of the gird, which depends on the distance between the converter and the source as well as the cable size has a direct effect on the parasitic resistance of the gird.

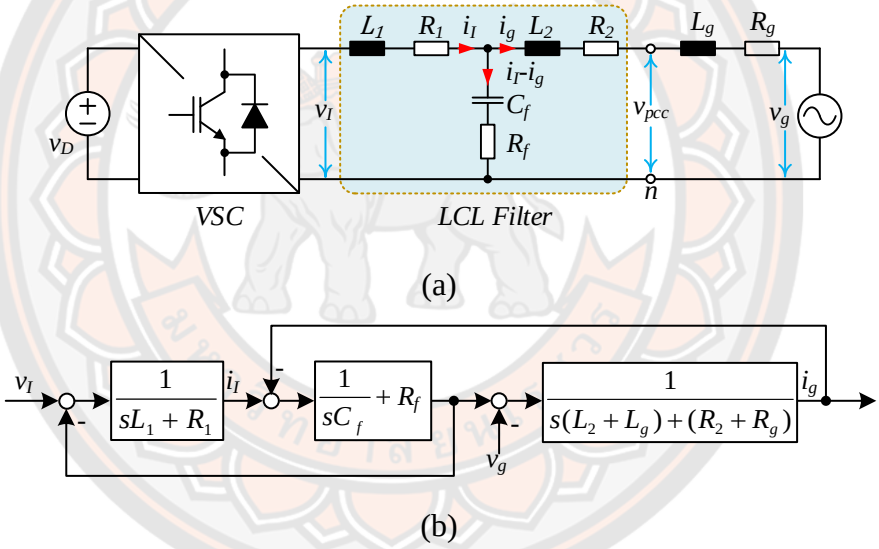


Figure 11 (a) The single-phase equivalent circuit of the LCL filter. (b) Open-loop block diagram of the LCL filter.

$$G_{LCL}(s) = \frac{i_g(s)}{v_I(s)} = \frac{1}{L_1 L_2 C_f s^3 + (L_1 + L_2)s} = \frac{1}{(L_1 + L_2)s} \cdot \frac{\omega_{LCL}^2}{s^2 + \omega_{LCL}^2} \qquad (18)$$

which is

$$\omega_{LCL} = \sqrt{\frac{L_1 + L_2}{L_1 + L_2 C_f}} \qquad (19)$$

or

$$f_{LCL} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 + L_2 C_f}} \tag{20}$$

where ω_{LCL}, and f_{LCL} are the resonance angular and resonance frequency, respectively. From (18) are the transfer functions of the LCL filter from the converter voltage to the grid current, which neglect the parasitic resistance and damping resistance, and can find the resonance angular and frequency from (19) and (20). And if considered, the parasitic resistance and damping resistance can be written as (21)

$$\frac{i_g(s)}{v_I(s)} = \frac{1 + C_f R_f}{L_1 L_2' C_f s^3 + C_f\left(L_1 R_2' + L_2' R_1 + L_t R_f\right)s^2 + \left(L_t + C_f\left(R_1 R_2' + R_f R_t\right)\right)s + R_t} \tag{21}$$

where $R_2' = R_2 + R_g$, $R_t = R_1 + R_2 + R_g$, $L_2' = L_2 + L_g$ and $L_t = L_1 + L_2 + L_g$.

The frequency response of the LCL filter is illustrated in Figure 12. It has shown a different LCL parameter with damping (21) and without damping (18). The resonance frequency f_{LCL} of both is equal, and the high-frequency attenuation slope is the same value (–60 dB/dec). But the LCL parameter without damping has a higher resonance peak than the LCL parameter with damping, and the slop at low-frequency range is different.

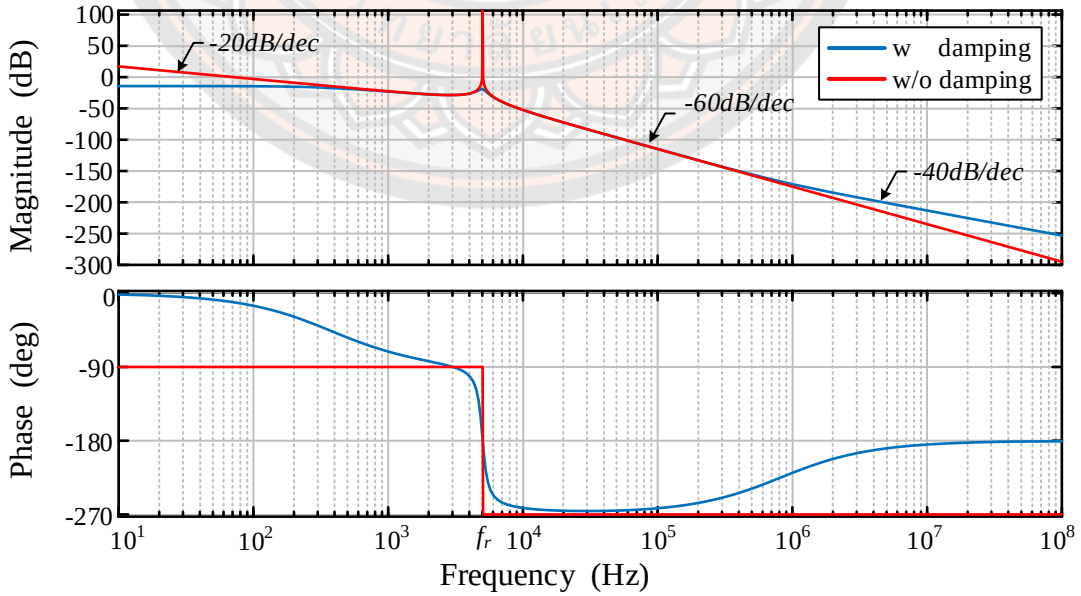


Figure 12 The frequency response of the LCL filter

Figure 13. depicts the behavior of the LCL filter when varying grid resistance R_g. It directly affects the resonance peak and the resonance frequency is not changing. But the high-frequency attenuation slope may change if the grid resistance has a large value and the resonance frequency may converge into the unstable region ($f_{LCL} < f_s/6$) [21, 48-50], where f_s is the sampling frequency.

Meanwhile, when changing the grid inductance of the LCL filter that is shown in Figure 14. The high-frequency attenuation slope is unaffected but the resonance frequency has changed if the grid inductance has a large value, it will cause the resonance frequency may converge into the unstable region ($f_{LCL} < f_s/6$). The parameter of the LCL filter in Figure 12., Figure 13. and Figure 14. shown in Table 2.

Table 2 The parameter of LCL filter

Parameters	**Values**	**Parameters**	**Values**
Converter -side inductance, L_1	1.4 mH	Winding resistance, R_1	0.11 Ω
Grid-side inductor, L_2	0.71 mH	Winding resistance, R_2	0.042 Ω
Grid inductance, L_g	1mH	Grid resistance, R_g	1 Ω
filter capacitor, C_f	1.94 μF	Series resistance R_f	0.001 Ω
Resonance frequency, f_{LCL}	4.95 kHz	$f_{LCL}$with grid parameter	5.17 kHz

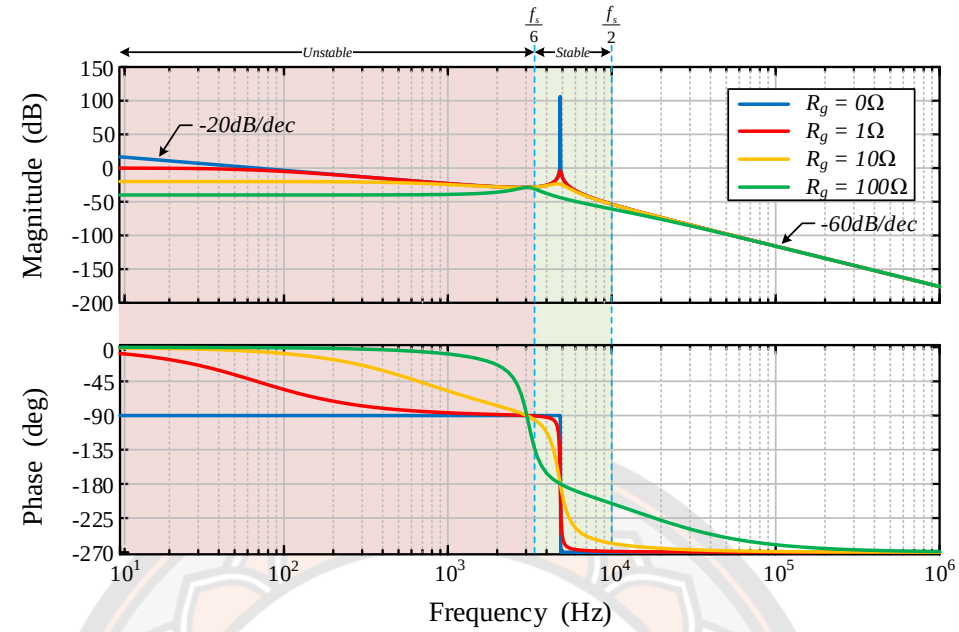


Figure 13 Bode plot of LCL-filters under different grid resistance

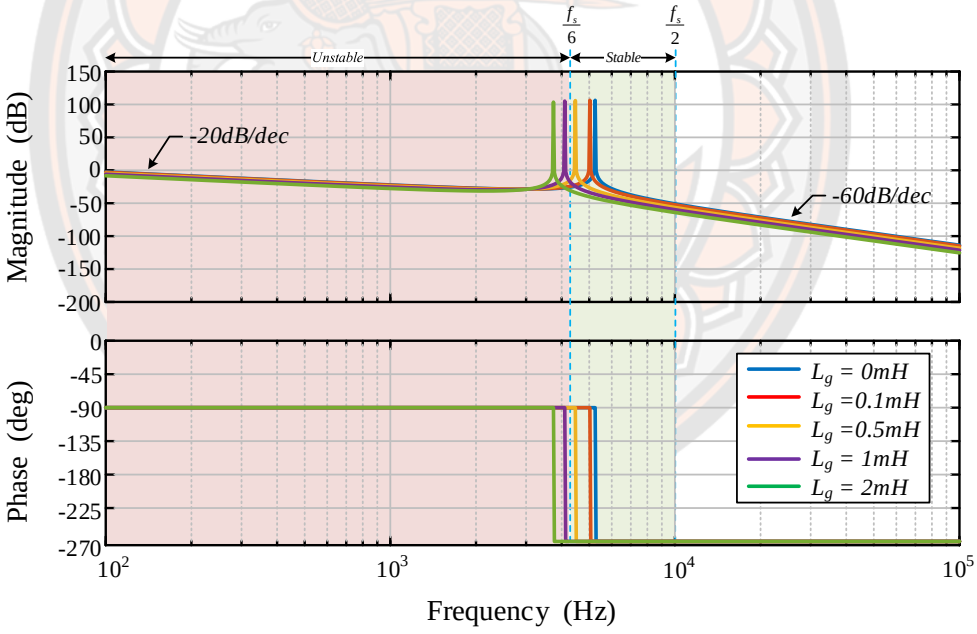


Figure 14 Bode plot of LCL-filters under different grid inductance

Grid voltage distortion

The distorted grid voltages v_{ga}, v_{gb} and v_{gc} are provided as follows:

$$\left.\begin{aligned} v_{ga}(t) &= \hat{V}_1 \cos\theta + \sum_{h}^{n} \hat{V}_k \cos h\theta \\ v_{gb}(t) &= \hat{V}_1 \cos(\theta - 2\pi/3) + \sum_{h}^{n} \hat{V}_k \cos h(\theta - 2\pi/3) \\ v_{gc}(t) &= \hat{V}_1 \cos(\theta + 2\pi/3) + \sum_{h}^{n} \hat{V}_k \cos h(\theta + 2\pi/3) \end{aligned}\right\} \quad (22)$$

where $\theta = \omega_g t$ and ω_g is the grid frequency. The three-phase three-wire (3P3W) system contains the harmonic orders $h = 5,7,11,13, \ldots$. Additional information is described in Appendix I. A phase-locked loop (PLL) is used to estimate the grid voltage angle $\hat{\theta}$ for the reference frame transformation. Simultaneously, it provides the peak value of the grid voltage $\hat{V}_g$. The grid voltage in the stationary reference frame is obtained from

$$\vec{v}_{\alpha\beta} = v_{g\alpha} + jv_{g\beta} = \frac{2}{3}\left(v_{ga} + v_{gb}e^{j\frac{2\pi}{3}} + v_{gb}e^{-j\frac{2\pi}{3}}\right). \quad (23)$$

Note that the zero sequence is neglected for the balanced system. Substituting (22) into (23), the grid voltage can be represented as

$$\vec{v}_{\alpha\beta} = \hat{V}_1 + \hat{V}_5 e^{-j5\theta} + \hat{V}_7 e^{j7\theta} + \hat{V}_{11} e^{-j11\theta} + \hat{V}_{13} e^{j13\theta} + \cdots \quad (24)$$

Thus, the grid voltage in the synchronous reference frame is given by

$$\vec{v}_{dq} = \vec{v}_{\alpha\beta} e^{-j\theta} = \hat{V}_1 + \hat{V}_5 e^{-j6\theta} + \hat{V}_7 e^{j6\theta} + \hat{V}_{11} e^{-j12\theta} + \hat{V}_{13} e^{j12\theta} + \cdots. \quad (25)$$

The voltage harmonic orders $\pm h = 6,12, \cdots$ in the synchronous reference frame result from the harmonic orders $(h \pm 1)$ in the stationary reference frame, which become the disturbances of the dq-axes current control loops.

The control of the VSC in discrete-time domain

The synchronous reference frame control is shown in Figure 15, which illustrates an LCL-filtered three-phase grid-connected voltage source converter. The voltages and currents from the power grid, as well as the voltage across DC bus, are converted from analog to digital format. Analog-to-digital (A/D) converters provide

this conversion. The digital values are modeled in simulations using zero-order hold (ZOH) blocks after conversion. The voltages are adjusted to the per-unit system using a scaling factor K_{SV}, while the currents are adjusted using a scaling factor K_{SI}.

The grid currents are converted to the synchronous reference frame, where the dq-axes current i'_{gd} and i'_{gq} are controlled by discrete-time current controllers $G_{ci}(z)$. The reference current $i'_{gd,ref}$ is determined by the active power control loop and/or the DC bus voltage control loop, while the reference current $i'_{gq,ref}$ is derived from the reactive power control loop or set to zero for a unity power factor.

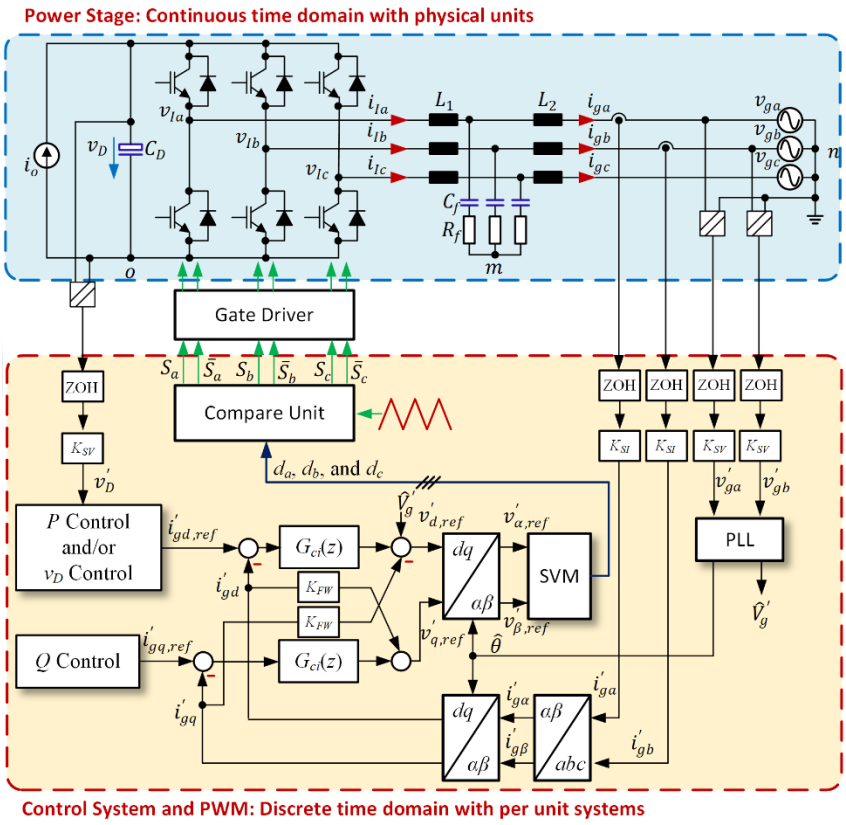


Figure 15 Three-phase grid-connected LCL-filtered VSC with the discrete-time control scheme in the synchronous reference frame

The outputs of the dq-axes current controllers with feedforward of the decoupled terms K_{FW} form the VSC reference voltages $v'_{d,ref}$ and $v'_{d,ref}$ which are converted to the stationary reference frame $v'_{\alpha,ref}$ and $v'_{\beta,ref}$ using the inverse Park transformation given by

$$\vec{v}'_{\alpha\beta,ref} = \left(v'_{\alpha,ref} + jv'_{\beta,ref}\right) = \left(v'_{d,ref} + jv'_{q,ref}\right) \cdot e^{j\theta}. \quad (26)$$

The reference voltages $v'_{\alpha,ref}$ and $v'_{\beta,ref}$ are the inputs for the space vector modulation (SVM) which calculates the duty ratios d_a, d_b and d_c for the compare unit to generate the VSC switching commands. The control scheme in Figure 15 is normally implemented on a DSP, and it must be executed within an interrupt service routine (ISR). Figure 16 illustrates the timing diagram of each ISR, which starts when the PWM carrier reaches zeros or the maxima. The analog signal sampling is synchronized with the ISR at time instance k that occurs in the middle of the switching action to avoid switching noise. This requires a small filtering effort for each signal, which enhances the control loop bandwidth. The analog-to-digital (A/D) conversion and scaling, and the PLL are executed every ISR. If the VSC operation is enabled, the other VSC control algorithms are performed; otherwise, they are skipped to the end of the ISR. The control scheme is executed within the sampling period T_s, and the calculated duty ratios $d_a(k)$, $d_b(k)$, and $d_c(k)$ are updated to the compare unit at the next time instance $k+1$.

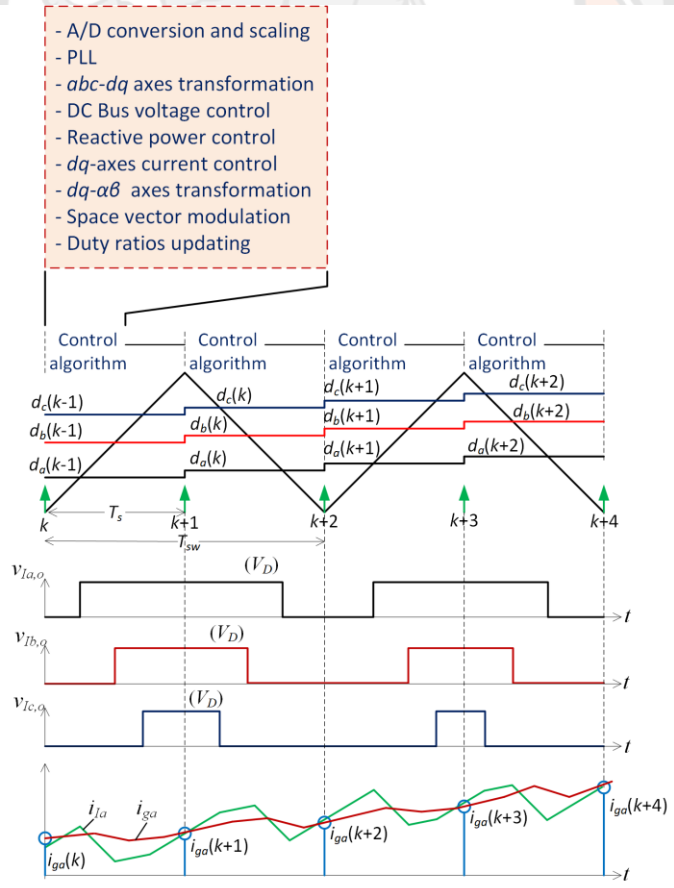


Figure 16 Timing diagram and control sequence of the VSC discrete-time control.

Simulation Structure

Figure 17 shows the simulation model developed in the MATLAB/Simulink environment. The simulation model emulates the experimental system, which is divided into two sections: the continuous-time domain and the discrete-time domain. The continuous-time domain represents the three-phase grid and the VSC power circuits with the switching signals S_a, S_b, and S_c as the inputs, where the switched-circuit model of the VSC and the LCL filter shown in Figure 9a are adopted. The single-stage topology is considered in this study, where the DC bus voltage is supplied by a constant voltage source V_D. The DC bus model in Figure 7b is neglected.

The discrete-time domain section emulates the control scheme depicted in Figure 3. The grid voltages v_{ga} and v_{gb}, and grid currents i_{ga} and i_{gb} are scaled by the base voltage V_B and base current I_B. Then, they are sampled by the ZOHs at the time instance k with the period of T_s. This process represents the beginning of each ISR as shown in Figure 5. The discrete-time algorithms for PLL, reference frame transformations, dq-axes current control, and the continuous SVM [51] are written in a MATLAB m file, which is executed every sampling period T_s by the interpreted MATLAB function block as shown in Figure10. The outputs of this interpreted MATLAB function block are the duty ratios $d_a(k)$, $d_b(k)$, and $d_c(k)$, which are delayed by T_s. This causes the duty ratios $d_a(k)$, $d_b(k)$, and $d_c(k)$ to be updated at the time instance $k+1$ to compare with the triangular waveform. This waveform has the switching period T_{sw} similar to that in Figure 5, which emulates the PWM process in the DSP. Thus, the controller parameters used in the simulation can be directly transferred to the experimental system if they use the same base units. The variable-step solver ODE45 with the maximum step size of $T_s/400 = 125$ ns was selected in the Simulink setting. The proposed simulation model developed in the MATLAB/Simulink 2020b is provided in [52].

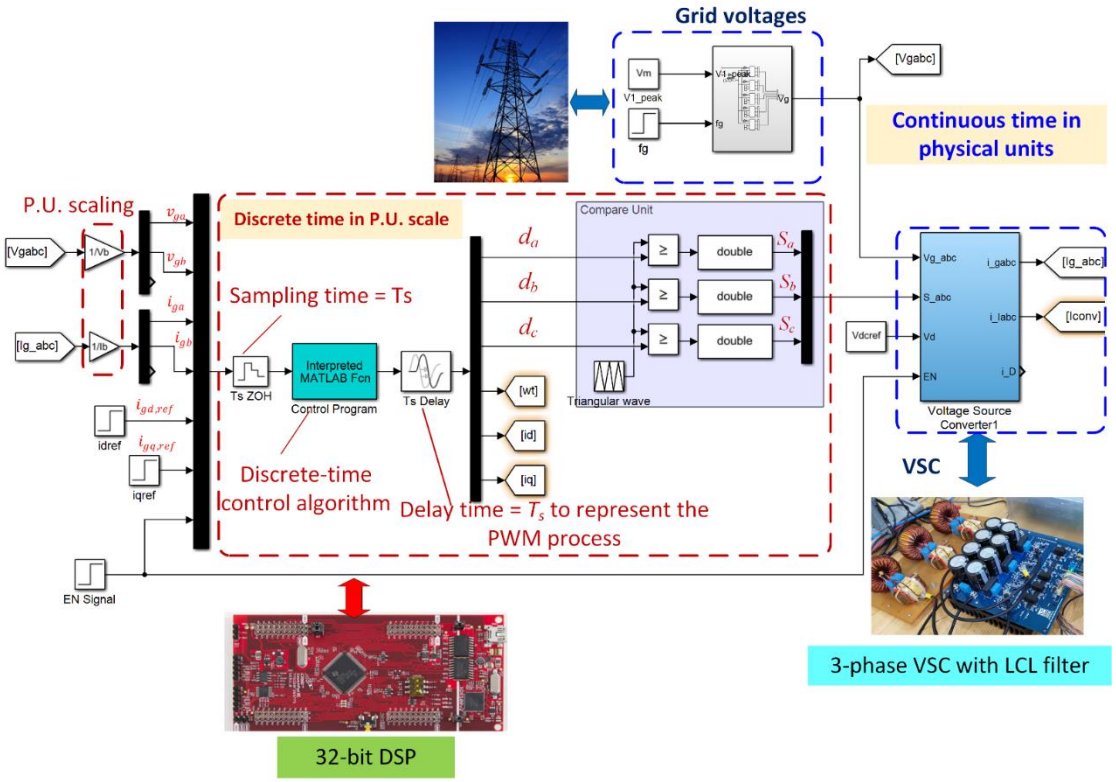


Figure 17 MATLAB/Simulink model of the discrete-time controlled 3-phase grid-connected VSC.

Discrete-Time Control Scheme

Figure 18 shows the Park-based PLL the discrete-time domain used for grid synchronization. The grid voltages v'_{ga}, v'_{gb}, and v'_{gc} are transformed to the $\alpha\beta$ axes using the Clarke transformation. The Park transformation converts the grid voltages to the dq axes, v'_{gd} and v'_{gq}, which are cleaned by the low-pass filters with the constant T_{PLL} for the distorted grid voltage. The integrator with a gain of the nominal grid frequency ω_{gn} estimates the grid voltage angle $\hat{\theta}$ for the Park transformation. The PI controller regulates the q-axis voltage v'_{gqf} toward zero, which forces $\hat{\theta} \cong \theta$, $\hat{\omega}' \cong \omega/\omega_{gn}$, and $v'_{gdf} \cong \hat{V}'_g$. The loop regulator is designed in the continuous-time domain using the symmetrical optimum (SO) method [53]. For simplicity, the low-pass filters and the PI regulators are discretized using the backward difference approximation because the sampling frequency is much greater than the PLL bandwidth. The coefficient for the low-pass filters in the discrete-time domain is given by

$$\alpha_{PLL} = \frac{T_s}{T_s + T_{PLL}} \tag{27}$$

The saturation limit on the PI regulator output with an anti-windup is implemented through the correction gain K_{cPLL} which is usually twice the integral gain K_{iPLL} [54]. Meanwhile, the integrator for estimation of the grid voltage angle $\hat{\theta}$ is discretized with the Tustin approximation with the lowest error. The estimated angle $\hat{\theta}$ is then used for the axis transformations.

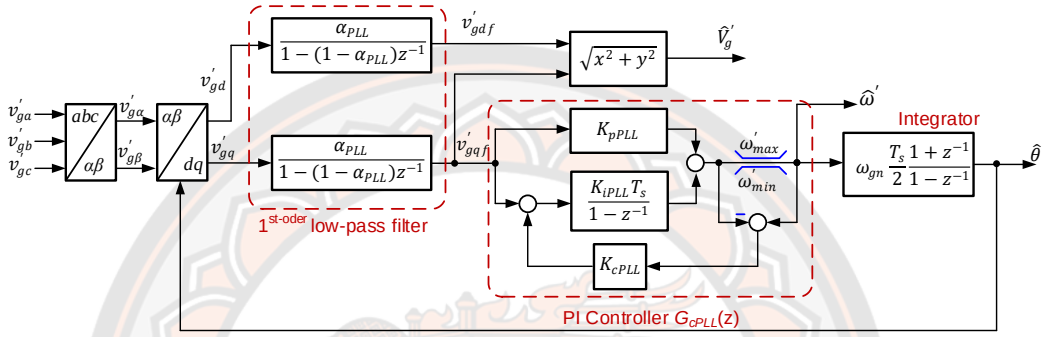
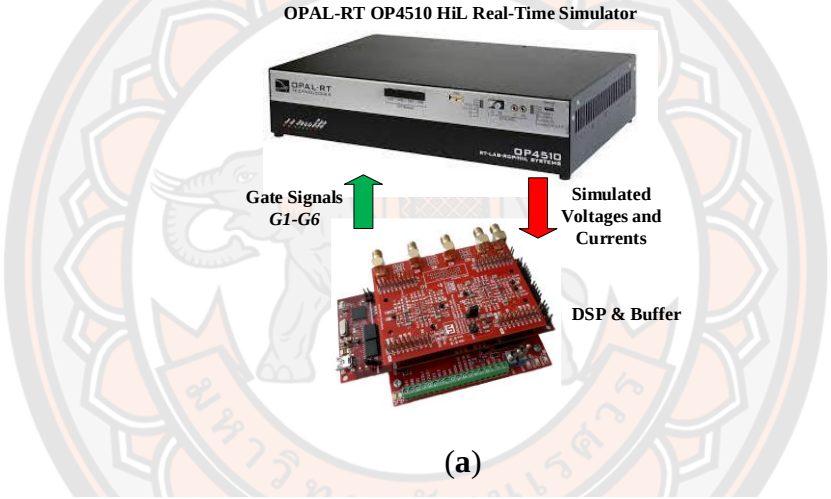


Figure 18 Park-based phase-locked loop in the discrete-time domain for grid synchronization.

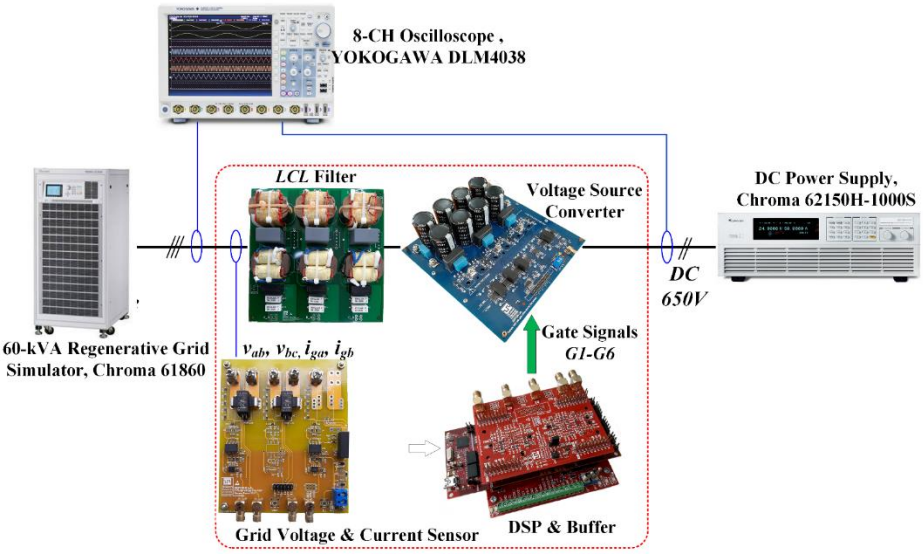
Implementations

Figure 19 illustrates the experimental system. The power circuit was firstly modeled in an OPAL-RT OP4510 HiL real-time simulator with a time step of 220 ns to validate the discrete-time control scheme, which was implemented on a Texas Instruments TMS320F28379D 32-bit DSP controller as shown in Figure 19a. The VSC parameters used for hardware-in-the-Loop (HiL) testing are listed in Table 3, which are the same parameters used in prototype hardware. The emulated grid voltages and currents in the HiL system had identical sensitivities to those used in the hardware implementation system, as depicted in Figure 19b. A deadtime of 1 μs in each VSC leg was configured in the DSP. The VSC was constructed from Infineon IKW25T120 insulated-gate bipolar transistors (IGBTs) with isolated gate drivers from Texas Instruments ISO5851. Amorphous C cores (AMCC6.3 equivalence) were used for the construction of the inductors L_1 and L_2 of the LCL filter. The VSC was connected to a Chroma 61,860 60-kVA grid simulator. The DC bus was supplied to a Chroma 62150H-1000S DC power supply, 15 kW 0–1000 V, for the inverter

operation. The discrete-time control scheme for the hardware implementation was identical to the HiL-based validation system. The ADC voltage range of this DSP is between 0 V to 3 V. Hall-effect current sensors, LEM HLSR 10-P/SP33, were used for measurement of the grid currents i_{ga} and i_{gb}. The grid voltage sensors were constructed from voltage divider circuits with AMC1200 isolation amplifiers. In this prototype, the line-to-line voltages v_{gab} and v_{gbc} were measured, of which the instantaneous voltage vector was shifted by $-pi/6$ to be in the same angle with the instantaneous voltage vector of the phase voltage vector. A voltage reference, REF2030, provided a 1.50 V offset voltage for the grid current and grid voltage sensors.



(**a**)



(**b**)

Figure 19 Experimental system of the three-phase VSC: (a) HiL-based implementation; (b) hardware implementation.

The measured voltages and currents were scaled into the per-unit system with the appropriate scaling factors, as illustrated in Figure 20. In this example, a grid current with the peak value of I_B is measured by a current sensor with the sensitivity of K_{Ti}. An offset voltage $V_{OF,i}$ is added to the sensor output to accommodate the 0-$V_{ADC,max}$ input range of the ADC, where $V_{ADC,max}$ is the maximum input voltage of the ADC, normally 3 V or 3.3 V. This translates to decimal values of 0 to $(2^{N_{ADC}} - 1)$, where N_{ADC} is the ADC bit number. The ADC output that is equivalent in decimal is then normalized by $2^{N_{ADC}}$. The offset is now equivalent to $V_{OF,i}/V_{ADC,max}$, which is subsequently removed in the software. The normalized signal with offset removal is multiplied by a scaling factor to have a unity amplitude at the base value. The numerical notation in the DSP can be in the signed fixed-point representation or the floating-point format. The scaling of the grid voltage has the same process as the grid current. No offset removal is required for the DC bus voltage, while the other procedures are similar to those for the grid voltage and current. In general, the signal scaling factor is given by

$$K_s = \frac{V_{ADC,max}}{(Sensor\ Senitivity) \times (Base\ Value)} \tag{28}$$

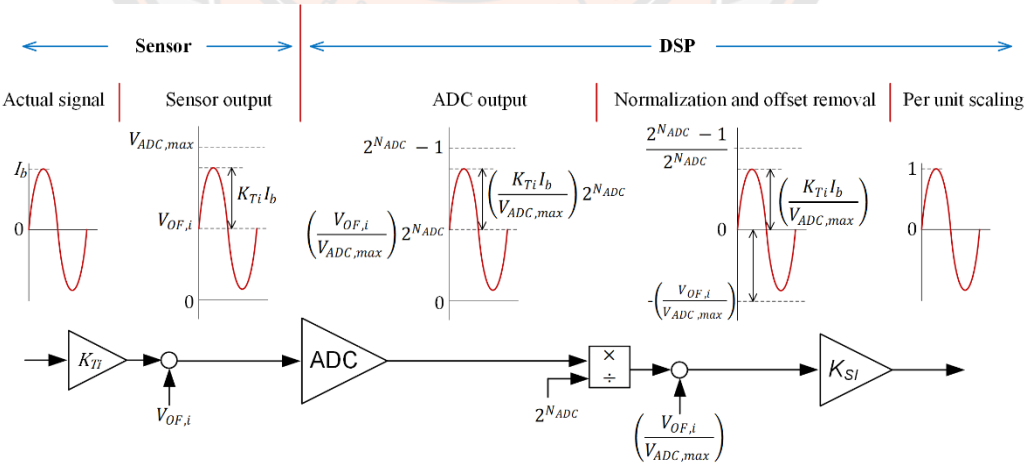


Figure 20 Grid current conversion and scaling process for the experimental system.

The discrete-time control algorithm implemented in the MATLAB m file was manually translated to the C language for the DSP with the same controller

parameters. Thus, the simulation and the experiment are closely related. However, there is a code generation tool for this DSP family with an additional licensing cost. The internal signals of the discrete-time control scheme implemented on the DSP were converted to 0–3.0 V analog signals via two embedded 12-bit digital-to-analog converters (DACs) for monitoring on an oscilloscope.

Table 3 Parameters of the VSC.

Parameters	**Value**
Nominal grid voltage	Three-phase 380 V line-line 50 Hz
Nominal power	5 kVA
Nominal DC bus voltage	650 V
DC bus capacitor, C_D	780 µF
Switching frequency, f_{sw}	10 kHz
Sampling frequency, f_s	20 kHz
DC bus resistor, R_D	94 kΩ
Converter-side inductor, L_1	1.4 mH
Winding resistance of L_1, R_1	0.110 Ω
Grid-side inductor, L_2	0.7 mH
Winding resistance of L_2, R_2	0.042 Ω
Filter capacitor, C_f	1.94 µF
Series resistor, R_f	0.001 Ω
Base voltage, V_B	311 V
Base current, I_B	10.74 A
Base impedance, Z_B	28.88 Ω

Simulation and Experimental Validations

The DC bus was connected to the Chroma 62150H-1000S DC power supply with $v_D = 700$ V. The grid voltage waveforms were set to be sinusoidal at the nominal phase voltage of 230 V, 50 Hz. The PI controllers for the fundamental

component were enabled without the harmonic compensators. The reference currents were set to $i'_{gd,ref} = 1.0$ p.u. and $i'_{gq,ref} = 0$ p.u.. This caused the VSC to inject an active power of 5 kW into the grid. A simulation platform 1 of the VSC was developed in the Simscape Electrical of the MATLAB/Simulink 2020b, which is provided in [52]. Figure 21 and Figure 22 compare the experiment and simulation results for the VSC-side currents i_{Ia}, i_{Ib}, and i_{Ic}, and the grid currents i_{ga}, i_{gb}, and i_{gc}. It can be observed the experimental VSC-side currents i_{Ia}, i_{Ib}, and i_{Ic} of the HiL and hardware implementations have the current envelopes due to the switching in close agreement with those of the proposed simulation method and the simulation platform 1. This confirms that the switched circuit modeling technique is applicable for the proposed platform. The waveforms of the experimental and simulation grid currents i_{ga}, i_{gb}, and i_{gc} are near sinusoidal as the LCL filter absorbs the switching current ripples.

Table 4 Line-neutral voltage harmonics.

V_1	V_5	V_7	V_{11}	V_{13}	**THD**
220 Vrms	4%	2%	1%	1%	4.69%

The voltage harmonics listed in Table 4 were added to the fundamental component, which resulted in a total harmonic distortion (THD) of 4.69%. Figure 23 shows the grid voltages and the grid currents without the harmonic compensators (HC). The experimental results from the HiL and hardware implementations closely agree with the proposed simulation method and simulation platform 1. The grid voltage harmonics make the grid currents even more distorted, with a THD of 10.84%.

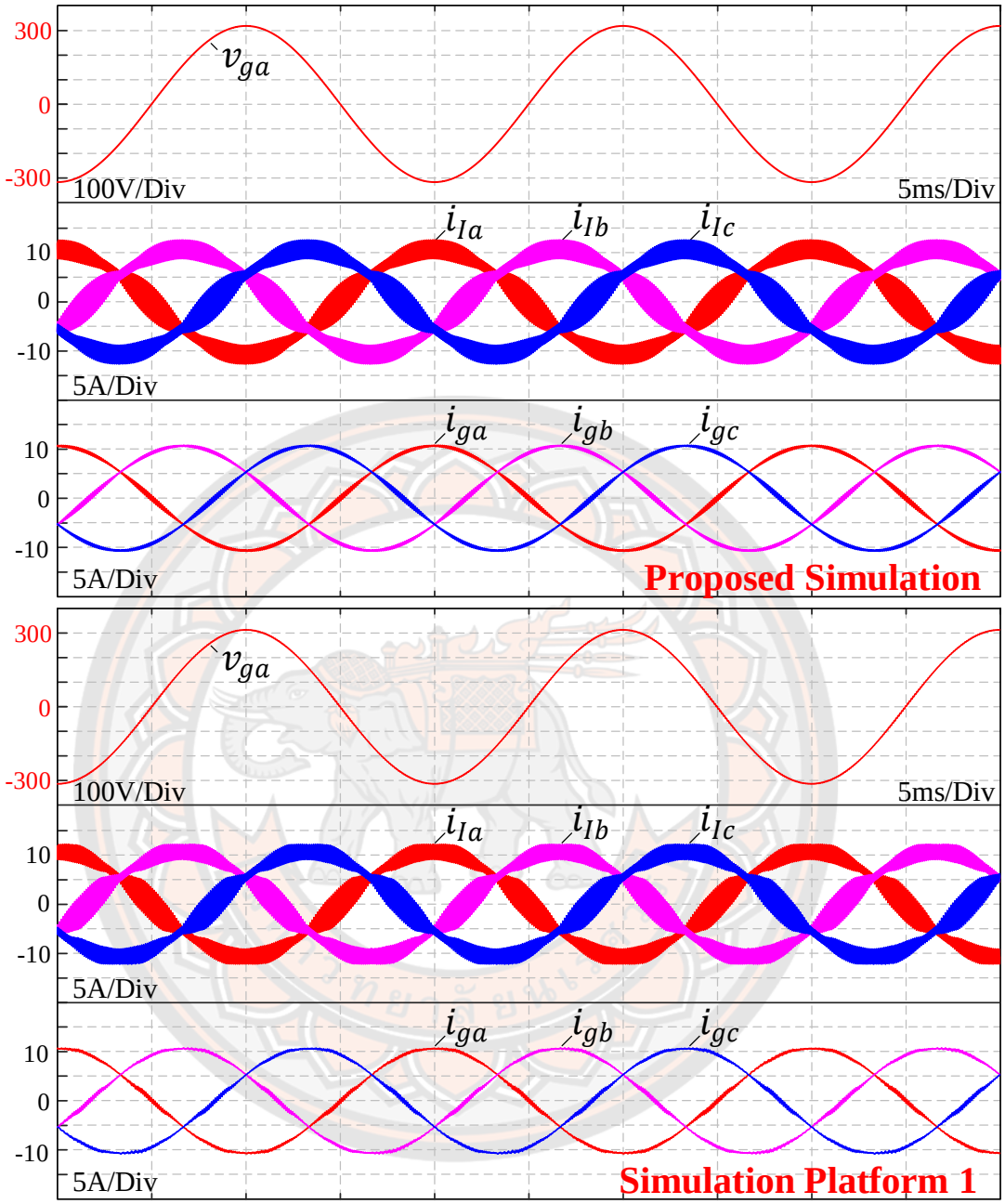


Figure 21 Simulation and experimental results of the VSC without the harmonic compensators under the sinusoidal voltages: Proposed simulation method and simulation platform 1.

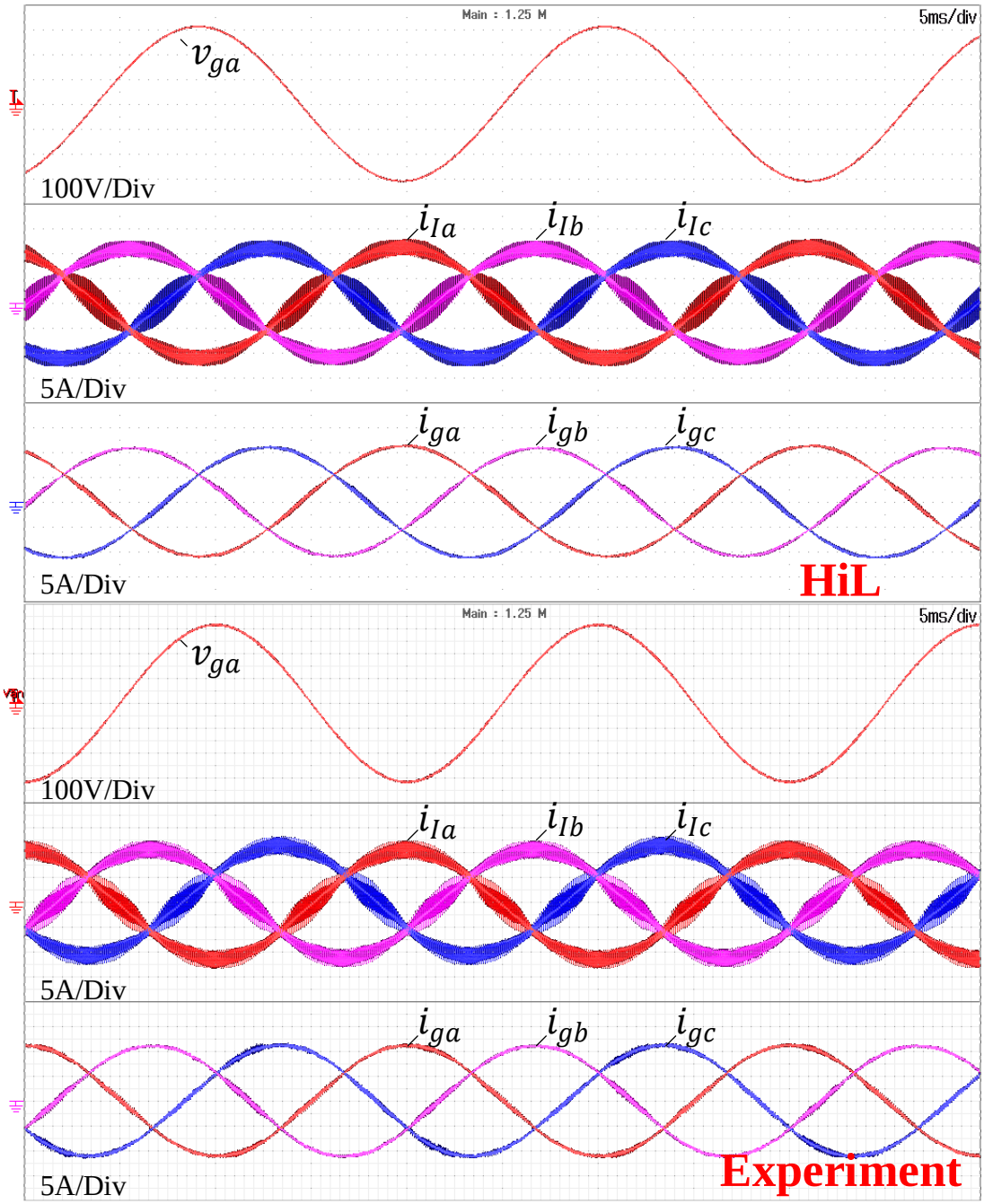


Figure 22 Simulation and experimental results of the VSC without the harmonic compensators under the sinusoidal voltages: HiL-based experiment and hardware implementation.

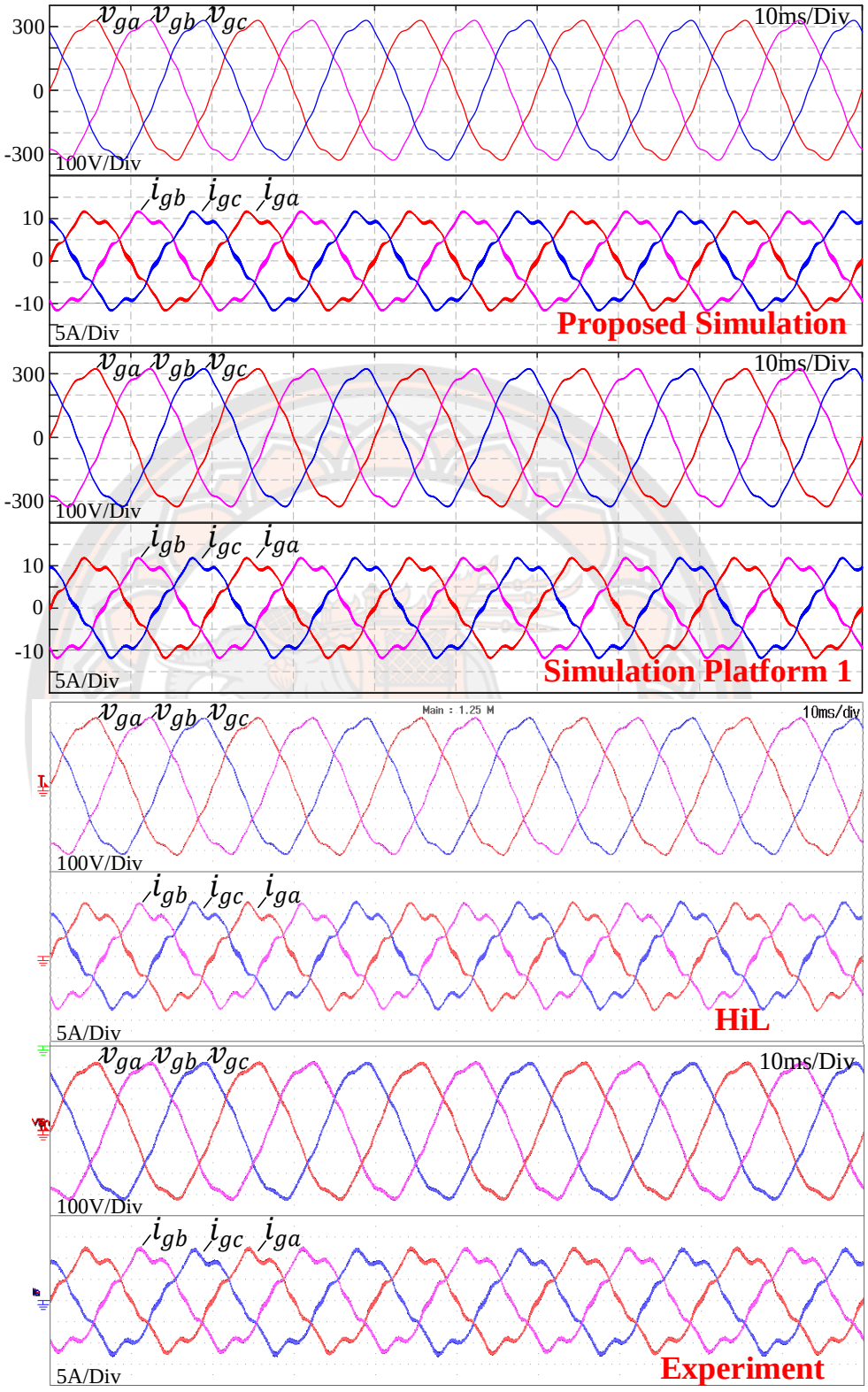


Figure 23 Simulation and experimental results of the VSC without the harmonic compensators under the distorted voltages.

CHAPTER IV

HARMONIC COMPENSATION OF VSC

According to the explanation of the problems that occurred in the previous chapter, it can solve the problem of harmonic voltage distortion by using the harmonic compensations in the current control loop. The harmonic components of the grid current can be represented in the stationary frame or the rotating reference frame. Therefore, can be explained the proposed system in two parts.

Proportional–integral plus multi-resonant (PIMR) controllers

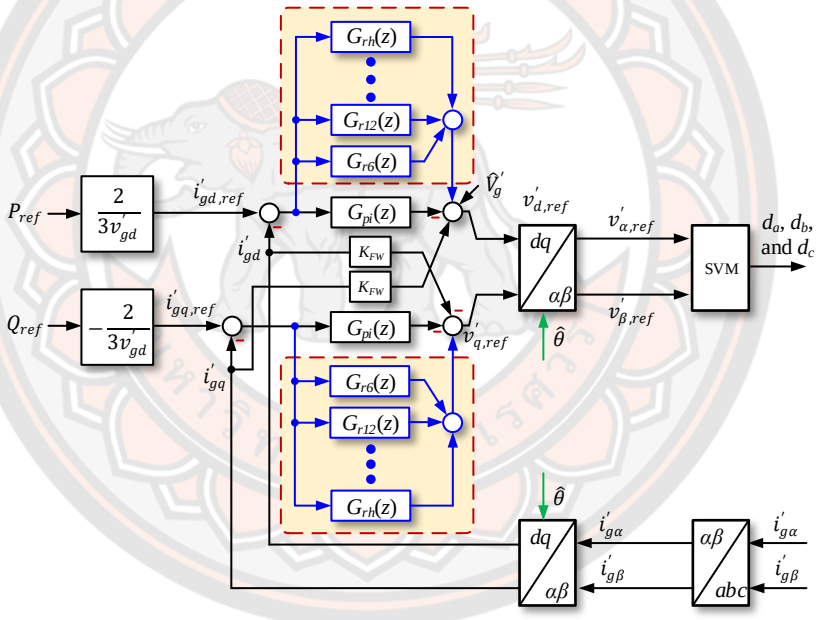


Figure 24 The PIMR controllers is integrated into the control structure.

This section discusses the control scheme of the PIMR controllers on the synchronous reference frame for current control of the three-phase grid-connected LCL-filtered VSC under conditions of grid voltage distortion and grid frequency variation, as illustrated in Figure 24. The harmonic controllers in each order G_{rh} are connected in parallel to the fundamental current controller. The PIMR controller depicted in Figure 25 is adopted for the dq-axes current regulators [14]. The PIMR transfer function in the s-domain is given by

$$G_{ci}(s) = K_p + \frac{K_{i1}}{s} + \sum_{h=6,12,\cdots} \frac{K_{rh}s}{s^2 + (h\omega)^2} \tag{29}$$

The proportional-integral (PI) controller regulates the fundamental component current, which is the DC quantities in the dq-axes. The multiple resonant (MR) controllers regulate both negative and positive sequence components [40], which can be used to attenuate the grid voltage harmonics at the frequencies $\pm 6\omega, \pm 12\omega, \cdots$ in the synchronous reference frame [14].

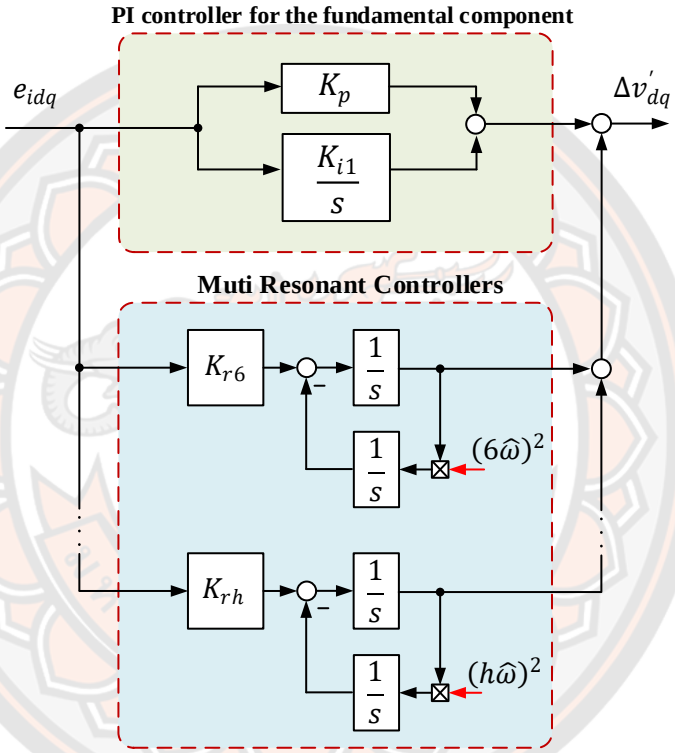


Figure 25 Proportional-integral plus multi-resonant controller.

The double integrator structure of the resonant controllers uses the estimated grid frequency from the PLL for frequency adaptation, as shown in Figure 26. The equivalent transfer function of $G_{ci}^{s}(s)$ in the stationary reference frame is determined from [40]. The superscript " s " denotes the stationary reference frame term.

$$G_{ci}^{s}(s) = G_{ci}(s + j\omega) + G_{ci}(s - j\omega) \tag{30}$$

Substitution of (29) into (30) becomes

$$G_{ci}(s) = K_p + \frac{2K_{i1}s}{s^2 + \omega^2} + \underbrace{\sum_{h=6,12,\cdots} \frac{2K_{ih}(s^2 + (1+h^2)\omega^2)s}{s^4 + 2(1+h^2)\omega^2 s^2 + (1-h^2)^2\omega^4}}_{H(s)} \tag{31}$$

The harmonic compensators $H(s)$ in (31) are identical to individual resonant controllers $R(s)$ tuned at frequencies $(1 \pm h)\omega$ in the stationary reference frame which is given by

$$R(s) = \sum_{h=6,12,\cdots} \frac{K_{ih}s}{s^2 + (1 \pm h)^2\omega^2} \tag{32}$$

Therefore, the stationary frame equivalence of the synchronous reference frame controller $G_{ci}(s)$ is similar to a proportional-multiple resonant controller implemented in the stationary reference frame [14], which is written by

$$G_{ci}^{s}(s) = K_p + \frac{2K_{i1}s}{s^2 + \omega^2} + \sum_{h=6,12,\cdots} \frac{K_{ih}s}{s^2 + (1 \pm h)^2\omega^2} \tag{33}$$

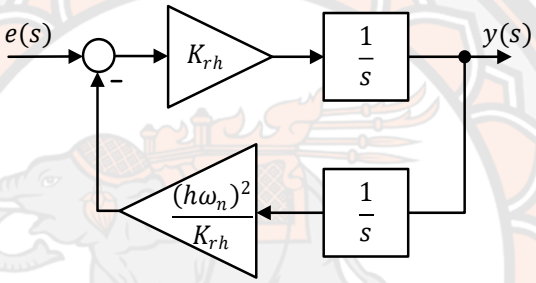


Figure 26 The double integrator structure of resonant controller in continuous time-domain.

Proportional–integral plus multiple synchronous reference frame (PIMSR) controllers

Figure 27 shows the PIMSR control structure, which has the same characteristic as the PIMR controller in the stationary frame [14]. The PIMSR scheme has a fundamental current controller identical to that of the PIMR control scheme. However, the selective HCs are implemented with the integral regulators in the synchronous reference frames corresponding to the grid voltage harmonic components[27, 29-33]. As seen in Figure 27, the reference currents $i'_{gd,ref}$ and $i'_{gq,ref}$ obtained from the active and reactive power commands, are converted to the stationary reference frame by the inverse Park transformation for the harmonic compensators. The reference currents $\mathrm{i}'_{\mathrm{gq,ref}}$ is obtained from the reactive power control loop or by setting $\mathrm{i}'_{\mathrm{gq,ref}} = 0$ for a unity power factor. The grid currents $i'_{g\alpha}$

and $i'_{g\beta}$ are determined from two grid current sensors using the Clarke transformation as follows $i'_{g\alpha} = i'_{ga}$, $i'_{g\beta} = \left(i'_{ga} + 2i'_{gb}\right)/\sqrt{3}$. Then, the grid current errors in the $\alpha\beta$-axes are converted into the dq-axes again using both the positive-sequence and negative-sequence transformations at the harmonic orders $(1 \pm h)$using the grid angles $(1 \pm h)\theta$obtained from PLL. The dc component errors of each order in the dq-axes are then compensated by the integral regulators on the multiple synchronous reference frames at the selective harmonic frequencies. The integral regulator's outputs are transformed to the stationary reference frame using inverse Park transformation. Finally, the VSC reference voltage of the harmonic compensators $v'_{HC\alpha\beta,ref}$ are obtained by adding together all the integral regulators given by

$$\vec{v}'_{HC\alpha\beta,ref} = \sum_{h=5,7,\ldots} \left(v'_{h\alpha,ref} + jv'_{h\beta,ref}\right) = \sum_{h=5,7,\ldots} \left(v'_{hd,ref} + jv'_{hq,ref}\right) \cdot e^{jh\theta} \quad (34)$$

The reference voltages in the $\alpha\beta$-frame of the harmonic compensators are then combined with those of the fundamental component controller.

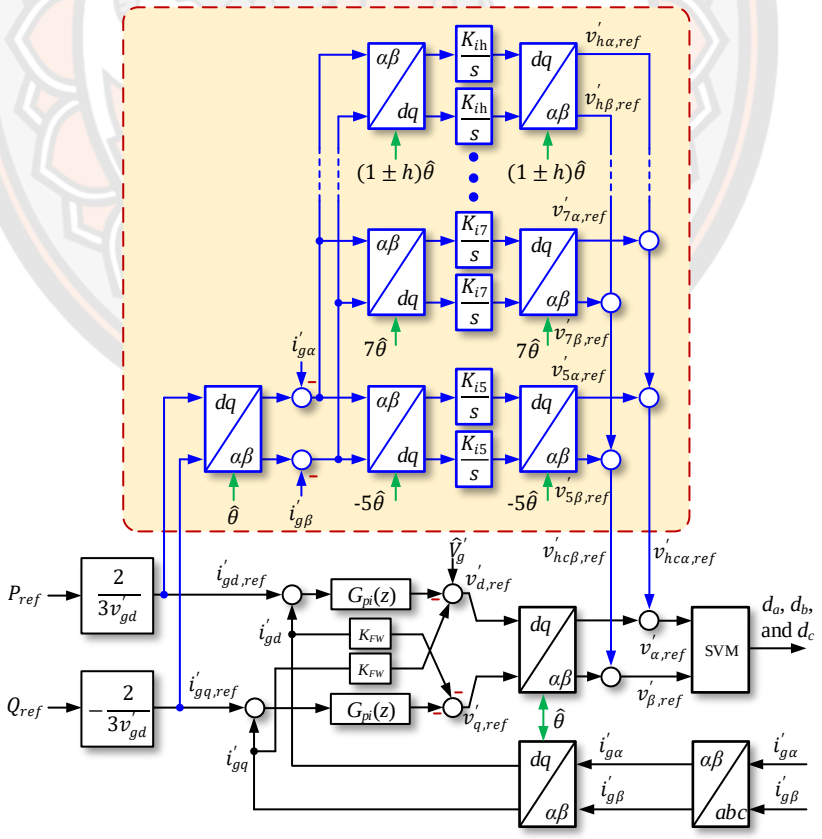


Figure 27 The PIMSR controllers is integrated into the control structure.

Current controller design

The PI controller is responsible for regulating the fundamental component current, which represents the DC quantities in the *dq*-axes. The synchronous reference frame commonly utilizes proportional-integral (PI) regulators in VSC current control. These regulators offer several advantages, including zero-steady state error, power decoupling capability, and the ability to adapt to the grid frequency through axis transformations [15, 17, 25, 26]. The PI controller function in the s-domain is defined in this study as

$$G_{ci}(s) = K_p + \frac{K_{i1}}{s}. \tag{35}$$

The decoupled terms leave the currents i'_{gd} and i'_{gq} are separately controlled. The PI regulator for the fundamental component current is initially designed in the continuous-time domain. The parameters K_{rh} for the resonant controllers are then selected in proportion to the integral gain K_{i1}. According to the design methodology in [47], the PI regulator parameters are selected as follows

$$K_p \approx \omega_{ci,max} L'_t \tag{36}$$

$$K_{i1} \approx \frac{\omega^2_{ci,max}}{10} L'_t \tag{37}$$

where $\omega_{ci,max}$ is the possible maximum cross-over frequency at a given phase margin ϕ_{mi}. The cross-over frequency $\omega_{ci,max}$ is given by

$$\omega_{ci,max} = \frac{\pi/2 - \phi_{mi}}{T_d} \tag{38}$$

where $T_d = 2T_s$ is the sampling and the transport delays caused by the digital control process with T_s as the sampling time. The resonant controllers' gains of the PIMR scheme, orders 6th and 12th, are added to eliminate the voltage harmonics, orders 5th, 7th, 11th, and 13th, whose resonant gains are set at $K_{r6} = K_{r12} = K_{i1}/3$. The integral gains of the PIMSR controller are then set at $K_{i5} = K_{i7} = K_{i11} = K_{i13} = K_{i1}/3$. Therefore, the parameters of the current controller can be found in Table 5.

Table 5 Parameters of the current controller.

Parameters	Value
K_p	0.4080
K_{i1}	213.60
$K_{i5}, K_{i7}, K_{i11}, K_{i13}$	71.21
K_{r6}, K_{r12}	71.21
a_{26}, a_{212}	0.003561
a_{36}	2.495233
a_{312}	9.980929

Figure 29 shows the frequency response of the simplified open-loop transfer function with the PI controller and the PIMR controller. The target phase margin is set at $\phi_{mi} = 60^{\circ}$ with the VSC parameter in Table 3, which results in $\omega_{ci,max} = 2\pi(1111)$ rad/s. The PI controller parameters K_p and K_{i1} are determined from (36) and (37). The resonant controllers, orders 6th and 12th, are added to compensate the voltage harmonics, orders 5th, 7th, 11th, and 13th, whose resonant gains are set at $K_{h6} = K_{h12} = K_{i1}/3$. For the PI controller, the DC loop gain of 100 dB is large enough to track the reference currents with a zero steady-state error. However, the loop gains at 300 Hz and 600 Hz are considerably low to reject the voltage harmonic disturbances. For the PIMR controller, the DC loop gain and the loop gains at 300 Hz and 600 Hz are greater than 100 dB. The phase margin $\phi_{mi} = 48^{\circ}$ of the system with the PIMR controller is still large enough to guarantee the control stability. The actual cross-over frequency $\omega_{ci} = 2\pi(916)$ rad/s is close to the desired value.

The current controller is designed based on the simplified model. Stability assessment is necessary before implementation. The stationary reference frame equivalence of the current controller given in (33) and the transfer function of the LCL filter in (18) are used in the open-loop transfer function $G_o^s(s)$ in the stationary reference frame which is written as

$$G_o^s(s) = \underbrace{G_{ci}^s(s)}_{Controller} \cdot \underbrace{\frac{V_D}{2} e^{-sTd}}_{VSC\&PWM} \cdot \underbrace{G_{LCL}(s)}_{LCL\ filter} \tag{39}$$

Figure 29 depicts the frequency response of $G_o^s(s)$ in the stationary reference frame, where there are three cross-over frequencies ω_{c1}, ω_{c2}, and ω_{c3}. The cross-over frequency near the loop bandwidth $\omega_{c1} = 2\pi(892)$ rad/s slightly shifts from that in the synchronous reference frame due to the presence of the 13th-harmonic peak gain. The phase margin $\phi_{m1} = 42°$ at ω_{c1} is still large enough to guarantee control stability. The other two cross-over frequencies $\omega_{c2} = 2\pi(4730)$ rad/s and $\omega_{c3} = 2\pi(5590)$ rad/s occur around the resonant frequency of the LCL filter ω_{LCL}, of which phase margins $\phi_{m2} = 83°$ and $\phi_{m3} = 67°$ satisfy the stability criterion for the inherent damping of the LCL filter with grid-current feedback control [55].

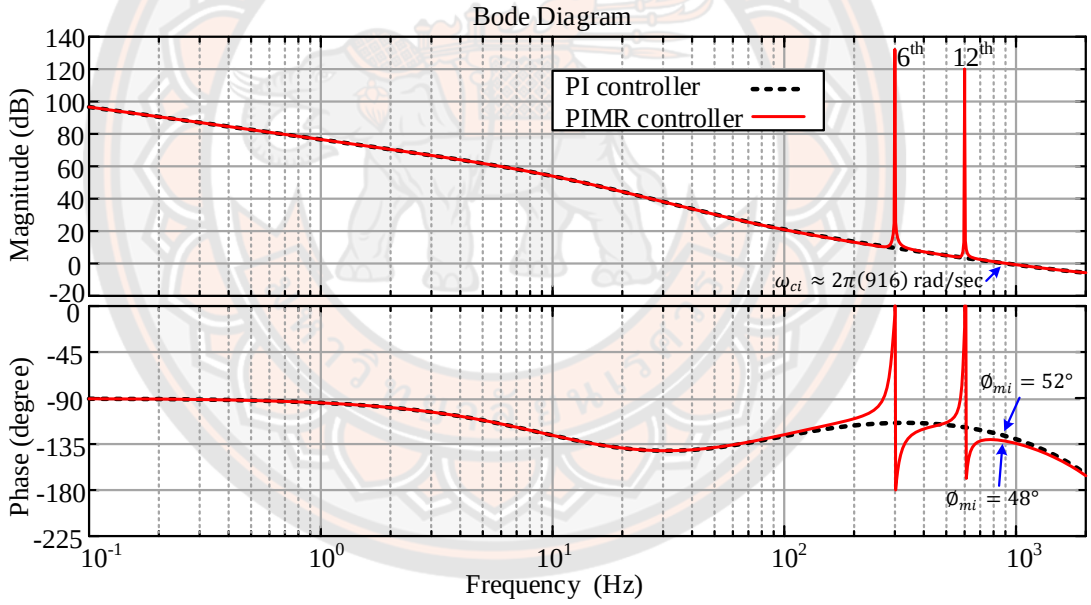
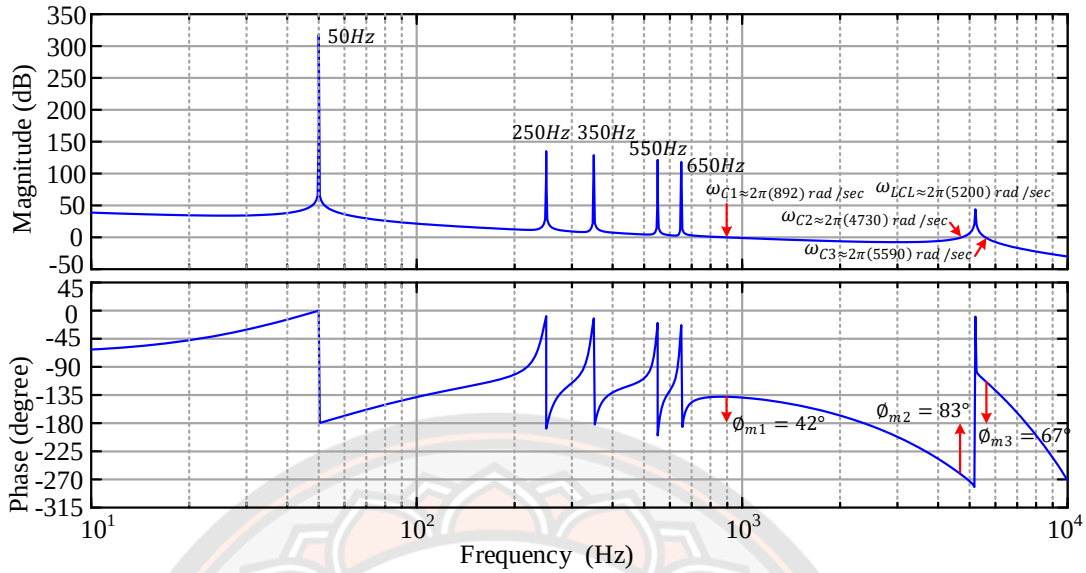


Figure 28 Frequency response of the current control loop: simplified open-loop transfer function in synchronous reference frame with the PI controller and the PIMR controller.



(**b**)

Figure 29 Frequency response of the current control loop: open-loop transfer function in the stationary reference frame.

Implementation of the current controllers with HCs

The PI regulators of the fundamental current controller and the integral regulators of the PIMSR controllers were discretized using the backward Euler approximation. The resonant controller transfer function of $G_{rh}(s)$ is constructed from the double integrator configuration as shown in Figure 26. For the discrete-time transformation of the resonant controller, the forward Euler method $s = (1 - z^{-1})/T_s z^{-1}$ and the backward Euler method $s = (1 - z^{-1})/T_s$ are used for the forward and feedback integrator [56]. Therefore, the control scheme of the multi-resonant controllers at the harmonic orders 6th and 12th can be rewritten in the discrete-time domain according to Fig. 6 and the discrete-time domain transfer function of the resonant controller can be expressed as

$$G_{rh}(z) = \frac{K_{rh}T_s(z^{-1} - z^{-2})}{1 + (T_s^2 h^2 \omega_n^2 - 2)z^{-1} + z^{-2}}. \quad (40)$$

The integrator coefficients of each resonant controllers in Figure 31 can be written as $a_{2h} = K_{rh}T_s$, $a_{3h} = (h\omega_n)^2 T_s/K_{rh}$.

The resonant frequencies at the harmonic orders 6th and 12th are kept tuned with the estimated frequency $\omega\hat{}\,'$ from PLL for grid frequency adaptation. The

fundamental current control has the intrinsic frequency adaptation capability through the Park transformation. For programming of the multi-resonant controllers, each HC is converted to a simple pseudo-code as described in Figure 30. This code is executed each sampling time period of the simulation software or DSP.

```
%Resonant Controller for Order 6th
v6(k) = a26*(e(k-1)-y26(k-1)) + v6(k-1);
y26(k) = a36*v6(k)*wn^2 + y26(k-1);
e(k-1) = e(k);
%Resonant Controller for Order 12th
v12(k) = a212*(e(k-1)-y212(k-1)) + v12(k-1);
y212(k) = a312*v12(k)*wn^2 + y212(k-1);
```

Figure 30 Pseudo-code of the harmonic compensators.

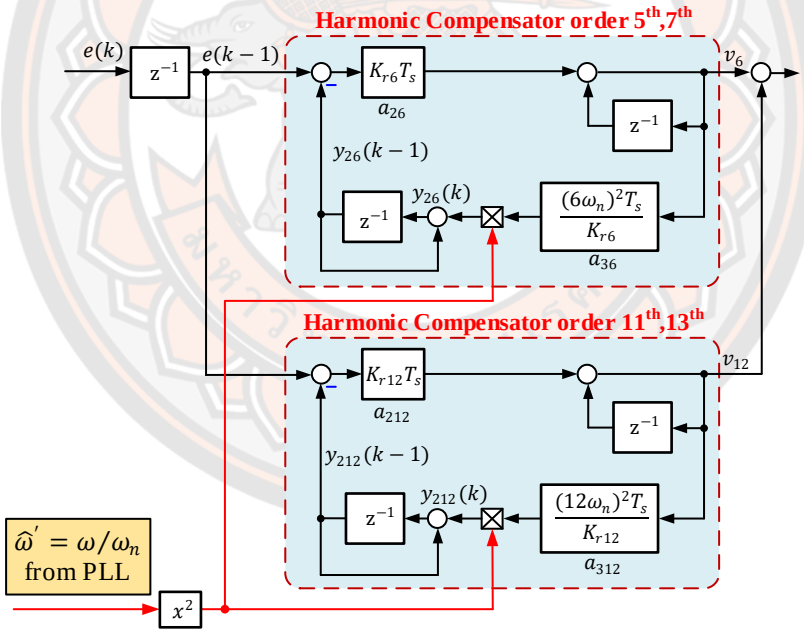
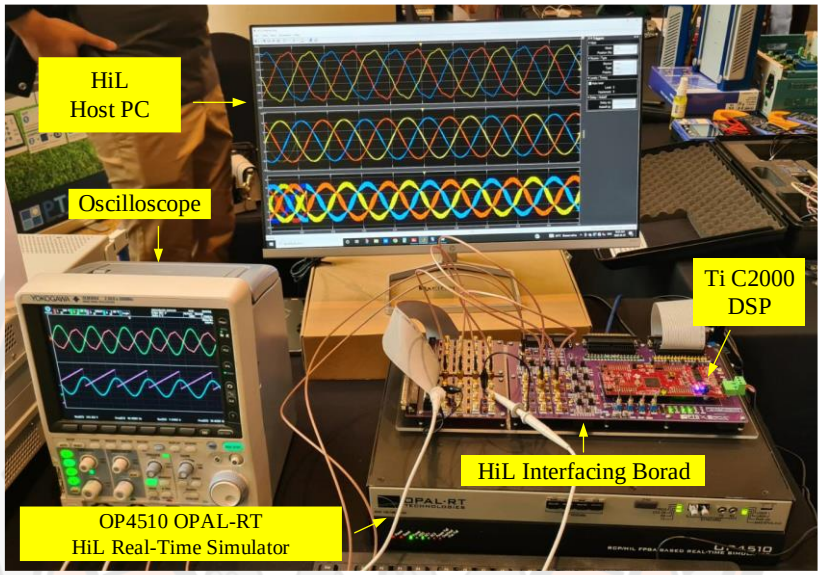


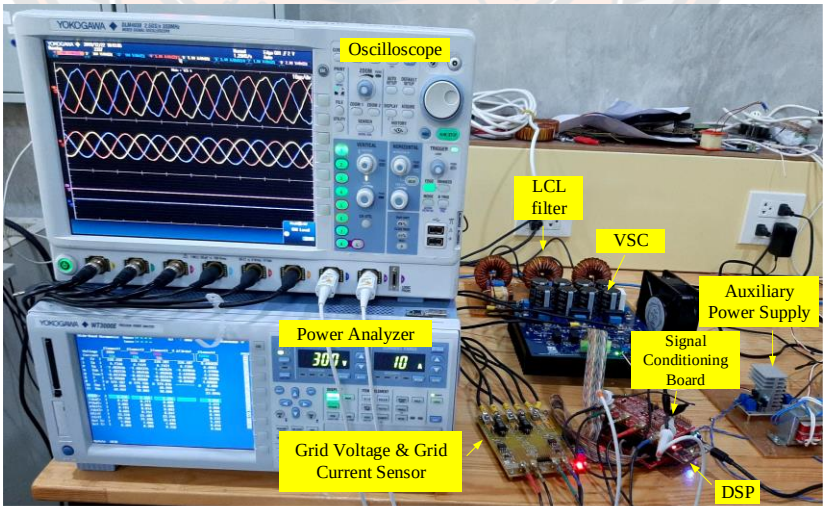
Figure 31 Discrete-time implementation of the PIMR controller with frequency adaptation.

Experimental verification

The simulation model of the VSC developed in MATLAB/Simulink 2022b is provided in [57], which has been presented in previous chapter. Moreover, the proposed control technique was verified through the hardware-in-the-loop (HiL) implementation and the hardware implementation. Figure 32 depict the experimental setup.



(a)



(b)

Figure 32 Experimental setup. (a) HiL configuration (b) Laboratory-scale environment.

Harmonic mitigation

The VSC with the PIMR and PIMSR control schemes was evaluated under the sinusoidal and distorted grid voltages with a nominal steady state power of 5 kW. The harmonic components V_5, V_7, V_{11} and V_{13} were added to the fundamental grid voltage V_1 as shown in Table 4 with a total harmonic distortion (THDv) of 4.69%. The grid frequency was tested under the allowable range of the Thailand grid: the nominal value of 50 Hz, the minimum value of 47 Hz, and the maximum value of 52 Hz. Figure 33 compares the current harmonic components of the fundamental component controller without the HCs (black) with those of the PIMR (red) and PIMSR (blue) control schemes at the nominal grid frequency. The harmonic orders 5th and 7th of the fundamental component controller exceed the IEEE 1547 standard (magenta line) [12]. Moreover, the current harmonic orders 11th and 13th are still noticed. On the other hand, the HCs of the PIMR and PIMSR controllers suppress the current harmonic orders 5th, 7th, 11th, and 13th close to zero, which complies with the IEEE 1547 standard.

Table 6 THD of the grid current at the nominal output power.

Control schemes	Sinusoidal grid voltages			Distorted grid voltages		
	47 Hz	50 Hz	52 Hz	47 Hz	50 Hz	52 Hz
Fundamental component controller	1.21%	1.40%	1.14%	10.97%	10.54%	10.77%
PIMR without frequency adaptation	1.05%	0.97%	1.11%	7.85%	1.08%	8.92%
PIMR	0.88%	0.91%	0.81%	0.96%	1.15%	0.90%
PIMSR	0.93%	0.95%	0.82%	0.93%	1.09%	0.83%

Table 6 summarizes the THDi values of the fundamental component controller, the PIMR controller with/without frequency adaptation, and the PIMSR controller under the sinusoidal and distorted grid voltages at the frequencies of 47 Hz, 50 Hz, and 52 Hz. The PIMR controller without frequency adaptation manages to suppress the voltage harmonics at the nominal grid frequency, compared with the fundamental component controller under the sinusoidal grid voltages. However, the THDi values deteriorate when the grid frequency deviates from the nominal value. The resonant frequencies of the PIMR controller updated from PLL keep the THDi values lower

1.15%. Meanwhile, the PIMSR controller has an inherent frequency adaptation capability, which exhibits a similar harmonic attenuation to the PIMR with frequency adaptation.

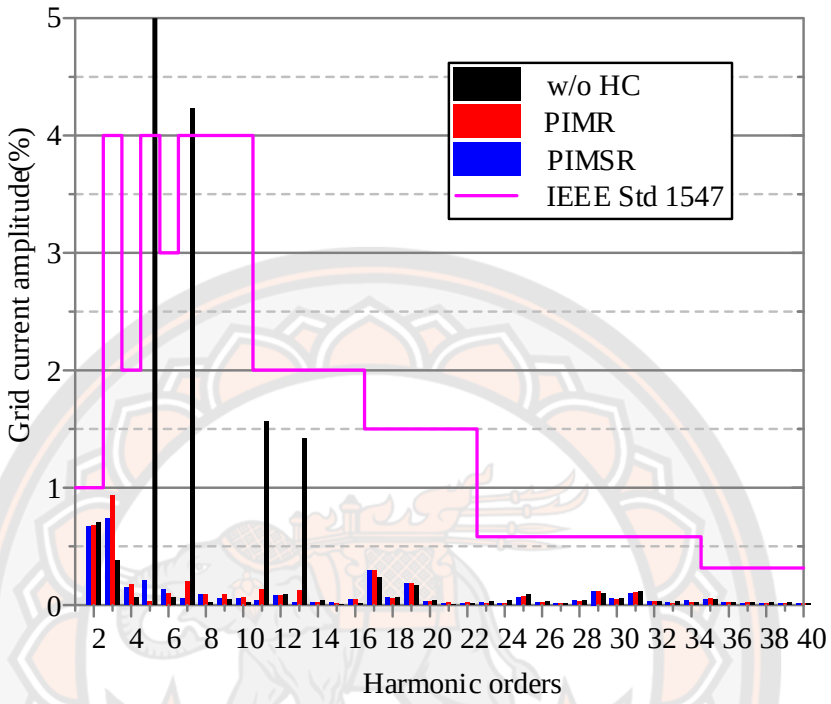


Figure 33 Grid current harmonic spectrum of the VSC at the nominal power of 5 kW under the distorted grid voltage.

Transient performance and power extraction capability

This section validates the transient performance and the power extraction capability of the PIMR and the PIMSR control schemes. Error! Reference source not found. and Error! Reference source not found. shows the simulation result of the dynamic response of the VSC when the reference current suddenly changes under distorted grid voltage, as shown in Table 4. Initially, both the reference currents were set to zero ($i'_{gd,ref} = 0$ p.u. and $i'_{gq,ref} = 0$ p.u.). Then, the reference currents were suddenly changed to $i'_{gd,ref} = -0.7$ p.u. and $i'_{gq,ref} = 0$ p.u.. At this time, the VSC feeds an active power of 3.5 kW into the grid. After that, the VSC injects a reactive power of 3.5 kVar (set $i'_{gq,ref} = -0.7$ p.u.). The experimental results show that the behavior of the grid current waveforms tracks the reference currents. The distorted voltage does not affect the transient response of the grid currents. The grid currents of the PIMR

and the PIMSR schemes at the steady-state conditions are close to the sinusoidal waveform. The zoomed areas in Figure 36 and Figure 37 indicate that the PIMR controller exhibits a transient response very close to the PIMSR controller because of their identical stationary frame transfer function as shown in (33) The simulation results, the experimental results of HiL, and the hardware implementations are in close agreement. However, there is still a slight difference in the rising edge of the grid current step. The oscillation of the grid current during the transient of the simulation result is slightly higher than that of the HiL and hardware experimental results. This is believed to be due to voltage drops in the IGBTs and the grid simulator's internal impedance, which were neglected in the simulation. The instantaneous active and reactive power can be calculated from the *dq*-axes currents directly.

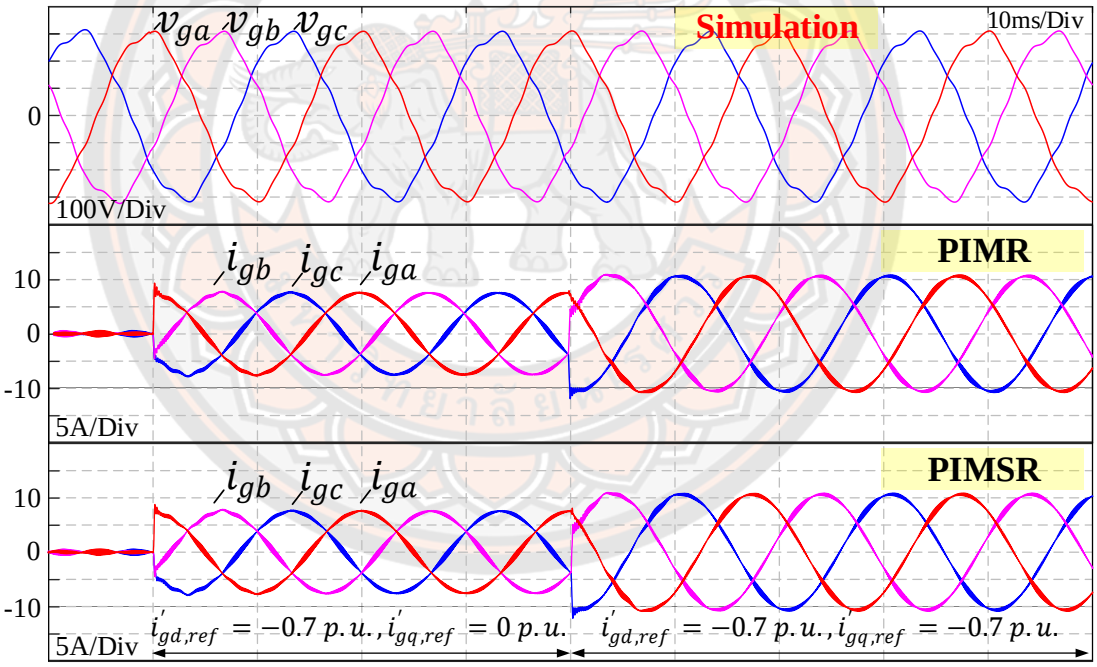


Figure 34 Simulation of the transient response of the grid current under distorted voltage.

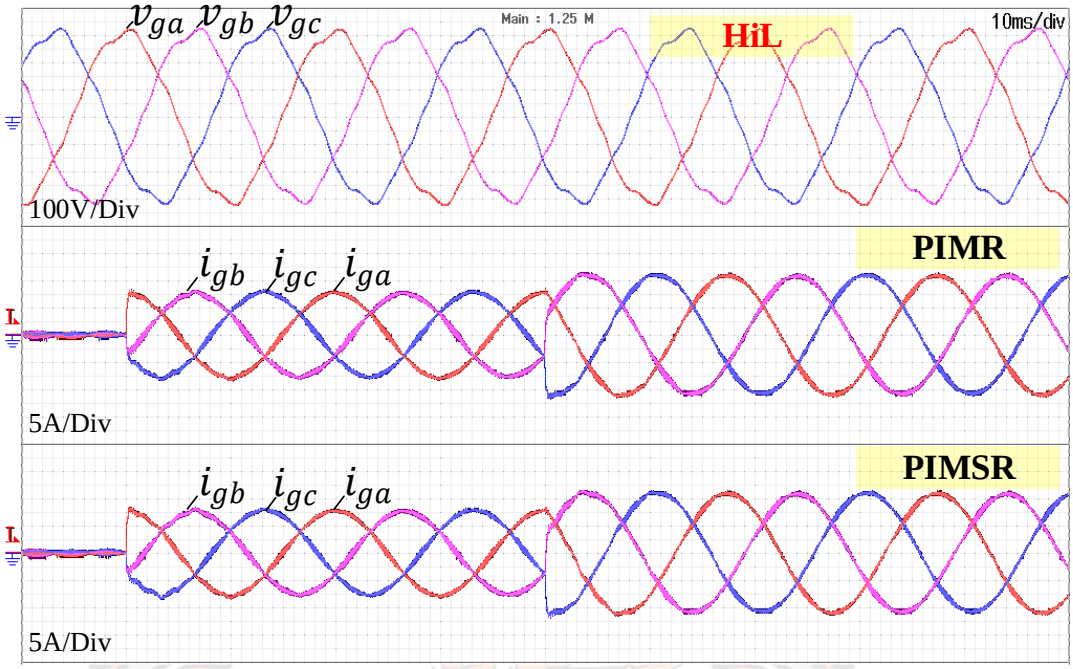


Figure 35 The HiL prototype investigates the transient behavior of the grid current when exposed to distorted voltage.

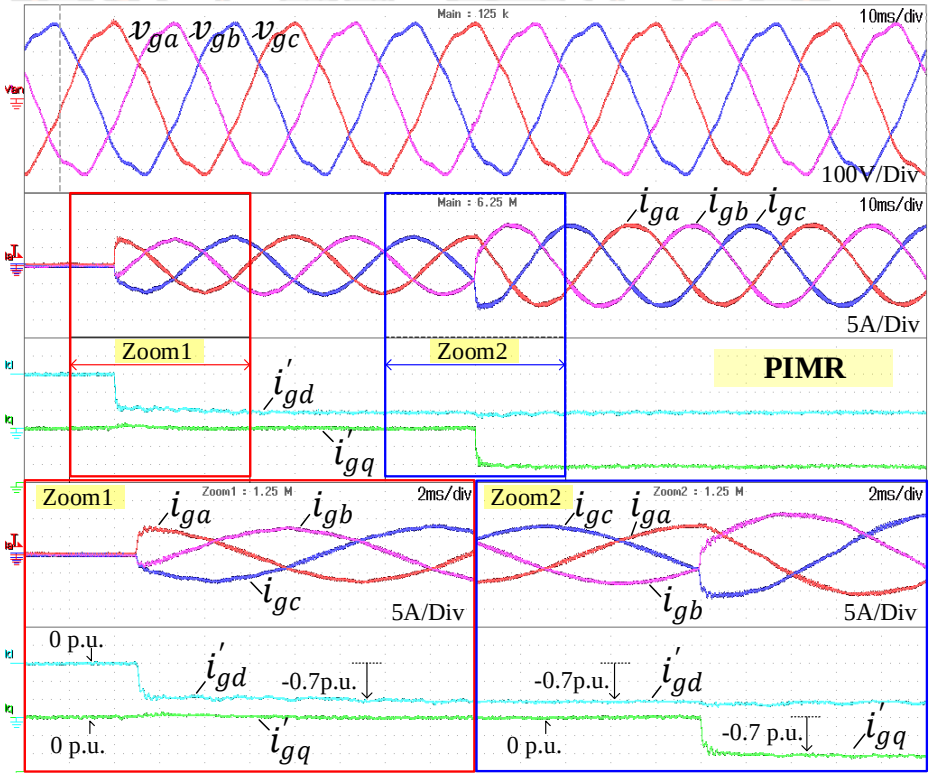


Figure 36 Transient response of the grid current under the distorted voltage.: Hardware prototype with the PIMR controller

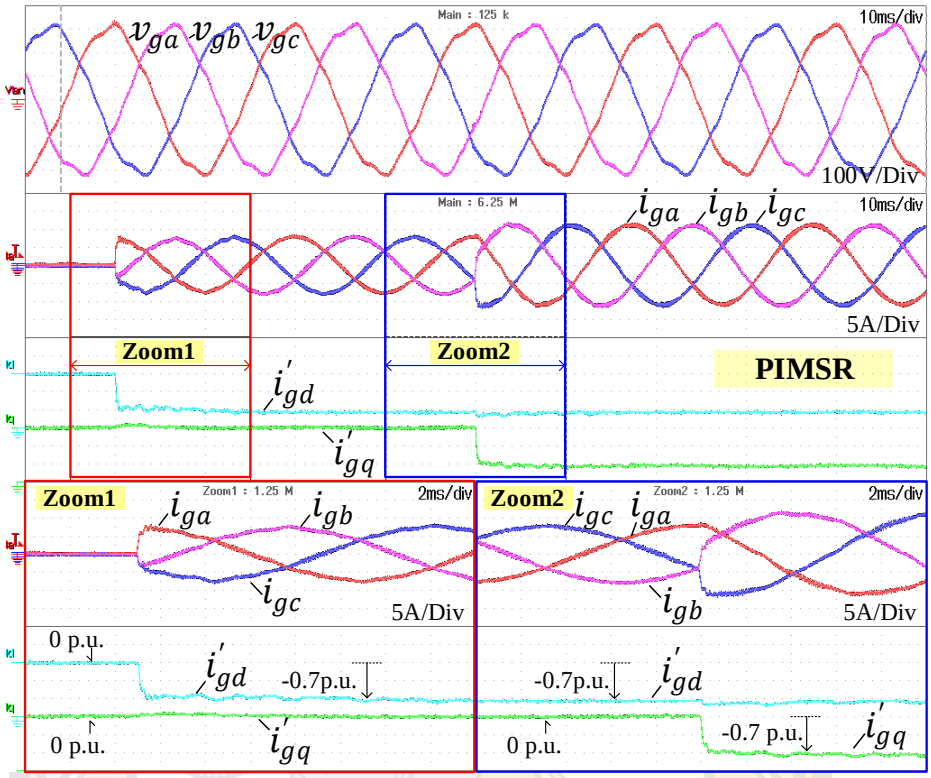


Figure 37 Transient response of the grid current under the distorted voltage.: Hardware prototype with the PIMSR controller

Performance under grid frequency and voltage variation

This section validates the frequency adaptation capability of the PIMR and PIMSR controllers under the sinusoidal and distorted grid voltages. Figure 38 shows the grid current waveforms of the PIMR control scheme under the sinusoidal voltages when the grid frequency changes from 47 Hz to 50 Hz, and from 50 Hz to 52 Hz. The grid current

THDi values with the PIMR controller are 0.88%, 0.90%, and 0.81 because there is no harmonic disturbance from the grid voltages. Figure 39(a) and Figure 39(b) indicate the grid current waves of the PIMR and PIMSR control schemes under the distorted grid voltages when the grid frequency changes from 47 Hz to 50 Hz, and from 50 Hz to 52 Hz. The grid current waveforms of the PIMR controller and the PIMSR controller are very close to those under the sinusoidal voltage in Figure 38 at all the changing frequencies, which has a slight distortion in the edge of the

frequencies, as illustrated in Figure 39(a). The PIMR scheme without the frequency adaptation depicted in Figure 39(b) cannot mitigate the effects of distorted grid voltage when the frequency deviates from the nominal value. Meanwhile, the PIMSR controller exhibits the inherent frequency adaptation capability through the axis transformations The PIMR controller without the frequency adaptation has the THDi of 7.85% at 47 Hz and 8.92% at 52 Hz, which exceeds IEEE 1547 standard [12]. On the other hand, the PIMR controller with frequency adaptation and the PIMSR controller maintain low THDi values at the frequencies of 47 Hz and 52 Hz. The grid current has a THDi approximately 1% that complies with the IEEE 1547 standard. The experimental results from HiL in Figure 39(a) are very close to those of the hardware implementation in Figure 39(b).

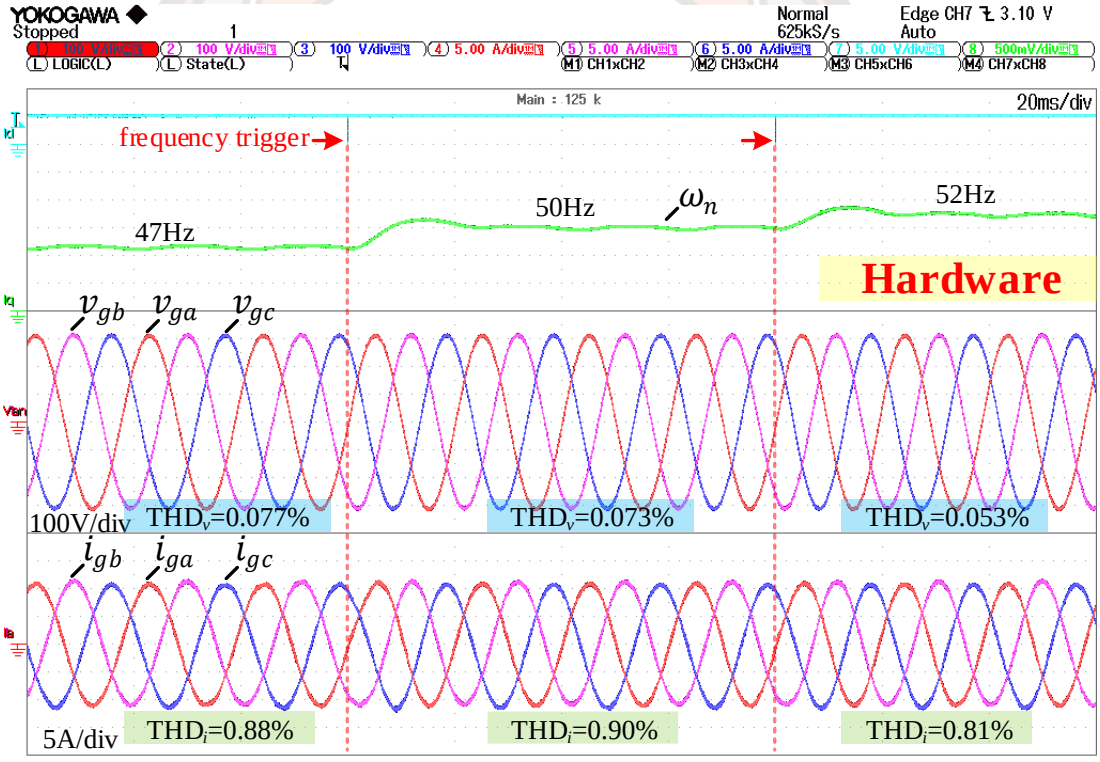
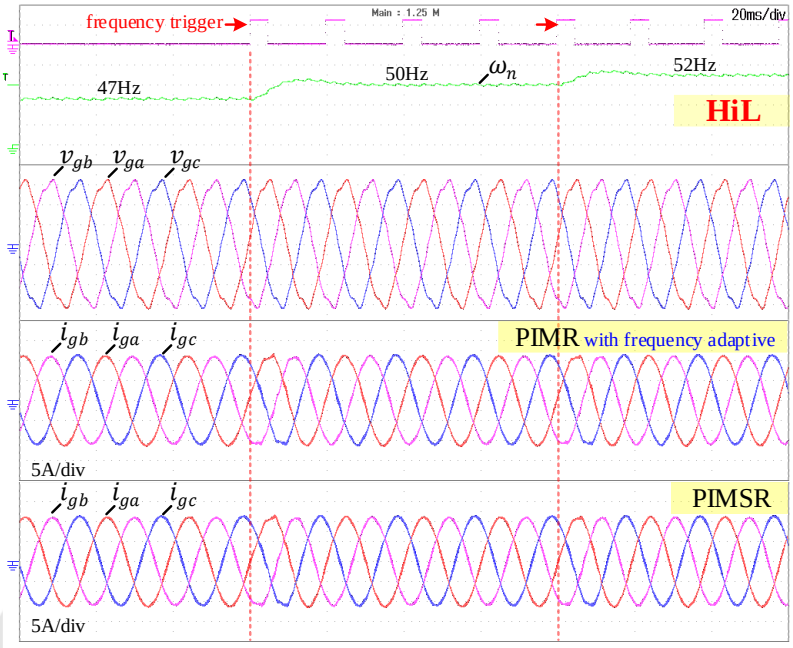
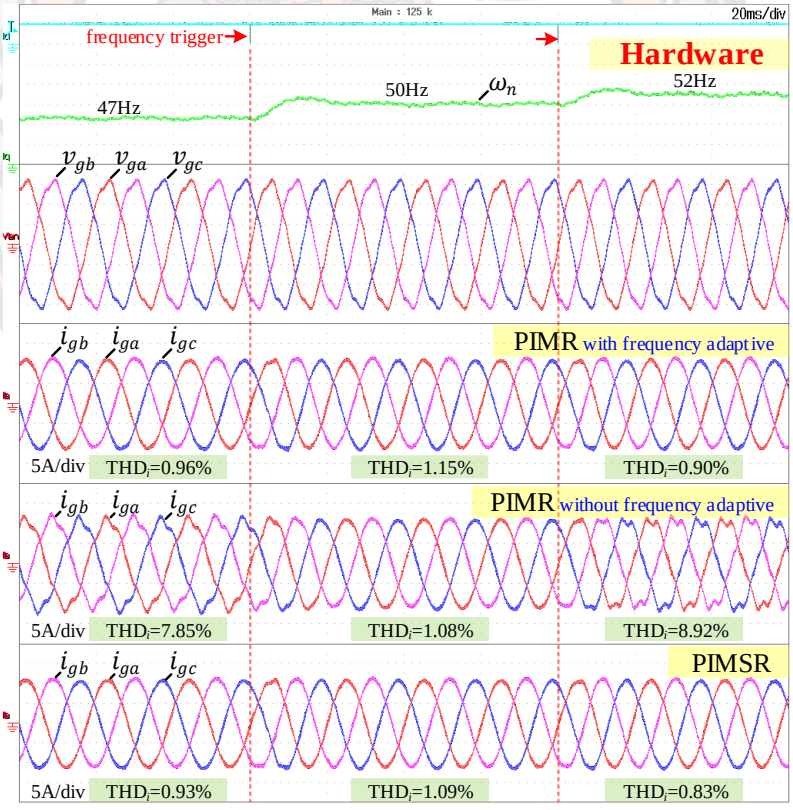


Figure 38 Performance of the PIMR control scheme under the sinusoidal grid voltages with the changing grid frequency.

Figure 40 shows the experimental performance of the PIMR and PIMSR control schemes under the ±10% sag/swell of the distorted grid voltages. The two controllers again exhibit close transient responses, which regulate the grid currents back to the reference values within 10 ms.



(a)



(b)

Figure 39 Performance of the PIMR and PIMSR control schemes under the distorted grid voltages with the changing grid frequency: (a) HiL system, (b) Hardware prototype.

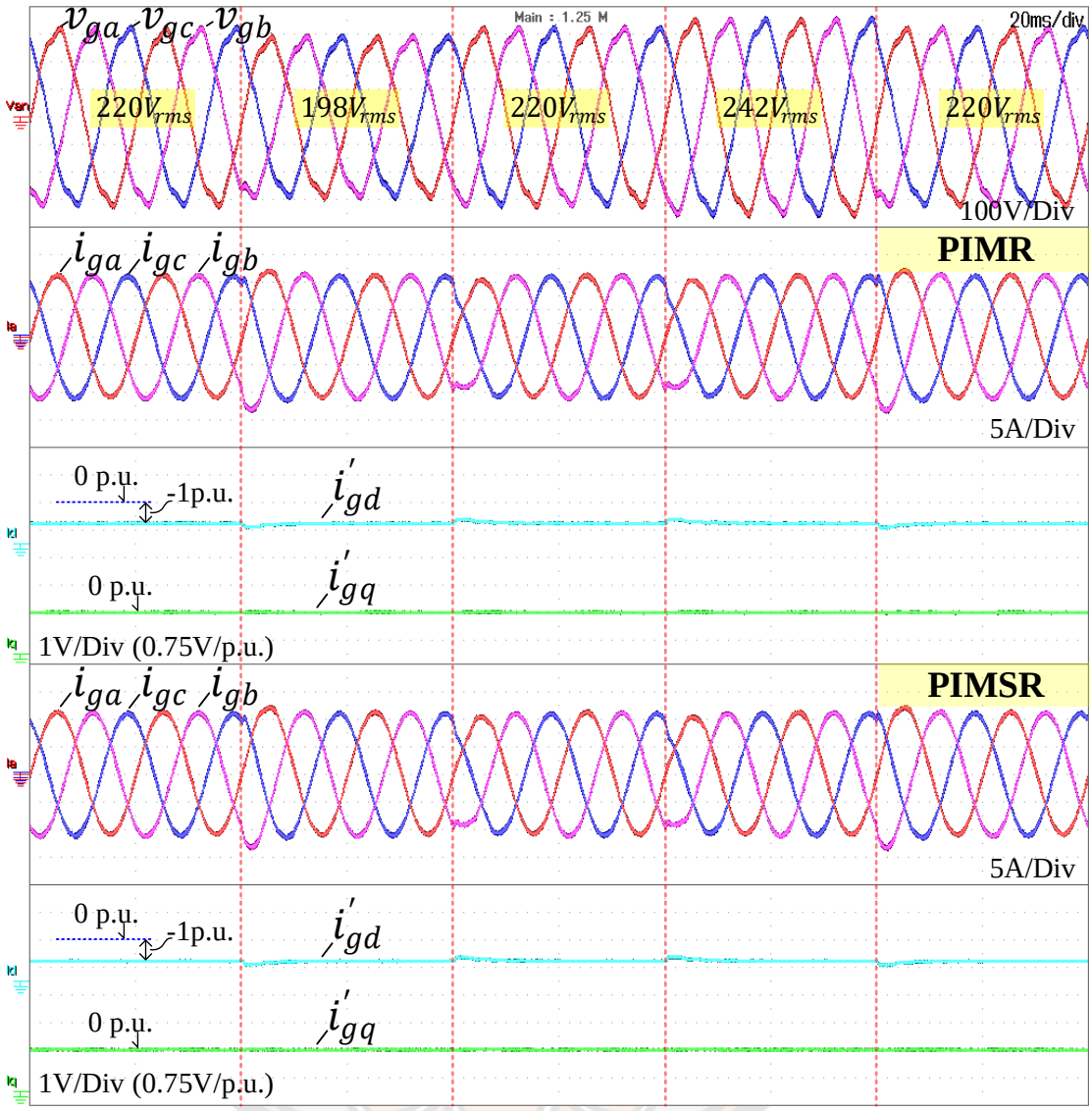


Figure 40 Performance of the PIMR and PIMSR control scheme under the grid voltage sag and swell from the hardware prototype.

Computational effort of the control schemes

Table 7 compares the estimated computational effort of the PIMR and PIMSR controllers for the TMS320F28379D DSP. The PISMR controller requires a substantial computational task for the multiplications and Trigonometric function operations for the harmonic orders, 5th, 7th, 11th, and 13th. Meanwhile, the PIMR controller requires the Trigonometric functions only at the fundamental component, while the resonant controllers at orders, 6th, 12th, use only the additions, subtractions, and multiplications. The PIMR controller presented in this study poses a one-third

computational effort of the PIMSR controller while maintaining the frequency adaptation and power extraction capability. Thus, the PIMSR controller is suggested for the three-phase VSC current control. Although the reduction in the computation time of 2.950 μs with the PIMR scheme seems insignificant when implemented on a powerful TMS320F28379D DSP with a sampling frequency of 20 kHz, the PIMR control scheme will be more beneficial with higher switching and sampling frequencies for wide bandgap devices. For example, the PIMR regulator will be helpful for the multi-loop grid-forming control of

the VSCs in inverter-based electric power systems [58]. Moreover, discretization of the resonant controller is crucial for high switching frequency applications with a significant computation delay [59]. Multiple resonant regulators in series with a fundamental current controller with the deadbeat control have been recently proposed in [60]. Meanwhile, in this study, the multiple resonant regulators are placed in parallel with the fundamental component PI controller. Thus, it would be interesting to compare the harmonic rejection performance and control stability of the parallel and series configuration of the harmonic controller.

Table 7 Computational effort of the control schemes

Mathematical operations	Control methodology	
	PIMR	PIMSR
Additions/subtractions	35	49
Multiplications	198	384
Trigonometric functions (Sin/Cosine)	78	468
Saturation limits	14	14
Execution cycles	325	915
Execution time (0.005 μs/cycle)	1.625 μs	4.575 μs

CHAPTER V

CONCLUSION AND FUTURE WORK

Conclusion

This in-depth exploration of grid-connected voltage source converters (VSCs) featuring selective harmonic mitigation represents a significant leap forward in both theoretical insights and applied solutions. The introductory chapter explores the essential principles, the challenges encountered, and the consequences of incorporating grid inverters into distribution networks affected by severe voltage distortions. Subsequent to this, chapter two offers an exhaustive review of the literature on the strategies for harmonic mitigation in grid-connected inverters under conditions of grid voltage distortion. Chapter three introduces a precise methodology for the modeling of VSCs, advancing further with the development and validation of a simulation approach using MATLAB/Simulink, and the application of switched-circuit modeling for the power stage. Additionally, the operation of a grid-connected inverter under standard grid voltage conditions was simulated using Hardware in the Loop (HiL), yielding simulation outcomes that aligned closely with those from MATLAB/Simulink and laboratory-constructed prototypes. Chapter four delves into the application of a Proportional-Integral plus Multi-Resonant (PIMR) Controller to address issues of grid voltage distortions and frequency variations, conducting a comparative analysis with the Proportional-Integral plus Multiple Synchronous Reference Frame (PIMSR) controller. The findings indicate that although both controllers produced similar results, the PIMR controller exhibited a lower computational complexity, rendering it more advantageous for practical implementation.

Future Work

1. Propose a technique for determining a Resonant controller's proper gain value

Chapter 4, in subtopic "Current Controller Design," provides a detailed explanation of how to determine the gain for a grid current controller using a PI controller. However, it does not address the process for determining the resonant controller's gain. The researcher relied on trial-and-error methods to identify a suitable gain value. For the resonant controller to effectively eliminate harmonic currents, it is essential to establish an analytical method to accurately and correctly determine the gain values.

2. Enhanced harmonic mitigation techniques

Future research could focus on developing adaptive harmonic controllers that automatically adjust their parameters in real-time to better handle varying grid conditions and load demands. This could involve the integration of machine learning algorithms to predict and mitigate harmonic distortions.

3. Impact of electric vehicle charging stations

The thesis mentions the increasing presence of electric vehicles (EVs) and their charging stations. However, it does not explore in-depth the specific challenges and solutions related to harmonic mitigation in the context of high-power, fast-charging stations for EVs. Research in this area could focus on mitigating harmonics specifically introduced by EV charging infrastructure.

4. High-order harmonic mitigation

The study addresses harmonic compensation for certain harmonic orders but does not extensively cover higher-order harmonics beyond the 12th. Future research could investigate methods for effectively mitigating higher-order harmonics and their impact on power quality.

5. Integration with renewable energy sources

Investigate the performance of the proposed harmonic mitigation techniques in hybrid systems that combine multiple renewable energy sources such as wind, solar, and hydro. This research could explore how the varying outputs of different renewable sources affect harmonic generation and mitigation.

6. Grid interaction and stability

Conduct comprehensive studies on the impact of harmonic mitigation techniques on overall grid stability. This can include examining how these techniques influence the stability margins of power systems and their interactions with other grid stability mechanisms.

7. Standards and compliance

As power quality standards evolve, future work should focus on ensuring that the proposed techniques comply with the latest regulations and standards. This may involve participating in standardization committees and contributing to the development of new guidelines.

8. Real-time monitoring and control

Develop real-time monitoring systems that continuously assess the harmonic levels and automatically adjust the mitigation techniques to ensure optimal performance. These systems can leverage IoT technologies for enhanced connectivity and data analytics.

9. Scalability and flexibility

Explore the scalability of the proposed techniques for different sizes and types of grid-connected systems. This can include small-scale residential systems to large-scale industrial applications.

REFERENCES

[1] B. K. Bose, "Global Warming: Energy, Environmental Pollution, and the Impact of Power Electronics," *IEEE Industrial Electronics Magazine*, vol. 4, no. 1, pp. 6-17, 2010, doi: 10.1109/MIE.2010.935860.

[2] H. Rahimi-Eichi, U. Ojha, F. Baronti, and M. Chow, "Battery Management System: An Overview of Its Application in the Smart Grid and Electric Vehicles," *IEEE Industrial Electronics Magazine*, vol. 7, no. 2, pp. 4-16, 2013, doi: 10.1109/MIE.2013.2250351.

[3] X. Fang, S. Misra, G. Xue, and D. Yang, "Smart Grid — The New and Improved Power Grid: A Survey," *IEEE Communications Surveys & Tutorials*, vol. 14, no. 4, pp. 944-980, 2012, doi: 10.1109/SURV.2011.101911.00087.

[4] K. Lo, Y. Chen, and Y. Chang, "Bidirectional Single-Stage Grid-Connected Inverter for a Battery Energy Storage System," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4581-4590, 2017, doi: 10.1109/TIE.2016.2559453.

[5] H. Qian, J. Zhang, J. Lai, and W. Yu, "A high-efficiency grid-tie battery energy storage system," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 886-896, 2011, doi: 10.1109/TPEL.2010.2096562.

[6] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 263-272, 2006, doi: 10.1109/TPEL.2005.861185.

[7] W. M. Wu, Y. Liu, Y. B. He, H. S. H. Chung, M. Liserre, and F. Blaabjerg, "Damping Methods for Resonances Caused by LCL-Filter-Based Current-Controlled Grid-Tied Power Inverters: An Overview," (in English), *Ieee Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7402-7413, Sep 2017, doi: 10.1109/Tie.2017.2714143.

[8] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology," *IEEE Industrial Electronics Magazine*, vol. 9, no. 1, pp. 47-61, 2015, doi: 10.1109/MIE.2014.2376976.

[9] M. Yilmaz and P. T. Krein, "Review of Battery Charger Topologies, Charging Power Levels, and Infrastructure for Plug-In Electric and Hybrid Vehicles," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2151-2169, 2013, doi: 10.1109/TPEL.2012.2212917.

[10] T. Erika and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 888-895, 2003, doi: 10.1109/TPEL.2003.810838.

[11] Z. Xin, P. Mattavelli, W. Yao, Y. Yang, F. Blaabjerg, and P. C. Loh, "Mitigation of Grid-Current Distortion for LCL-Filtered Voltage-Source Inverter With Inverter-Current Feedback Control," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6248-6261, 2018, doi: 10.1109/TPEL.2017.2740946.

[12] "IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces," *IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003)*, pp. 1-138, 2018, doi: 10.1109/IEEESTD.2018.8332112.

[13] Y. Yang, K. Zhou, H. Wang, and F. Blaabjerg, "Analysis and Mitigation of Dead-Time Harmonics in the Single-Phase Full-Bridge PWM Converter With Repetitive Controllers," *IEEE Transactions on Industry Applications,* vol. 54, no. 5, pp. 5343-5354, 2018, doi: 10.1109/TIA.2018.2825941.

[14] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Multiple harmonics control for three-phase grid converter systems with the use of PI-RES current controller in a rotating frame," *IEEE Trans. Power Electron.,* vol. 21, no. 3, pp. 836-841, 2006, doi: 10.1109/TPEL.2006.875566.

[15] C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg, "Frequency Response Analysis of Current Controllers for Selective Harmonic Compensation in Active Power Filters," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 2, pp. 337-347, 2009, doi: 10.1109/TIE.2008.2006953.

[16] Y. Liu, W. Wu, Y. He, Z. Lin, F. Blaabjerg, and H. S. Chung, "An Efficient and Robust Hybrid Damper for LCL- or $LLCL$-Based Grid-Tied Inverter With Strong Grid-Side Harmonic Voltage Effect Rejection," *IEEE Transactions on Industrial Electronics,* vol. 63, no. 2, pp. 926-936, 2016, doi: 10.1109/TIE.2015.2478738.

[17] J. Hu, H. Nian, H. Xu, and Y. He, "Dynamic Modeling and Improved Control of DFIG Under Distorted Grid Voltage Conditions," *IEEE Transactions on Energy Conversion,* vol. 26, no. 1, pp. 163-175, 2011, doi: 10.1109/TEC.2010.2071875.

[18] C. Xie, X. Zhao, K. Li, J. Zou, and J. M. Guerrero, "Multirate Resonant Controllers for Grid-Connected Inverters With Harmonic Compensation Function," *IEEE Transactions on Industrial Electronics,* vol. 66, no. 11, pp. 8981-8991, 2019, doi: 10.1109/TIE.2018.2868249.

[19] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 814-822, 2003, doi: 10.1109/TPEL.2003.810852.

[20] G. Shen, X. Zhu, J. Zhang, and D. Xu, "A New Feedback Method for PR Current Control of LCL-Filter-Based Grid-Connected Inverter," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 6, pp. 2033-2041, 2010, doi: 10.1109/TIE.2010.2040552.

[21] X. Li, J. Fang, Y. Tang, X. Wu, and Y. Geng, "Capacitor-Voltage Feedforward With Full Delay Compensation to Improve Weak Grids Adaptability of LCL-Filtered Grid-Connected Converters for Distributed Generation Systems," *IEEE Transactions on Power Electronics,* vol. 33, no. 1, pp. 749-764, 2018, doi: 10.1109/TPEL.2017.2665483.

[22] X. Wang, F. Blaabjerg, and P. C. Loh, "Virtual RC Damping of LCL-Filtered Voltage Source Converters With Extended Selective Harmonic Compensation," *IEEE Transactions on Power Electronics,* vol. 30, no. 9, pp. 4726-4737, 2015, doi: 10.1109/TPEL.2014.2361853.

[23] Y. Yang, K. Zhou, and F. Blaabjerg, "Enhancing the Frequency Adaptability of Periodic Current Controllers With a Fixed Sampling Rate for Grid-Connected Power Converters," *IEEE Transactions on Power Electronics,* vol. 31, no. 10, pp. 7273-7285, 2016, doi: 10.1109/TPEL.2015.2507545.

[24] S. Somkun, "High performance current control of single-phase grid-connected converter with harmonic mitigation, power extraction and frequency adaptation capabilities," *IET Power Electronics,* vol. 14, no. 2, pp. 352-372, 2020, doi:

10.1049/pel2.12038.

[25] C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg, "High Performance Current Controller for Selective Harmonic Compensation in Active Power Filters," *IEEE Transactions on Power Electronics,* vol. 22, no. 5, pp. 1826-1835, 2007, doi: 10.1109/TPEL.2007.904060.

[26] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Transactions on Industrial Electronics,* vol. 53, no. 5, pp. 1398-1409, 2006, doi: 10.1109/TIE.2006.881997.

[27] D. Campos-Gaona, R. Peña-Alzola, J. L. Monroy-Morales, M. Ordonez, O. Anaya-Lara, and W. E. Leithead, "Fast Selective Harmonic Mitigation in Multifunctional Inverters Using Internal Model Controllers and Synchronous Reference Frames," *IEEE Transactions on Industrial Electronics,* vol. 64, no. 8, pp. 6338-6349, 2017, doi: 10.1109/TIE.2017.2682003.

[28] M. J. Newman, D. N. Zmood, and D. G. Holmes, "Stationary frame harmonic reference generation for active filter systems," *IEEE Transactions on Industry Applications,* vol. 38, no. 6, pp. 1591-1599, 2002, doi: 10.1109/TIA.2002.804739.

[29] L. Asiminoael, F. Blaabjerg, and S. Hansen, "Detection is key - Harmonic detection methods for active power filter applications," *IEEE Industry Applications Magazine,* vol. 13, no. 4, pp. 22-33, 2007, doi: 10.1109/MIA.2007.4283506.

[30] L. Bao, J. Xia, Z. Dong, Y. Deng, Y. Lu, and Y. Yang, "An Improved Three-Phase Four-Wire Harmonic Detection Algorithm Based on Multi-Synchronous Rotating Frame Transformation," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society,* 14-17 Oct. 2019 2019, vol. 1, pp. 2115-2120, doi: 10.1109/IECON.2019.8927561. [Online]. Available: https://ieeexplore.ieee.org/stampPDF/getPDF.jsp?tp=&arnumber=8927561&ref=

[31] S. Bhattacharya, T. M. Frank, D. M. Divan, and B. Banerjee, "Active filter system implementation," *IEEE Industry Applications Magazine,* vol. 4, no. 5, pp. 47-63, 1998, doi: 10.1109/2943.715508.

[32] P. Mattavelli, "A closed-loop selective harmonic compensation for active filters," *IEEE Transactions on Industry Applications,* vol. 37, no. 1, pp. 81-89, 2001, doi: 10.1109/28.903130.

[33] E. Uz-Logoglu, O. Salor, and M. Ermis, "Online Characterization of Interharmonics and Harmonics of AC Electric Arc Furnaces by Multiple Synchronous Reference Frame Analysis," *IEEE Transactions on Industry Applications,* vol. 52, no. 3, pp. 2673-2683, 2016, doi: 10.1109/TIA.2016.2524455.

[34] C. G. Moral, J. M. Guerrero, D. Fernández, D. Reigosa, C. R. Pereda, and F. Briz, "Realizable Reference Antiwindup Implementation for Parallel Controller Structures," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 9, no. 4, pp. 5055-5068, 2021, doi: 10.1109/JESTPE.2020.3021035.

[35] N. F. Guerrero-Rodríguez, A. B. Rey-Boué, and E. Reyes-Archundia, "Overview and comparative study of two control strategies used in 3-phase grid-connected

inverters for renewable systems," *Renewable Energy Focus*, vol. 19-20, pp. 75-89, 2017/06/01/ 2017, doi: https://doi.org/10.1016/j.ref.2017.05.007.

[36] R. A. Khan, M. N. Ashraf, and W. Choi, "A Harmonic Compensation Method Using a Lock-In Amplifier under Non-Sinusoidal Grid Conditions for Single Phase Grid Connected Inverters," *Energies*, vol. 14, no. 3, doi: 10.3390/en14030597.

[37] M. C. Kisacikoglu, M. Kesler, and L. M. Tolbert, "Single-Phase On-Board Bidirectional PEV Charger for V2G Reactive Power Operation," *IEEE Transactions on Smart Grid*, vol. 6, no. 2, pp. 767-775, 2015, doi: 10.1109/TSG.2014.2360685.

[38] J. Xia, Y. Guo, X. Zhang, J. Jatskevich, and N. Amiri, "Robust Control Strategy Design for Single-Phase Grid-Connected Converters Under System Perturbations," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 11, pp. 8892-8901, 2019, doi: 10.1109/TIE.2019.2902791.

[39] S. Zhou, Y. Zhang, Z. Liu, J. Liu, and L. Zhou, "Implementation of Cross-coupling Terms in Proportional-Resonant Current Control Schemes for Improving Current Tracking Performance," *IEEE Transactions on Power Electronics*, pp. 1-1, 2021, doi: 10.1109/TPEL.2021.3080131.

[40] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *IEE Proceedings - Electric Power Applications*, vol. 153, no. 5, pp. 750-762, 2006, doi: 10.1049/ip-epa:20060008.

[41] S. Srita *et al.*, "Modeling, Simulation and Development of Grid-Connected Voltage Source Converter with Selective Harmonic Mitigation: HiL and Experimental Validations," *Energies*, vol. 15, no. 7, p. 2535, 2022. [Online]. Available: https://www.mdpi.com/1996-1073/15/7/2535.

[42] F. J. Rodriguez, E. Bueno, M. Aredes, L. G. B. Rolim, F. A. S. Neves, and M. C. Cavalcanti, "Discrete-time implementation of second order generalized integrators for grid converters," in *2008 34th Annual Conference of IEEE Industrial Electronics*, 10-13 Nov. 2008 2008, pp. 176-181, doi: 10.1109/IECON.2008.4757948.

[43] S. Srita and S. Somkun, "Implementation of Harmonic Compensation for Three-Phase Grid-Connected Voltage-Source Converter Under Grid Voltage Distortion," in *2022 19th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)*, 24-27 May 2022 2022, pp. 1-5, doi: 10.1109/ECTI-CON54298.2022.9795533.

[44] K. Zhou, Y. Yang, F. Blaabjerg, and D. Wang, "Optimal Selective Harmonic Control for Power Harmonics Mitigation," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 1220-1230, 2015, doi: 10.1109/TIE.2014.2336629.

[45] A. Milczarek, K. Możdżyński, M. Malinowski, and S. Styński, "Effective and Simple Control of Grid-Connected Three-Phase Converter Operating at a Strongly Distorted Voltage," *IEEE Access*, vol. 8, pp. 12307-12315, 2020, doi: 10.1109/ACCESS.2020.2965727.

[46] J. Dannehl, C. Wessels, and F. W. Fuchs, "Limitations of Voltage-Oriented PI Current Control of Grid-Connected PWM Rectifiers With LCL Filters," (in

English), *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 380-388, Feb 2009, doi: 10.1109/Tie.2008.2008774.

[47] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized design of stationary frame three phase AC current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417-2426, 2009, doi: 10.1109/tpel.2009.2029548.

[48] S. G. Parker, B. P. McGrath, and D. G. Holmes, "Regions of Active Damping Control for LCL Filters," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 424-432, 2014, doi: 10.1109/TIA.2013.2266892.

[49] W. Yao, Y. Yang, X. Zhang, F. Blaabjerg, and P. C. Loh, "Design and Analysis of Robust Active Damping for LCL Filters Using Digital Notch Filters," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2360-2375, 2017, doi: 10.1109/TPEL.2016.2565598.

[50] Y. Han *et al.*, "Modeling and Stability Analysis of LCL -Type Grid-Connected Inverters: A Comprehensive Overview," *IEEE Access*, vol. 7, pp. 114975-115001, 2019, doi: 10.1109/ACCESS.2019.2935806.

[51] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation For Power Converters Principles and Practice* (IEEE Series on Power Engineering). IEEE PRESS, 2003.

[52] S. SRITA and S. SOMKUN. *3-Phase LCL-Filtered Grid-Connected VSC Modeling*, doi: 10.17632/xbpchksg3k.1.

[53] S. Golestan, F. D. Freijedo, and J. M. Guerrero, "A Systematic Approach to Design High-Order Phase-Locked Loops," (in English), *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2885-2890, Jun 2015, doi: Doi 10.1109/Tpel.2014.2351262.

[54] K. J. Åström and T. Hägglund, *PID Controllers: Theory, Design, and Tuning*, 2nd ed. ISA, 1995.

[55] J. Wang, J. D. Yan, L. Jiang, and J. Zou, "Delay-dependent stability of single-loop controlled grid-connected inverters with LCL filters," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 743-757, 2016, doi: 10.1109/TPEL.2015.2401612.

[56] A. G. Yepes, F. D. Freijedo, J. Doval-Gandoy, L. Ó, J. Malvar, and P. Fernandez-Comesaña, "Effects of Discretization Methods on the Performance of Resonant Controllers," *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1692-1712, 2010, doi: 10.1109/TPEL.2010.2041256.

[57] S. a. S. Srita, S. 3-Phase LCL-Filtered Grid-Connected VSC Modeling

[58] X. Quan, "Improved Dynamic Response Design for Proportional Resonant Control Applied to Three-Phase Grid-Forming Inverter," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 10, pp. 9919-9930, 2021, doi: 10.1109/TIE.2020.3021654.

[59] O. Husev, C. Roncero-Clemente, E. Makovenko, S. P. Pimentel, D. Vinnikov, and J. Martins, "Optimization and Implementation of the Proportional-Resonant Controller for Grid-Connected Inverter With Significant Computation Delay," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 2, pp. 1201-1211, 2020, doi: 10.1109/TIE.2019.2898616.

[60] C. Tang, K. Zhou, Y. Shu, Q. He, and Q. Chen, "Analysis and Design of Multiple Resonant Current Control for Grid-Connected Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 2539-2546, 2022, doi: 10.1109/JESTPE.2021.3138934.

APPENDIX I

HARMONIC IN THREE-PHASE SYSTEM

Harmonics in a three-phase system refer to frequencies that are whole number multiples of the fundamental frequency (often 50 Hz or 60 Hz) of the power supply. These frequencies have the potential to alter the typical sinusoidal waveforms of voltage and current, resulting in a range of issues within the electrical network. Below is an analysis of the nature of harmonics in three-phase system.

Phase sequence of harmonic in a three-phase system

The phase sequence of harmonics in a three-phase system is a critical aspect that influences how harmonics interact with the power system. To gain a deeper understanding, it's crucial to explore the determination of the phase sequence and the behavior of various harmonic types in relation to their sequence:

In a three-phase power system, the fundamental frequency follows a specific phase sequence, typically A-B-C, which means that phase A reaches its peak first, followed by phase B, and then phase C. This sequence results in a clockwise rotation of the power system's magnetic field.

For harmonics, the order of the harmonic (i.e., the multiplier of the fundamental frequency) determines its sequence and properties:

1. Positive Sequence Harmonics

Harmonics of the form $n = 1 + 3k$ (where k is an integer 0, 1, 2,.) are called positive sequence harmonics, such as the 1st, 4th, 7th, 10th, etc. These harmonics follow the same sequence as the fundamental (A-B-C). They rotate in the same direction as the fundamental frequency's magnetic field and add constructively to the system's power.

2. Negative Sequence Harmonics

Harmonics of the form $n = 2 + 3k$ are called negative sequence harmonics, like the 2nd, 5th, 8th, 11th, etc. These harmonics follow the opposite sequence of the

fundamental (A-C-B). They rotate in the opposite direction and can lead to destructive interference, reducing system efficiency and potentially causing heating and mechanical stresses, particularly in rotating machinery.

3. Zero Sequence Harmonics

Harmonics of the form $n = 3 + 3k$, such as the 3rd, 6th, 9th, 12th, etc., are called zero sequence harmonics. These harmonics do not rotate and are in phase with each other across all three phases (A-A-A or B-B-B or C-C-C). In systems with a connected neutral, they can generate significant neutral current, resulting in excessive heating and neutral overloading.

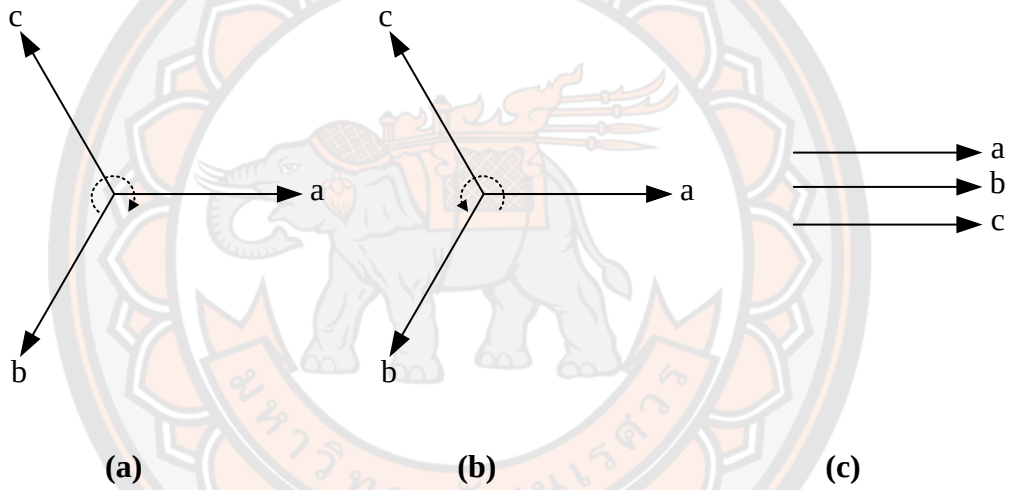


Figure A.1 Phase sequence vector of a balanced three-phase system: (a) Positive Sequence, (b) Negative Sequence and (c) Zero Sequence.

APPENDIX II

PUBLICATIONS

energies

MDPI

Article

Modeling, Simulation and Development of Grid-Connected Voltage Source Converter with Selective Harmonic Mitigation: HiL and Experimental Validations

Suparak Srita [1,2], Sakda Somkun [1,*], Tanakorn Kaewchum [1], Wattanapong Rakwichian [1], Peter Zacharias [3], Uthen Kamnarn [2], Jutturit Thongpron [2], Damrong Amorndechaphon [4] and Matheepot Phattanasak [5]

1 School of Renewable Energy and Smart Grid Technology (SGtech), Naresuan University, Phitsanulok 65000, Thailand; suparak@rmutl.ac.th (S.S.); tanakornk63@nu.ac.th (T.K.); wattanapongr@nu.ac.th (W.R.)
2 Department of Electrical Engineering, Rajamangala University of Technology Lanna, Chiang Mai 50300, Thailand; uthen@rmutl.ac.th (U.K.); jutturit@rmutl.ac.th (J.T.)
3 Department of Electrical Power Supply Systems, University of Kassel, Wilhelmshöher Allee 71, D-34121 Kassel, Germany; peter.zacharias@uni-kassel.de
4 Automotive and Transportation Technology Development Center (ATDC), School of Engineering, University of Phayao, Phayao 56000, Thailand; a_damrong@hotmail.com
5 Department of Teacher Training in Electrical Engineering, King Mongkut's University of Technology North Bangkok, Bangkok 10800, Thailand; matheepotp@kmutnb.ac.th
* Correspondence: sakdaso@nu.ac.th

Citation: Srita, S.; Somkun, S.; Kaewchum, T.; Rakwichian, W.; Zacharias, P.; Kamnarn, U.; Thongpron, J.; Amorndechaphon, D.; Phattanasak, M. Modeling, Simulation and Development of Grid-Connected Voltage Source Converter with Selective Harmonic Mitigation: HiL and Experimental Validations. *Energies* **2022**, *15*, 2535. https://doi.org/10.3390/en15072535

Academic Editor: Krzysztof Sozański

Received: 5 February 2022
Accepted: 25 March 2022
Published: 30 March 2022

Abstract: This paper elaborates on a development technique for the grid-connected voltage source converter (VSC). We propose a simulation technique in the MATLAB/Simulink environment that emulates the operation of the discrete-time controlled grid-connected VSC. The switched-circuit modeling approach is used for simulation of the power stage in the continuous-time domain with the physical unit scale. The discrete-time control algorithm is implemented in an interpreted MATLAB function in the per-unit scale, which synchronizes with the switching period. Such a control algorithm is easily translated into the C language for programing of the 32-bit C2000 DSP controller with the same regulators' parameters. The proposed platform was validated with a hardware-in-the-loop real-time simulator and with a 5-kVA 3-phase *LCL*-filtered grid-connected VSC. The discrete-time control scheme was implemented in the synchronous reference frame control with proportional-integral with multi-resonant controllers at harmonic orders 6th and 12th for suppression of the grid voltage harmonic orders 5th, 7th, 11th, and 13th. The experimental results closely agreed with the simulation results. The experimental grid currents complied with the IEEE 1547 standard thanks to the multi-resonant controllers. The proposed platform provides a smooth transition from implementation to a near-commercial prototype with a low investment cost in simulation and rapid prototyping tools. A MATLAB/Simulink VSC model is provided as an attachment of this paper.

Keywords: discrete-time control; harmonics; grid-connected inverter; modeling; voltage source converter

1. Introduction

Power electronic converters now play a vital role in modern electric power generation and distribution systems [1,2]. Three-phase voltage source converters (VSCs) are widely used to interlink DC and AC systems as illustrated in Figure 1. Common applications of the three-phase VSCs include photovoltaic [3] and wind energy systems [4], grid integration of battery storage systems [5], traction motor drives for transportation applications [6], and electric vehicle charging stations, etc. [7].

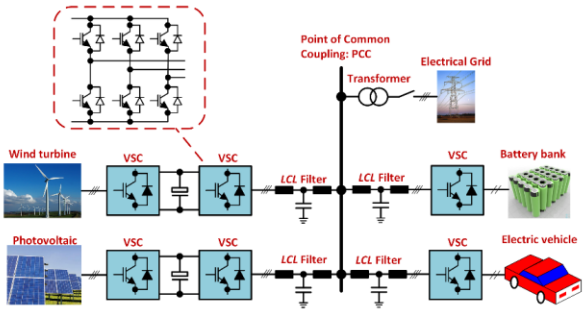


Figure 1. Applications of VSCs in the electrical system.

Figure 2 illustrates the three-phase VSC structure where it can be divided into the power stage, switching signal generation, and discrete-time control system. The DC bus voltage v_D control and the active/reactive power control are the outer control loops, which generate the reference grid current $\mathbf{i}_g^*$ for the inner current control loop. The grid current $\mathbf{i}_g$ is required to track the reference and to reject low-frequency harmonics in the grid voltage $\mathbf{v}_g$. Harmonic controllers are normally plugged into the fundamental component current controller. Multi-resonant controllers and repetitive controllers in the stationary reference frame $\alpha\beta$, and multiple synchronous reference frame control are the common solutions for grid voltage harmonic mitigation. Moreover, frequency adaptation capability is required to maintain the control performance with the grid frequency variation. The duty ratios from the current control loop are sent to the pulse width modulation (PWM) unit to generate the switching signals for the semiconductor switches of the VSC. The control scheme of the three-phase VSCs and other power converters are now normally implemented on a microcontroller (μC) or a digital signal processor (DSP).

Development of a three-phase VSC starts from a simulation using power simulation software for the power stage, PWM, control systems such as PSIM or Simscape in MATLAB/Simulink (simulation platform 1 in Figure 2). This platform provides a quick validation before hardware prototyping. Component losses and thermal behavior can be easily modeled. However, a lack of deep knowledge in modeling the converter circuit and dynamic makes it difficult when designing the controllers. Moreover, the dedicated software cost is considerably high.

The power stage of the VSC can be simulated using the switched-circuit modeling technique [8] where the state equations are calculated for every switching state herein defined as simulation platform 2 in Figure 2. The semiconductors devices are normally considered as the ideal switches without voltage drops and switching and conducting losses. This technique can be modeled with basic blocks in MATLAB/Simulink. This switched circuit model can be easily connected with other control blocks that are already available in the Simulink. Investment cost in the software license is comparatively low. However, this method requires a deep understanding of the converter operation which takes additional time and effort compared with the simulation platform 1.

After computer simulation, the control scheme can be implemented into a rapid control prototyping (RCP) system, while the power stage of the VSC can be modeled in a hardware in the loop (HiL) system, defined as prototype platform 1 in Figure 2. RCP and HiL systems are normally equipped with field-programmable gate arrays (FPGAs) or high-performance microprocessors with digital and analog interfacing, which accelerates validation of the prototype. No programming effort is required since the control block diagrams in the simulation are directly translated into the RCP system. HiL systems provide high fidelity with a small-time step for real-time simulation of the semiconductor switches and passive components. It has been reported that the ratio of the switching period to the simulation time step should be greater than 60 times for equation-based modeling and 60,000 for

physical-based modeling [9]. Common RCP systems for power electronic applications are dSPACE Microlabbox (Paderborn, Germany) [10,11] and OPAL-RT OP4510 (Montreal, QC, Canada) [12,13] and Imperix B-Box (Sion, Switzerland) [14] etc. Common commercial HiL systems are OPAL-RT OP4510 (Montreal, QC, Canada) [12], dSPACE SCALEXIO (Paderborn, Germany) [9], Typhoon HiL (Somerville, MA, USA) [15,16] and National Instruments LabVIEW FPGA (Austin, TX, USA) [17]. The VSC power stage emulated in a HiL system is easily connected with the control stage implemented in an RCP system or a DSP-based controller. Hardware simulation using HiL systems is normally used to validate control schemes for a large system such as a microgrid controller [18] or a high-power wind turbine converter [19].

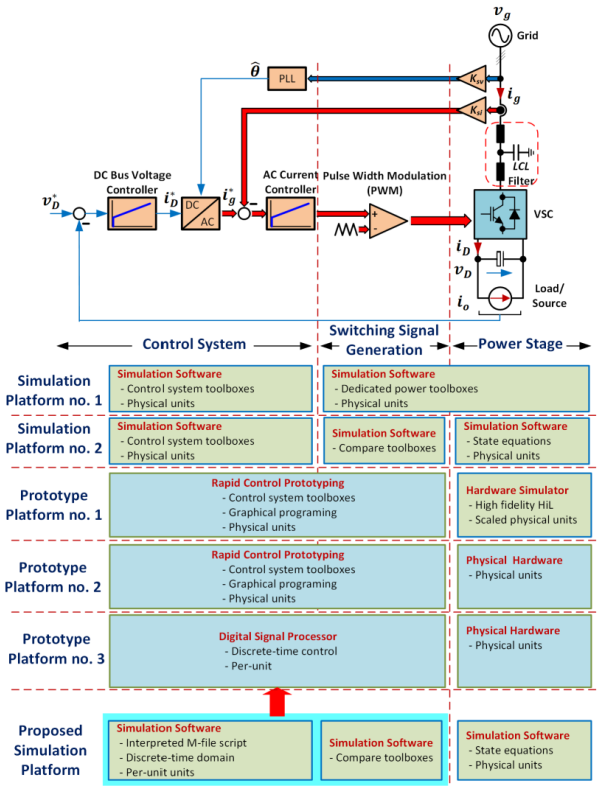


Figure 2. Development platforms of the three-phase grid-connected VSC.

The control scheme implemented in the RCP system can be connected to the physical hardware for the power converter, here defined as prototype platform 2 in Figure 2. This research platform is popular for quick verification of converter control methodologies, for which no programming effort is required. Physical units are virtually employed in such a system. Measured signals, i.e., voltages and currents are just scaled into the control block diagrams with their associated gains. Commercialization of prototype platform 2 takes further effort in the implementation of the control scheme. The control scheme is discretized and programmed onto a microcontroller or a DSP [20–24], here called prototype platform 3. The sampled currents and voltages are normally scaled into the per-unit (p.u.) system so that they are compatible with a limited numerical range of the DSP. This prototype platform 3 has a similar structure to commercial products for example power factor correction

rectifiers, grid-connected inverters, and back-back converters [2,20,24]. Thus, it takes a little effort to commercialize the prototype platform 3.

Simulation platform 1 and prototype platforms 1 and 2 enable a smooth transition from modeling to implementation with a substantial investment in simulation software, RCP systems, and HiL systems. Alternatively, simulation platform 2 and prototype platform 3 are the cheapest development platforms, which are suitable for power converter research and development in developing countries. Example products and estimated costs of the simulation and prototype platforms are summarized in Table 1.

Table 1. Example products and estimated cost for the simulation and prototype platforms.

Platforms	Products	Cost	Implementation Effort
Simulation platform 1	MATLAB/Simulink with Simscape and Simscape Electrical	11,800 USD	Little
Simulation platform 2 & proposed method	MATLAB/Simulink	5900 USD	Moderate
Prototype platform 1	dSPACE Microlabbox Associated MATLAB/Simulink products	+30,000 USD	Little
Prototype platform 2	dSPACE Microlabbox OPAL-RT OP4510 Associated MATLAB/Simulink products	+80,000 USD	Little
Prototype platform 2	Texas Instruments LaunchXL379D Power electronic hardware for 5-kVA 3-ph VSC	2000 USD	Hard

This paper illustrates a development methodology for a DSP-based control power electronic converter that facilitates a smooth transition from implementation to a near-commercial prototype without a circuit-based simulation package and an RCP tool. This paper covers switched circuit modeling of the VSC, and its discrete-time control scheme developed in the MATLAB/Simulink environment from basic block diagrams. The control scheme is scaled into the per-unit system so that the regulators' parameters can be directly transferred to the discrete-time control system implemented on a TMS320F28379D DSP controller from Texas Instruments (Dallas, TX, USA) as illustrated at the bottom of Figure 2. A three-phase grid-connected VSC with the proportional-integral plus multi-resonant (PIMR) controllers in the synchronous reference frame for mitigation of grid voltage harmonics is selected in this study. The proposed method was validated with a simulation platform 1 using the Simscape Electrical toolboxes in the MATLAB/Simulink, an HiL real-time simulator, and 5-kVA three-phase grid-connected VSC.

2. System Description

Figure 3 depicts an *LCL*-filtered three-phase grid-connected VSC with the synchronous reference frame control. The grid voltages, grid currents, and the DC bus voltage are sampled by the analog-to-digital converters (ADCs), which are represented as the zero-order hold (ZOH) blocks in the simulation. The sampled voltages are scaled by K_{SV} into the per-unit system and K_{SI} for the sampled currents. The superscript " $'$ " denotes the signals in the p.u. scale. The grid currents are transformed to the synchronous reference frame, on which the dq-axes current i'_{gd} and i'_{gq} are regulated by the discrete-time current controllers $G_{ci}(z)$ with the reference current $i'_{gd,ref}$ generated from the active power control loop and/or the DC bus voltage control loop and the reference current $i'_{gq,ref}$ obtained from the reactive power control loop or by setting $i'_{gq,ref} = 0$ for a unity power factor. The distorted grid voltages v_{ga}, v_{gb} and v_{gc} are given by

$$\left.\begin{array}{c} v_{ga}(t) = \hat{V}_1 \cos\theta + \sum_h^n \hat{V}_k \cos h\theta \\ v_{gb}(t) = \hat{V}_1 \cos(\theta - 2\pi/3) + \sum_h^n \hat{V}_k \cos h(\theta - 2\pi/3) \\ v_{gc}(t) = \hat{V}_1 \cos(\theta + 2\pi/3) + \sum_h^n \hat{V}_k \cos h(\theta + 2\pi/3) \end{array}\right\} \quad (1)$$

where $\theta = \omega t$ and ω is the grid frequency. The three-phase three-wire system contains the harmonic orders $h = 5, 7, 11, 13, \ldots$. A phase-locked loop (PLL) is used to estimate the grid voltage angle $\hat{\theta}$ for the reference frame transformation. The grid voltage in the stationary reference frame is obtained from

$$\vec{v}_{\alpha\beta} = v_{g\alpha} + jv_{g\beta} = \frac{2}{3}\left(v_{ga} + v_{gb}e^{j\frac{2\pi}{3}} + v_{gb}e^{-j\frac{2\pi}{3}}\right). \tag{2}$$

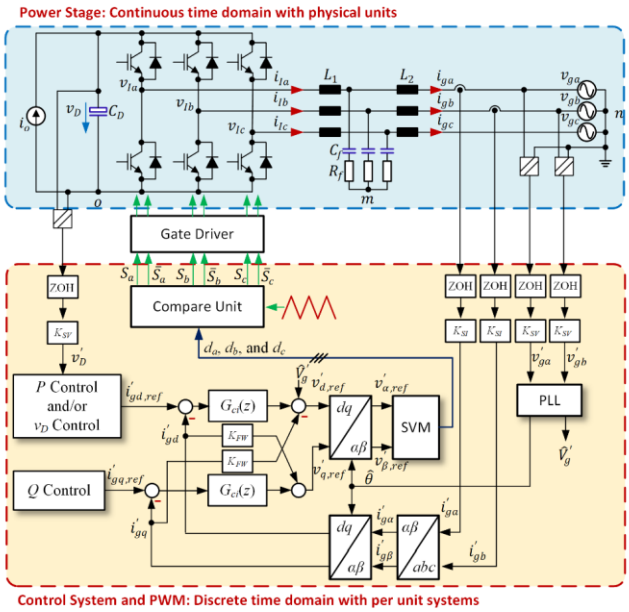


Figure 3. Three-phase grid-connected LCL-filtered VSC with the discrete-time control scheme in the synchronous reference frame.

Note that the zero-sequence is neglected for the balanced system. Substituting (1) into (2), the grid voltage can be represented as

$$\vec{v}_{\alpha\beta} = \hat{V}_1 + \hat{V}_5 e^{-j5\theta} + \hat{V}_7 e^{j7\theta} + \hat{V}_{11} e^{-j11\theta} + \hat{V}_{13} e^{j13\theta} + \cdots. \tag{3}$$

Thus, the grid voltage in the synchronous reference frame is given by

$$\vec{v}_{dq} = \vec{v}_{\alpha\beta} e^{-j\theta} = \hat{V}_1 + \hat{V}_5 e^{-j6\theta} + \hat{V}_7 e^{j6\theta} + \hat{V}_{11} e^{-j12\theta} + \hat{V}_{13} e^{j12\theta} + \cdots. \tag{4}$$

The voltage harmonic orders $\pm h = 6, 12, \cdots$ in the synchronous reference frame result from the harmonic orders $(h \pm 1)$ in the stationary reference frame, which become the disturbances of the dq-axes current control loops. The PIMR controller depicted in Figure 4 is adopted for the dq-axes current regulators [25]. The PMR transfer function in the s-domain is given by

$$G_{ci}(s) = K_p + \frac{K_{i1}}{s} + \sum_{h=6,12,\cdots} \frac{K_{ih}s}{s^2 + (h\omega)^2}. \tag{5}$$

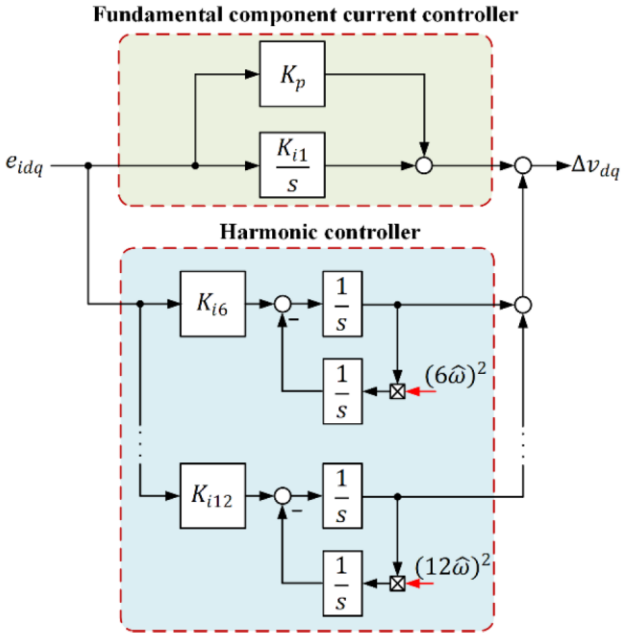


Figure 4. Proportional-integral plus multi-resonant controller.

The proportional-integral (PI) controller regulates the fundamental component current which is the DC quantities in the dq-axes. The multiple resonant (MR) controllers regulate both negative and positive sequence components [26], which can be used to attenuate the grid voltage harmonics at the frequencies $\pm 6\omega, \pm 12\omega, \cdots$ in the synchronous reference frame [25]. The double integrator structure of the resonant controllers uses the estimated grid frequency from the PLL for frequency adaptation. The equivalent transfer function of $G_{ci}(s)$ in the stationary reference frame is determined from [26].

$$G_{ci}^{s}(s) = G_{ci}(s + j\omega) + G_{ci}(s - j\omega). \tag{6}$$

Substitution of (5) into (6) becomes

$$G_{ci}(s) = K_p + \frac{2K_{i1}s}{s^2 + \omega^2} + \underbrace{\sum_{h=6,12,\cdots} \frac{2K_{ih}(s^2 + (1+h^2)\omega^2)s}{s^4 + 2(1+h^2)\omega^2 s^2 + (1-h^2)^2\omega^4}}_{H(s)}. \tag{7}$$

The harmonic compensators $H(s)$ in (7) are identical to individual resonant controllers $R(s)$ tuned at frequencies $(1 \pm h)\omega$ in the stationary reference frame which is given by

$$R(s) = \sum_{h=6,12,\cdots} \frac{K_{ih}s}{s^2 + (1 \pm h)^2\omega^2}. \tag{8}$$

Therefore, the stationary frame equivalence of the synchronous reference frame controller $G_{ci}(s)$ is similar to a proportional-multiple resonant controller implemented in the stationary reference frame [25], which is written by

$$G_{ci}^{s}(s) = K_p + \frac{2K_{i1}s}{s^2 + \omega^2} + \sum_{h=6,12,\cdots} \frac{K_{ih}s}{s^2 + (1 \pm h)^2\omega^2}. \tag{9}$$

The outputs of the dq-axes current controllers with feedforward of the decoupled terms K_{FW} form the VSC reference voltages $v'_{d,ref}$ and $v'_{d,ref}$, which are converted to the stationary reference frame $v'_{\alpha,ref}$ and $v'_{\beta,ref}$ using the inverse Park transformation given by

$$\vec{v}'_{\alpha\beta,ref} = \left(v'_{\alpha,ref} + jv'_{\beta,ref}\right) = \left(v'_{d,ref} + jv'_{q,ref}\right) \cdot e^{j\theta}. \quad (10)$$

The reference voltages $v'_{\alpha,ref}$ and $v'_{\beta,ref}$ are the inputs for the space vector modulation (SVM) which calculates the duty ratios d_a, d_b, and d_c for the compare unit to generate the VSC switching commands.

The control scheme in Figure 3 is normally implemented on a DSP, and it must be executed within an interrupt service routine (ISR). Figure 5 illustrates the timing diagram of each ISR, which starts when the PWM carrier reaches zeros or the maxima. The controller sampling frequency f_s doubles the switching frequency f_{sw}. The analog signal sampling is synchronized with the ISR at time instance k that occurs in the middle of the switching action to avoid switching noise. This requires a small filtering effort for each signal, which enhances the control loop bandwidth. The analog to digital conversion and scaling, and the PLL are executed every ISR. If the VSC operation is enabled, the other VSC control algorithms are performed, otherwise, they are skipped to the end of the ISR. The control scheme is executed within the sampling period $T_s = 1/f_s$, and the calculated duty ratios $d_a(k)$, $d_b(k)$, and $d_c(k)$ are updated to the compare unit at the next time instance $k+1$.

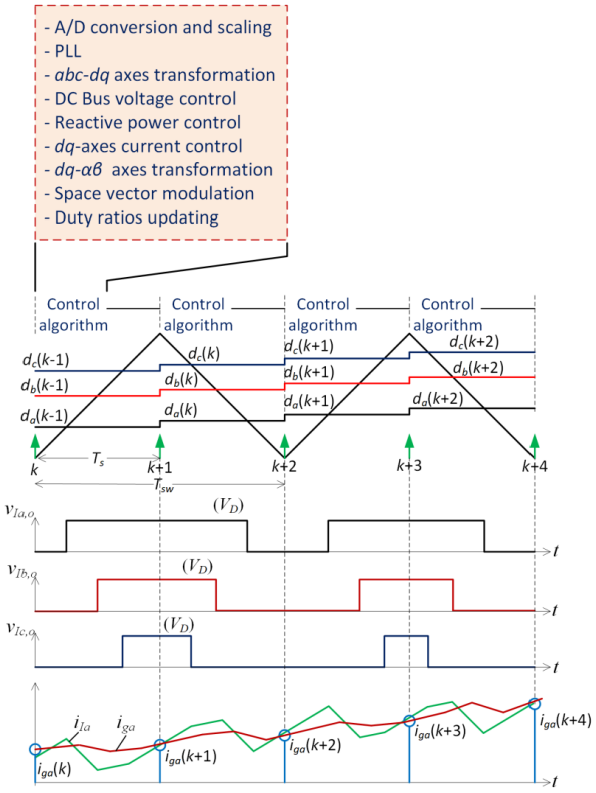


Figure 5. Timing diagram and control sequence of the VSC discrete-time control.

The VSC currents i_{Ia}, i_{Ib}, and i_{Ic} or the grid currents i_{ga}, i_{gb}, and i_{gc} can be used as the feedback signals for the current control loop. For the VSC current feedback, current sensors can be embedded in the VSC where overcurrent is directly protected. However, the injected power to the grid is not directly controlled. Moreover, the grid currents are susceptible to grid voltage harmonics [27]. Therefore, the grid currents are used for the feedback signals to directly control the injected power. The per-phase transfer function of the *LCL* filter is given by

$$G_{LCL}(t) = \frac{i_g(s)}{v_I(s)} = \frac{sC_fR_f + 1}{C_fL_1L_2s^3 + C_f(L_1 + L_2)R_fs^2 + C_f(L_1 + L_2)s}. \tag{11}$$

This yields the resonant frequency of the *LCL* filter f_{LCL} as

$$f_{LCL} = \frac{1}{2\pi\sqrt{\left(\frac{L_1L_2}{L_1+L_2}\right)C_f}}. \tag{12}$$

For the inherent damping, the sampling frequency f_s and the resonant frequency of the *LCL* filter f_{LCL} have to satisfy the stability criterion given by [28]

$$\frac{f_s}{6} < f_{LCL} < \frac{f_s}{2}. \tag{13}$$

Table 2 lists the key parameters of the VSC and the *LCL* filter in this study. This *LCL* filter is inherited damped by the inductor winding resistances R_1 and R_2, and the capacitor equivalent series resistance R_f. This results in a resonant frequency of $f_{LCL} = 5245$ Hz which satisfies the stability criterion in (13). Passive, active, or hybrid damping techniques can be used to further improve control stability with the presence of large grid impedance [29].

Table 2. Parameters of the VSC.

Parameters	Value
Nominal grid voltage	Three-phase 380 V line-line 50 Hz
Nominal power	5 kVA
Nominal DC bus voltage	650 V
DC bus capacitor, C_D	780 µF
Switching frequency, f_{sw}	10 kHz
Sampling frequency, f_s	20 kHz
DC bus resistor, R_D	94 kΩ
Converter-side inductor, L_1	1.4 mH
Winding resistance of L_1, R_1	0.110 Ω
Grid-side inductor, L_2	0.7 mH
Winding resistance of L_2, R_2	0.042 Ω
Filter capacitor, C_f	1.94 µF
Series resistor, R_f	0.001 Ω
Base voltage, V_B	311 V
Base current, I_B	10.74 A
Base impedance, Z_B	28.88 Ω

3. Modeling of the *LCL*-Filtered VSC

3.1. Switched Circuit Modeling of the Power Circuit

Figure 6 displays the equivalent circuit of the VSC. Resistors R_1 and R_2 are the winding resistance of the inductors L_1 and L_2. Resistors R_f are the equivalent series resistance of the capacitors C_f plus the series damping resistance of the *LCL* filter. Resistor R_D is the effective DC bus capacitance of the DC bus voltage sensor and the discharging resistor. The semiconductor switches are represented by switches S_a, S_b, and S_c. The status of

each switch is represented by "1" for the closed state and "0" for the opened state. The complementary switches $\overline{S}_a$, $\overline{S}_b$, and $\overline{S}_c$ operate opposite S_a, S_b, and S_c. Therefore, there are eight possible output states of the VSC. There are three reference points: m, n, and o. The DC bus current i_o is supplied or drawn by another converter, which is positive for the inverting mode and negative for the rectifying mode.

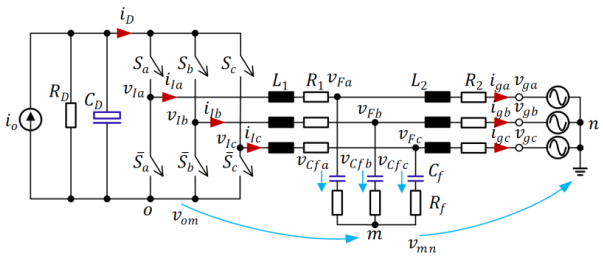


Figure 6. Equivalent circuit of the three-phase grid-connected VSC with the LCL filter.

The grid currents i_{ga}, i_{gb}, and i_{gc} can be written as follows

$$\left.\begin{aligned} L_2\frac{di_{ga}}{dt} &= (v_{Fa,m}+v_{mn})-v_{ga,n}-R_2i_{ga}\\ L_2\frac{di_{gb}}{dt} &= (v_{Fb,m}+v_{mn})-v_{gb,n}-R_2i_{gb}\\ L_2\frac{di_{gc}}{dt} &= (v_{Fc,m}+v_{mn})-v_{gc,n}-R_2i_{gc}\end{aligned}\right\}. \tag{14}$$

where $v_{Fa,m}$, $v_{Fb,m}$, and $v_{Fc,m}$ are the voltages across the filter capacitor C_f and the series resistor R_f with respect to point m, which are given by

$$\left.\begin{aligned} v_{Fa,m} &= v_{Cfa}+R_f\left(i_{ga}-i_{Ia}\right)\\ v_{Fb,m} &= v_{Cfb}+R_f\left(i_{gb}-i_{Ib}\right)\\ v_{Fc,m} &= v_{Cfc}+R_f\left(i_{gc}-i_{Ic}\right)\end{aligned}\right\}. \tag{15}$$

The voltages across the filter capacitor C_f, v_{Cfa}, v_{Cfb}, and v_{Cfc} are determined from

$$\left.\begin{aligned} C_f\frac{dv_{Cfa}}{dt} &= i_{ga}-i_{Ia}\\ C_f\frac{dv_{Cfb}}{dt} &= i_{gb}-i_{Ib}\\ C_f\frac{dv_{Cfc}}{dt} &= i_{gc}-i_{Ic}\end{aligned}\right\}. \tag{16}$$

The VSC currents i_{Ia}, i_{Ib}, and i_{Ic} are given by

$$\left.\begin{aligned} L_1\frac{di_{Ia}}{dt} &= \underbrace{(v_{Ia,o}+v_{om})}_{v_{Ia,m}}-v_{Fa,m}-R_1i_{Ia}\\ L_1\frac{di_{Ib}}{dt} &= \underbrace{(v_{Ib,o}+v_{om})}_{v_{Ib,m}}-v_{Fb,m}-R_1i_{Ib}\\ L_1\frac{di_{Ic}}{dt} &= \underbrace{(v_{Ic,o}+v_{om})}_{v_{Ic,m}}-v_{Fc,m}-R_1i_{Ic}\end{aligned}\right\}. \tag{17}$$

where the VSC voltages $v_{Ia,o}$, $v_{Ib,o}$, and $v_{Ic,o}$ with respect to point o depends on the switching states as follows

$$\left.\begin{aligned} v_{Ia,o} &= S_av_D\\ v_{Ib,o} &= S_bv_D\\ v_{Ic,o} &= S_cv_D\end{aligned}\right\}. \tag{18}$$

For the balanced three-phase three-wire system, $v_{ga,n} + v_{gb,n} + v_{gc,n} = 0$, $v_{Fa,m} + v_{Fb,m} + v_{Fc,m} = 0$, $i_{ga} + i_{gb} + i_{gc} = 0$ and $i_{Ia} + i_{Ib} + i_{Ic} = 0$, which results in

$$v_{mn} = 0. \tag{19}$$

Thus, the grid currents can be written as follows

$$\left.\begin{array}{l} L_2 \frac{di_{ga}}{dt} = v_{Fa,m} - v_{ga,n} - R_2 i_{ga} \\ L_2 \frac{di_{gb}}{dt} = v_{Fb,m} - v_{gb,n} - R_2 i_{gb} \\ L_2 \frac{di_{gc}}{dt} = v_{Fc,m} - v_{gc,n} - R_2 i_{gc} \end{array}\right\}. \tag{20}$$

Adding the sub-equations of (17) together, the common mode voltage v_{om} is expressed as

$$v_{om} = -\frac{v_D}{3}(S_a + S_b + S_c). \tag{21}$$

This common-mode voltage v_{om} intrinsically exists in the two-level VSC due to limited switching states, which creates a leakage current through the parasitic capacitance between the DC bus and the neutral points of the system. The VSC currents i_{Ia}, i_{Ib}, and i_{Ic} are driven by the differential mode voltages $v_{Ia,m}$, $v_{Ib,m}$, and $v_{Ic,m}$ between the VSC legs and the neutral point m of the capacitor bank, which can be written as

$$\left.\begin{array}{l} L_1 \frac{di_{Ia}}{dt} = \underbrace{v_D(2S_a - S_b - S_c)/3}_{v_{Ia,m}} + v_{Fa,m} - R_1 i_{Ia} \\ L_1 \frac{di_{Ib}}{dt} = \underbrace{v_D(2S_b - S_a - S_c)/3}_{v_{Ib,m}} + v_{Fb,m} - R_1 i_{Ib} \\ L_1 \frac{di_{Ic}}{dt} = \underbrace{v_D(2S_c - S_a - S_b)/3}_{v_{Ic,m}} + v_{Fc,m} - R_1 i_{Ic} \end{array}\right\}. \tag{22}$$

The VSC DC current i_D is written as

$$i_D = i_{Ia}S_a + i_{Ib}S_b + i_{Ic}S_c. \tag{23}$$

If the DC bus is connected to another converter buffered by the DC bus capacitor C_D, the DC bus voltage v_D is then modeled as

$$C_D \frac{dv_D}{dt} = i_o - i_D - \frac{v_D}{R_D}. \tag{24}$$

Figure 7a displays the VSC and *LCL* filter model developed in the MATLAB/Simulink environment, where (15), (16), (20), (22), and (23) are implemented. This model is valid when the DC bus voltage is greater than the peak value of the line-to-line grid voltage $\hat{V}_{LL}$. The signal EN is used for the enable ($EN = 1$) and disable ($EN = 0$) VSC operation. If the VSC is disabled and $v_D \geq \hat{V}_{LL}$, the VSC currents i_{Ia}, i_{Ib}, and i_{Ic} are kept reset at zero. Meanwhile, the grid currents i_{ga}, i_{gb}, and i_{gc} circulate through L_2, R_2, C_f, and R_f. At the enable time t_{EN}, the switching signals S_a, S_b, and S_c are enabled and the VSC is fully operated. Figure 7b shows the MATLAB/Simulink model of the DC bus voltage v_D in (24), which is kept reset while the VSC is disabled. For the single-stage topology where the VSC is connected to a voltage source, the DC bus voltage equation in (24) is neglected.

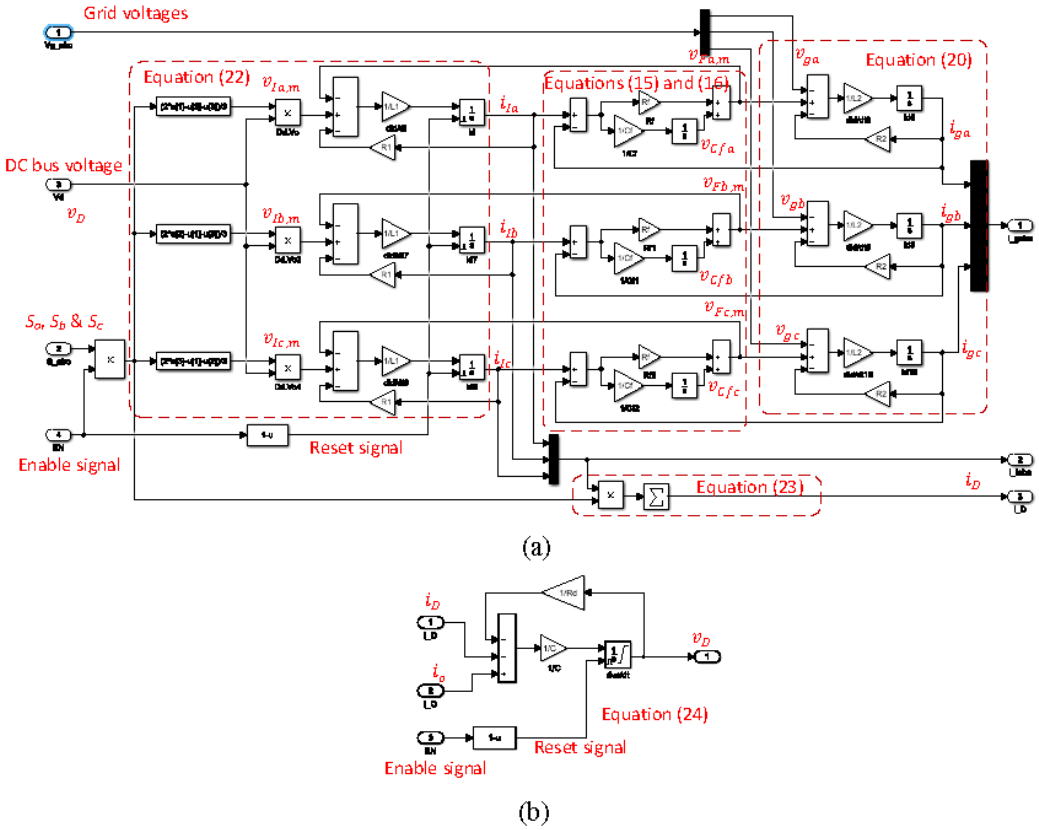


Figure 7. MATLAB/Simulink model: (**a**) the VSC and LCL filter; (**b**) the DC bus voltage.

3.2. Averaged Circuit Modeling and Current Controller Design

The frequency response of the *LCL* filter below its resonant frequency is similar to that of the *L* filter [30]. Moreover, the control bandwidth is selected below the resonant frequency of the *LCL* filter. Thus, the *LCL* filter can be approximated as the *L* filter for design of the current controller. The grid currents can be simplified as

$$\left.\begin{array}{l} L_t\frac{di_{ga}}{dt}+R_t i_{ga}=v_{1a,n}-v_{ga,n} \\ L_t\frac{di_{gb}}{dt}+R_t i_{gb}=v_{1b,n}-v_{gb,n} \\ L_t\frac{di_{gc}}{dt}+R_t i_{gc}=v_{1c,n}-v_{gc,n} \end{array}\right\} \tag{25}$$

where $L_t = L_1 + L_2$, $R_t = R_1 + R_2$. The VSC voltages are written by

$$\begin{bmatrix} v_{1a,n} \\ v_{1b,n} \\ v_{1c,n} \end{bmatrix} = \begin{bmatrix} v_{1a,m} \\ v_{1b,m} \\ v_{1c,m} \end{bmatrix} + v_{mn}. \tag{26}$$

According to (19) $v_{mn} = 0$, the grid currents in (25) become

$$\left.\begin{array}{l} L_t \frac{di_{ga}}{dt} + R_t i_{ga} = v_{Ia,m} - v_{ga,n} \\ L_t \frac{di_{gb}}{dt} + R_t i_{gb} = v_{Ib,m} - v_{gb,n} \\ L_t \frac{di_{gc}}{dt} + R_t i_{gc} = v_{Ic,m} - v_{gc,n} \end{array}\right\}. \tag{27}$$

The variables in (26) are averaged over a sampling period $T_s = f_s$ for continuous-time domain approximation, which becomes

$$\left.\begin{array}{l} L_t \frac{d\langle i_{ga}\rangle}{dt} + R_t \langle i_{ga}\rangle = \langle v_{Ia,m}\rangle - \langle v_{ga,n}\rangle \\ L_t \frac{d\langle i_{gb}\rangle}{dt} + R_t \langle i_{gb}\rangle = \langle v_{Ib,m}\rangle - \langle v_{gb,n}\rangle \\ L_t \frac{d\langle i_{gc}\rangle}{dt} + R_t \langle i_{gc}\rangle = \langle v_{Ic,m}\rangle - \langle v_{gc,n}\rangle \end{array}\right\} \tag{28}$$

where the brackets '$\langle\ \rangle$' represent the variables averaged over T_s. Equation (28) is scaled into the per-unit scale using the base voltage $V_B = I_B Z_B$ where I_B is the base current and Z_B is the base impedance, which yields

$$\left.\begin{array}{l} L_t' \frac{d\langle i_{ga}'\rangle}{dt} + R_t' \langle i_{ga}'\rangle = \langle v_{Ia,m}'\rangle - \langle v_{ga,n}'\rangle \\ L_t' \frac{d\langle i_{gb}'\rangle}{dt} + R_t' \langle i_{gb}'\rangle = \langle v_{Ib,m}'\rangle - \langle v_{gb,n}'\rangle \\ L_t' \frac{d\langle i_{gc}'\rangle}{dt} + R_t' \langle i_{gc}'\rangle = \langle v_{Ic,m}'\rangle - \langle v_{gc,n}'\rangle \end{array}\right\} \tag{29}$$

where symbols '$'$' denotes variables in the per-unit scale, and $L_t' = L_t/Z_B$ and $R_t' = R_t/Z_B$. The grid currents in (29) are transformed to the synchronous reference frame, dq axes, which results in

$$\left.\begin{array}{l} L_t' \frac{d\langle i_{gd}'\rangle}{dt} + R_t' \langle i_{gd}'\rangle = \langle v_{Id}'\rangle - \hat{V}_g' + \underbrace{\omega L_t'}_{K_{FW}} \langle i_{gq}'\rangle \\ L_t' \frac{d\langle i_{gq}'\rangle}{dt} + R_t' \langle i_{gq}'\rangle = \langle v_{Iq}'\rangle + \underbrace{\omega L_t'}_{K_{FW}} \langle i_{gd}'\rangle \end{array}\right\}. \tag{30}$$

Figure 8 shows the equivalent control block diagram of the grid current in the synchronous reference frame with the per-unit scale. Note that the cross-coupling terms $K_{FW} = \omega L_t'$ are due to the Park transformation, which can be decoupled in the control scheme. The delay terms e^{-sT_d} represent the sampling delay caused by the digital control scheme and the transport delay caused by the PWM process, where $T_d = 2T_s$ for the double update rate PWM is shown in Figure 5 [31]. The decoupled terms leave the currents i_{gd}' and i_{gq}' are separately controlled. The PI regulator for the fundamental component current is initially designed in the continuous-time domain. The parameters K_{ih} for the resonant controllers are then selected in proportion to the integral gain K_{i1}. According to the design methodology in [31], the PI regulator parameters are selected as follows

$$K_p \approx \omega_{ci,max} L_t' \tag{31}$$

$$K_{i1} \approx \frac{\omega_{ci,max}^2}{10} L_t' \tag{32}$$

where $\omega_{ci,max}$ is the possible maximum cross-over frequency at a given phase margin ϕ_{mi}. The cross-over frequency $\omega_{ci,max}$ is given by

$$\omega_{ci,max} = \frac{\pi/2 - \phi_{mi}}{T_d}. \tag{33}$$

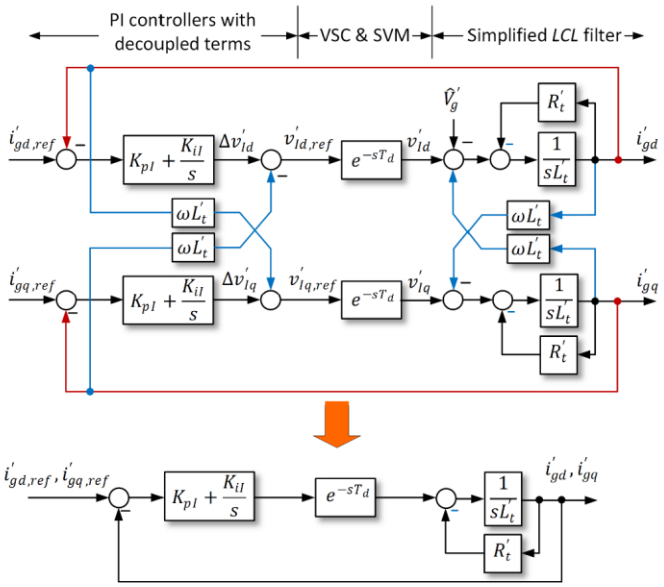


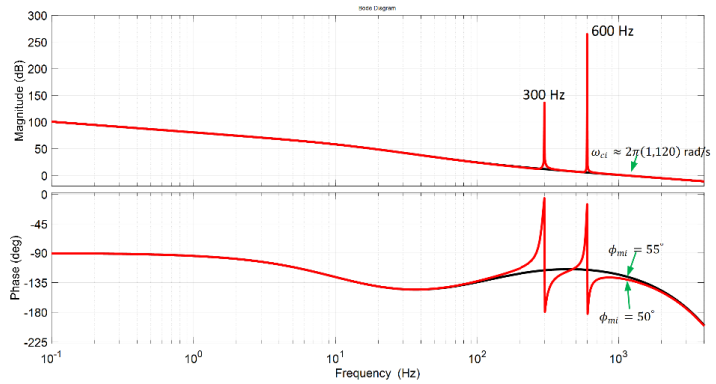
Figure 8. Equivalent block diagram of the grid current in the synchronous reference frame.

Figure 9a shows the frequency response of the simplified open-loop transfer function with the PI controller and the PIMR controller. The target phase margin is set at $\phi_{mi} = 60^{\circ}$ with the VSC parameter in Table 1, which results in $\omega_{ci,max} = 2\pi(1111)$ rad/s. The PI controller parameters K_p and K_{i1} are determined from (31) and (32). The resonant controllers, orders 6th and 12th, are added to compensate the voltage harmonics, orders 5th, 7th, 11th, and 13th, whose resonant gains are set at $K_{i6} = K_{i12} = K_{i1}/3$. For the PI controller, the DC loop gain of 100 dB is large enough to track the reference currents with a zero steady-state error. However, the loop gains at 300 Hz and 600 Hz are considerably low to reject the voltage harmonic disturbances. For the PIMR controller, the DC loop gain and the loop gains at 300 Hz and 600 Hz are greater than 100 dB. The phase margin $\phi_{mi} = 50^{\circ}$ of the system with the PIMR controller is still large enough to guarantee the control stability. The actual cross-over frequency $\omega_{ci} = 2\pi(1120)$ rad/s is close to the desired value.

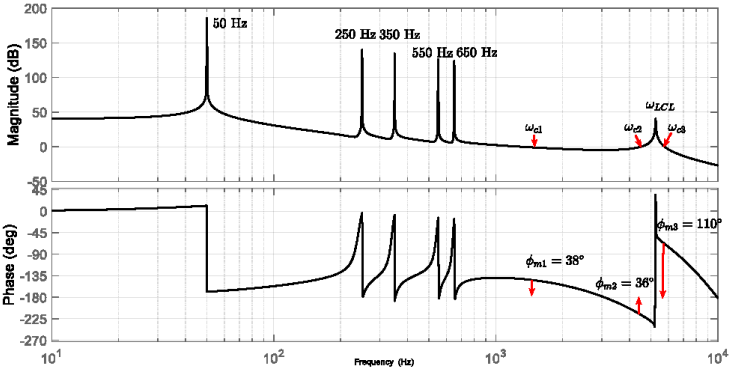
The current controller is designed based on the simplified model. Stability assessment is necessary before implementation. The stationary reference frame equivalence of the current controller given in (9) and the transfer function of the LCL filter in (11) are used in the open-loop transfer function $G_o^s(s)$ in the stationary reference frame which is written as

$$G_o^s(s) = \underbrace{G_{ci}^s(s)}_{Controller} \underbrace{\frac{V_D}{2} e^{-sTd}}_{VSC\&PWM} \underbrace{G_{LCL}(s)}_{LCL\ filter} \tag{34}$$

Figure 9b depicts the frequency response of $G_o^s(s)$ in the stationary reference frame, where there are three cross-over frequencies ω_{c1}, ω_{c2}, and ω_{c3}. The cross-over frequency near the loop bandwidth $\omega_{c1} = 2\pi(1300)$ rad/s slightly shifts from that in the synchronous reference frame due to the presence of the 13th-harmonic peak gain. The phase margin $\phi_{m1} = 38^{\circ}$ at ω_{c1} is still large enough to guarantee control stability. The other two cross-over frequencies $\omega_{c2} = 2\pi(4400)$ rad/s and $\omega_{c3} = 2\pi(5760)$ rad/s occur around the resonant frequency of the LCL filter ω_{LCL}, of which phase margins $\phi_{m2} = 36^{\circ}$ and $\phi_{m3} = 110^{\circ}$ satisfy the stability criterion for the inherent damping of the LCL filter with grid-current feedback control [28].



(a)



(b)

Figure 9. Frequency response of the current control loop: (**a**) simplified open-loop transfer function in synchronous reference frame with the PI controller (black) and the PIMR controller (red); (**b**) open-loop transfer function in the stationary reference frame.

4. Simulation

4.1. Simulation Structure

Figure 10 shows the simulation model developed in the MATLAB/Simulink environment. The simulation model emulates the experimental system, which is divided into 2 sections: continuous-time domain and discrete-time domain. The continuous-time domain represents the three-phase grid and the VSC power circuits with the switching signals S_a, S_b, and S_c as the inputs, where the switched-circuit model of the VSC and the *LCL* filter shown in Figure 7a is adopted. The single-stage topology is considered in this study where the DC bus voltage is supplied by a constant voltage source V_D. The DC bus model in Figure 7b is neglected.

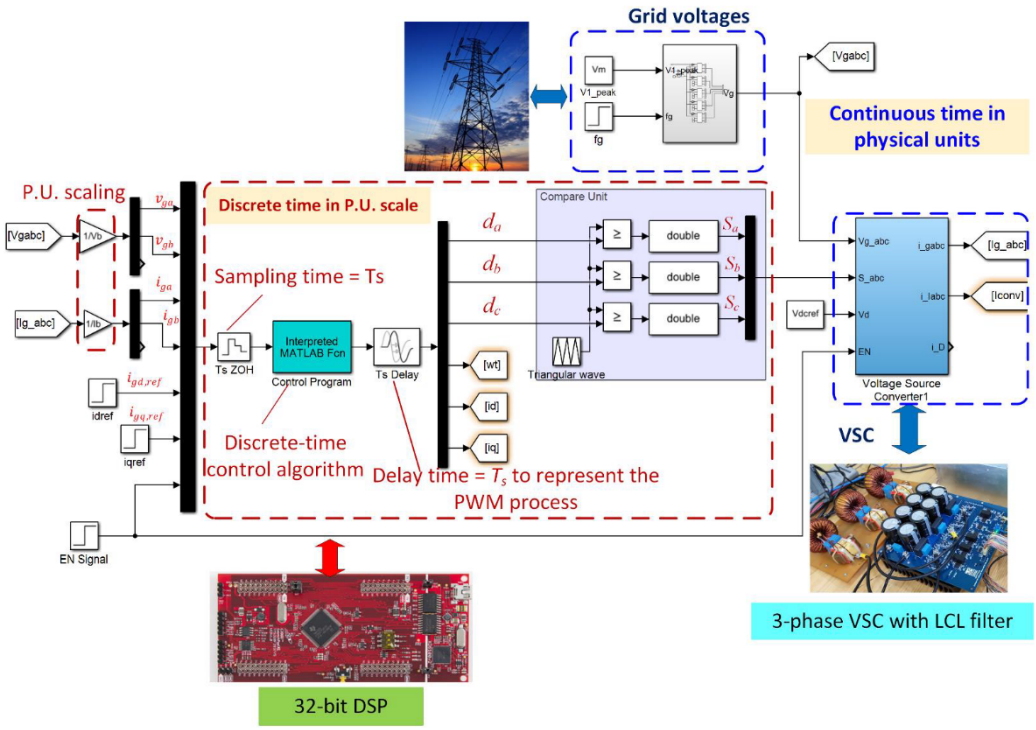


Figure 10. MATLAB/Simulink model of the discrete-time controlled 3-phase grid-connected VSC.

The discrete-time domain section emulates the control scheme depicted in Figure 3. The grid voltages v_{ga} and v_{gb}, and grid currents i_{ga} and i_{gb} are scaled by the base voltage V_B and base current I_B. Then, they are sampled by the ZOHs at the time instance k with the period of T_s. This process represents the beginning of each ISR as shown in Figure 5. The discrete-time algorithms for PLL, reference frame transformations, dq-axes current control, and the continuous SVM [32] are written in a MATLAB m file, which is executed every sampling period T_s by the interpreted MATLAB function block as shown in Figure 10. The outputs of this interpreted MATLAB function block are the duty ratios $d_a(k)$, $d_b(k)$, and $d_c(k)$, which are delayed by T_s. This causes the duty ratios $d_a(k)$, $d_b(k)$, and $d_c(k)$ to be updated at the time instance $k+1$ to compare with the triangular waveform. This waveform has the switching period T_{sw} similar to that in Figure 5, which emulates the PWM process in the DSP. Thus, the controller parameters used in the simulation can be directly transferred to the experimental system if they use the same base units. The variable-step solver ODE45 with the maximum step size of $T_s/400 = 125$ ns was selected in the Simulink setting. The proposed simulation model developed in the MATLAB/Simulink 2020b is provided in [33].

4.2. Discrete-Time Control Scheme

Figure 11 shows the Park-based PLL the discrete-time domain used for grid synchronization. The grid voltages v'_{ga}, v'_{gb}, and v'_{gc} are transformed to the $\alpha\beta$ axes using the Clarke transformation. The Park transformation converts the grid voltages to the dq axes, v'_{gd} and v'_{gq}, which are cleaned by the low-pass filters with the constant T_{PLL} for the distorted grid voltage. The integrator with a gain of the nominal grid frequency ω_{gn} estimates the grid

voltage angle $\hat{\theta}$ for the Park transformation. The PI controller regulates the q-axis voltage v'_{gqf} toward zero, which forces $\hat{\theta} \cong \theta$, $\hat{\omega}' \cong \omega/\omega_{gn}$, and $v'_{gdf} \cong \hat{V}'_g$. The loop regulator is designed in the continuous-time domain using the symmetrical optimum (SO) method [34]. For simplicity, the low-pass filters and the PI regulators are discretized using the backward difference approximation because the sampling frequency is much greater than the PLL bandwidth. The coefficient for the low-pass filters in the discrete-time domain is given by

$$\alpha_{PLL} = \frac{T_s}{T_s + T_{PLL}}. \tag{35}$$

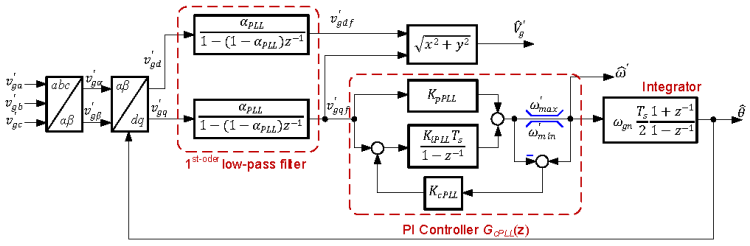


Figure 11. Park-based phase-locked loop in the discrete-time domain for grid synchronization.

The saturation limit on the PI regulator output with an anti-windup is implemented through the correction gain K_{cPLL} which is usually twice the integral gain K_{iPLL} [35]. Meanwhile, the integrator for estimation of the grid voltage angle $\hat{\theta}$ is discretized with the Tustin approximation with the lowest error. The estimated angle $\hat{\theta}$ is then used for the axis transformations.

Figure 12 illustrates the discrete-time structure of the PIMR controller for control of the dq axes currents with the controller parameters obtained from the previous section. The PI controller for the fundamental component current is discretized using the backward difference approximation. Anti-windup is also implemented with the correction gain K_c. For the resonant regulators, the forward difference approximation is used for the forward integrator, and the backward difference approximation is adopted for the feedback integrator [36]. This discretization technique is simple and does not create algebraic loops. The resonant frequency of the discrete controller is shifted from that in the continuous-time domain, especially at a higher frequency. However, it was analyzed in our previous work [37] that the shifted resonant frequency is marginal and creates an insignificant effect on the control performance. The two integrators can be discretized with the backward difference with an added one-step delay in the feedback path [36]. Discretization of both with the Tustin approximation causes a large shift of the resonant peak and poses implementation problems due to algebraic loops [36]. The resonant frequencies at the harmonic orders 6th and 12th are kept tuned with the estimated frequency $\hat{\omega}'$ from PLL for grid frequency adaptation. The fundamental current control has the intrinsic frequency adaptation capability through the Park transformation. Table 3 summarizes the parameters of the PLL and PIMR controller parameters.

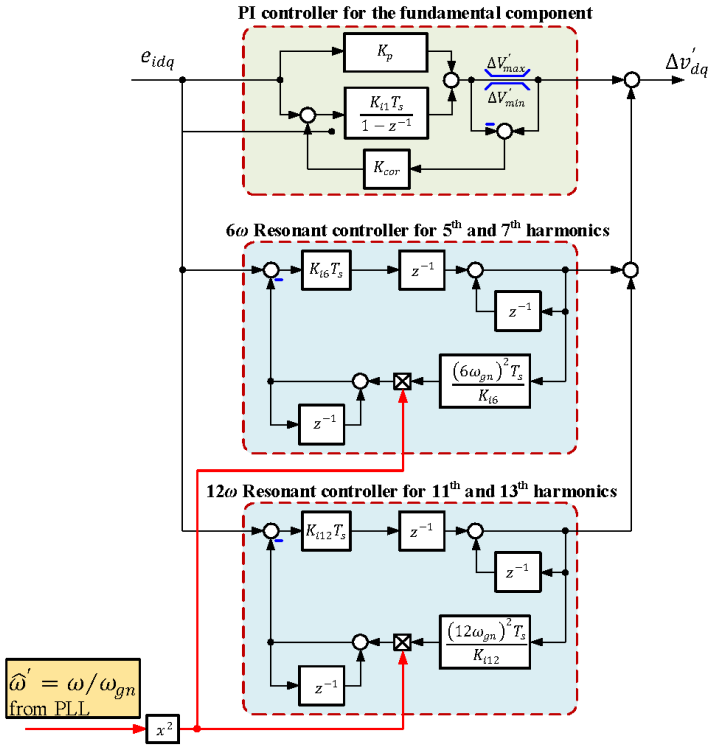


Figure 12. Discrete-time implementation of the PIMR controller.

Table 3. Parameters of the discrete-time controllers.

Parameters	PLL	dq Current Control
Bandwidth	61.3 Hz	1111 Hz
Phase margin	45°	60°
Proportional gain, K_p	1.2247	0.4922
Integral gain, K_iT_s	0.0096	0.0172
Correction gain, K_c	0.0192	0.0344
Resonant gains, K_{i6} and K_{i12}	-	114.5518
Low-pass filter, α	0.0045	-

5. Implementations

Figure 13 illustrates the experimental system. The power circuit was firstly modeled in an OPAL-RT OP4510 HiL real-time simulator with a time step of 220 ns to validate the discrete-time control scheme, which was implemented on a Texas Instruments TMS320F28379D 32-bit DSP controller as shown in Figure 13a. The emulated grid voltages and currents in the HiL system had the identical sensitivities to those used in the hardware implementation system as depicted in Figure 13b. A deadtime of 1 µs in each VSC leg was configured in the DSP. The VSC was constructed from Infineon IKW25T120 insulated-gate bipolar transistors (IGBTs) with isolated gate drivers from Texas Instruments ISO5851. Amorphous C cores (AMCC6.3 equivalence) were used for the construction of the inductors L_1 and L_2 of the *LCL* filter. The VSC was connected to a Chroma 61,860 60-kVA grid simulator. The DC bus was supplied to a Chroma 62150H-1000S DC power supply, 15 kW 0–1000 V, for the inverter operation. The discrete-time control scheme

for the hardware implementation was identical to the HiL-based validation system. The ADC voltage range of this DSP is between 0 V to 3 V. Hall-effect current sensors, LEM HLSR 10-P/SP33, were used for measurement of the grid currents i_{ga} and i_{gb}. The grid voltage sensors were constructed from voltage divider circuits with AMC1200 isolation amplifiers. In this prototype, the line-to-line voltages v_{gab} and v_{gbc} were measured, of which the instantaneous voltage vector was shifted by $-pi/6$ to be in the same angle with the instantaneous voltage vector of the phase voltage vector. A voltage reference, REF2030, provided a 1.50 V offset voltage for the grid current and grid voltage sensors.

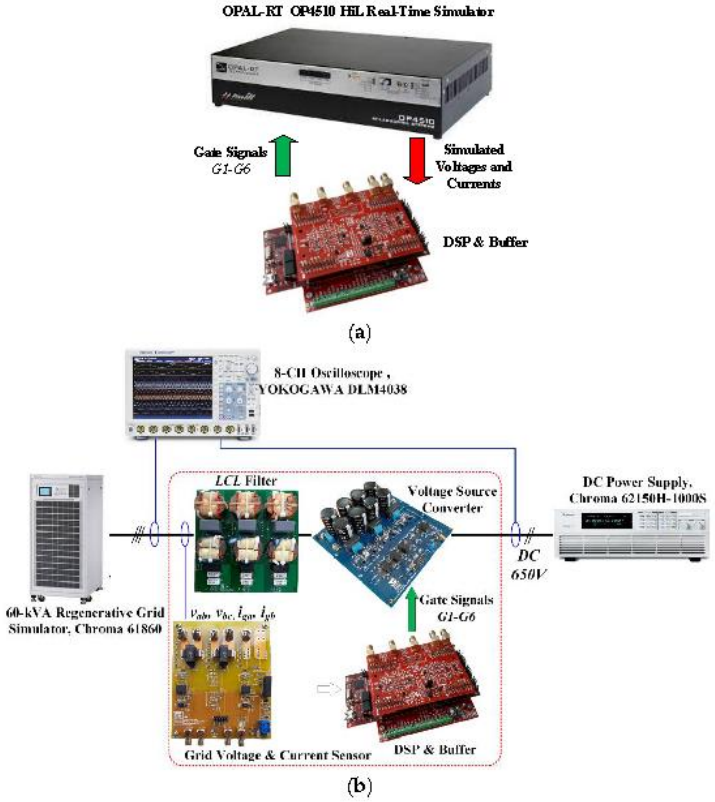


Figure 13. Experimental system of the three-phase VSC: (**a**) HiL-based implementation; (**b**) hardware implementation.

The measured voltages and currents were scaled into the per-unit system with the appropriate scaling factors as illustrated in Figure 14. In this example, a grid current with the peak value of I_B is measured by a current sensor with the sensitivity of K_{Ti}. An offset voltage $V_{OF,i}$ is added to the sensor output to accommodate the 0-$V_{ADC,max}$ input range of the ADC, where $V_{ADC,max}$ is the maximum input voltage of the ADC, normally 3 V or 3.3 V. This translates to decimal values of 0 to $\left(2^{N_{ADC}}-1\right)$, where N_{ADC} is the ADC bit number. The ADC output that is equivalent in decimal is then normalized by $2^{N_{ADC}}$. The offset is now equivalent to $V_{OF,i}/V_{ADC,max}$, which is subsequently removed in the software. The normalized signal with offset removal is multiplied by a scaling factor to have a unity amplitude at the base value. The numerical notation in the DSP can be in the signed fixed-point representation or the floating-point format. Scaling of the grid voltage

has the same process as the grid current. No offset removal is required for the DC bus voltage, while the other procedures are similar to those of the grid voltage and current. In general, the signal scaling factor is given by

$$K_s = \frac{V_{ADC,max}}{(Sensor\ Senitivity) \times (Base\ Value)}. \tag{36}$$

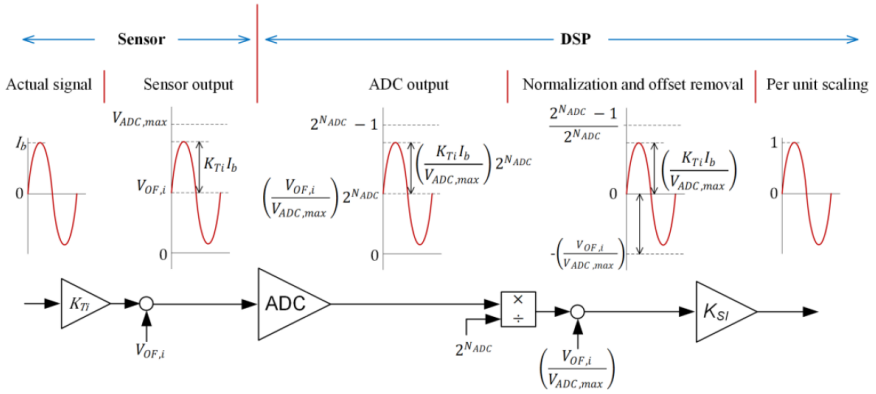


Figure 14. Grid current conversion and scaling process for the experimental system.

The discrete-time control algorithm implemented in the MATLAB m file was manually translated to the C language for the DSP with the same controller parameters. Thus, the simulation and the experiment are closely related. However, there is a code generation tool for this DSP family with an additional licensing cost. The internal signals of the discrete-time control scheme implemented on the DSP were converted to 0–3.0 V analog signals via two embedded 12-bit digital-to-analog converters (DACs) for monitoring on an oscilloscope.

6. Simulation and Experimental Validations

The DC bus was connected to the Chroma 62150H-1000S DC power supply with $v_D = 700$ V. The grid voltage waveforms were set to be sinusoidal at the nominal phase voltage of 230 V, 50 Hz. The PI controllers for the fundamental component were enabled without the harmonic compensators. The reference currents were set to $i'_{gd,ref} = 1.0$ p.u. and $i'_{gq,ref} = 0$ p.u. This caused the VSC to inject an active power of 5 kW into the grid. A simulation platform 1 of the VSC was developed in the Simscape Electrical of the MATLAB/Simulink 2020b, which is provided in [33]. Figure 15 compares the experiment and simulation results for the VSC-side currents i_{Ia}, i_{Ib}, and i_{Ic}, and the grid currents i_{ga}, i_{gb}, and i_{gc}. It can be observed the experimental VSC-side currents i_{Ia}, i_{Ib}, and i_{Ic} of the HiL and hardware implementations have the current envelops due to the switching in close agreement with those of the proposed simulation method and the simulation platform 1. This confirms that the switched circuit modeling technique is applicable for the proposed platform. The waveforms of the experimental and simulation grid currents i_{ga}, i_{gb}, and i_{gc} are near sinusoidal as the *LCL* filter absorbs the switching current ripples.

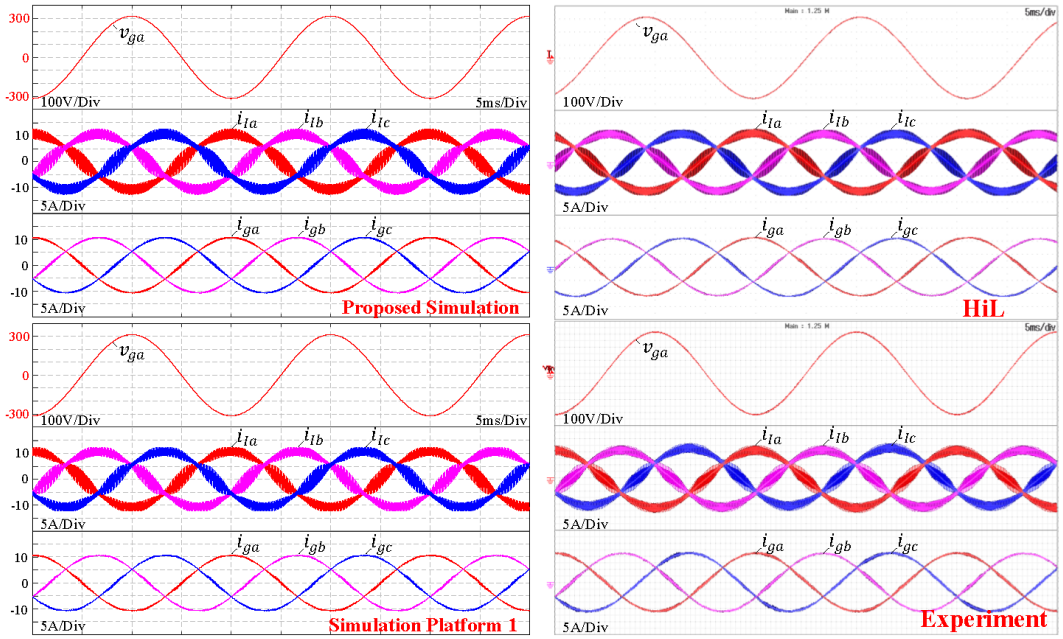


Figure 15. Simulation and experimental results of the VSC without the harmonic compensators under the sinusoidal voltages: (**a**) Proposed simulation method and simulation platform 1; (**b**) HiL-based experiment and hardware implementation.

Voltage harmonics listed in Table 4 were added to the fundamental component, which resulted in a total harmonic distortion (THD) of 4.69%. Figure 16 shows the grid voltages and the grid currents without the harmonic compensators (HC). The experimental results from the HiL and hardware implementations closely agree with the proposed simulation method and simulation platform 1. The grid voltage harmonics make the grid currents even more distorted with a THD of 10.84%. The PIMR controller was adopted for control of the VSC under the distorted grid. The PIMR controller is capable of mitigating the grid voltage distortion as depicted in Figure 17. The grid current waveforms in the steady state are near sinusoidal. The control performance is maintained when the frequency changes from 47 Hz to 50 Hz and from 50 Hz to 52 Hz through the estimated frequency $\hat{\omega}'$ from the PLL. This is the allowable frequency range for a VSC connected to the Thailand low-voltage grid [38]. Figure 18 compares the current harmonic spectrum of the VSC at the nominal power of 5 kW under the distorted grid voltage. For the PI controller without the HCs, the current harmonics, orders 5th and 7th, exceed the IEEE 1547 standard [39] and there is a significant presence of orders 11th and 13th, which reflects the grid voltage harmonics. Moreover, the 2nd harmonic current also exceeds the IEEE 1547 standard, which is believed to be due to DC offsets in the current measurement [40]. The PIMR controller effectively suppresses the grid voltage harmonics as the current harmonic orders 5th, 7th, 11th, and 13th are attenuated close to zero. The grid current with the PIMR controller has a THD of 1.08% and complies with the IEEE 1547 standard.

Table 4. Line-neutral voltage harmonics.

V_1	V_5	V_7	V_{11}	V_{13}	**THD**
220 Vrms	4%	2%	1%	1%	4.69%

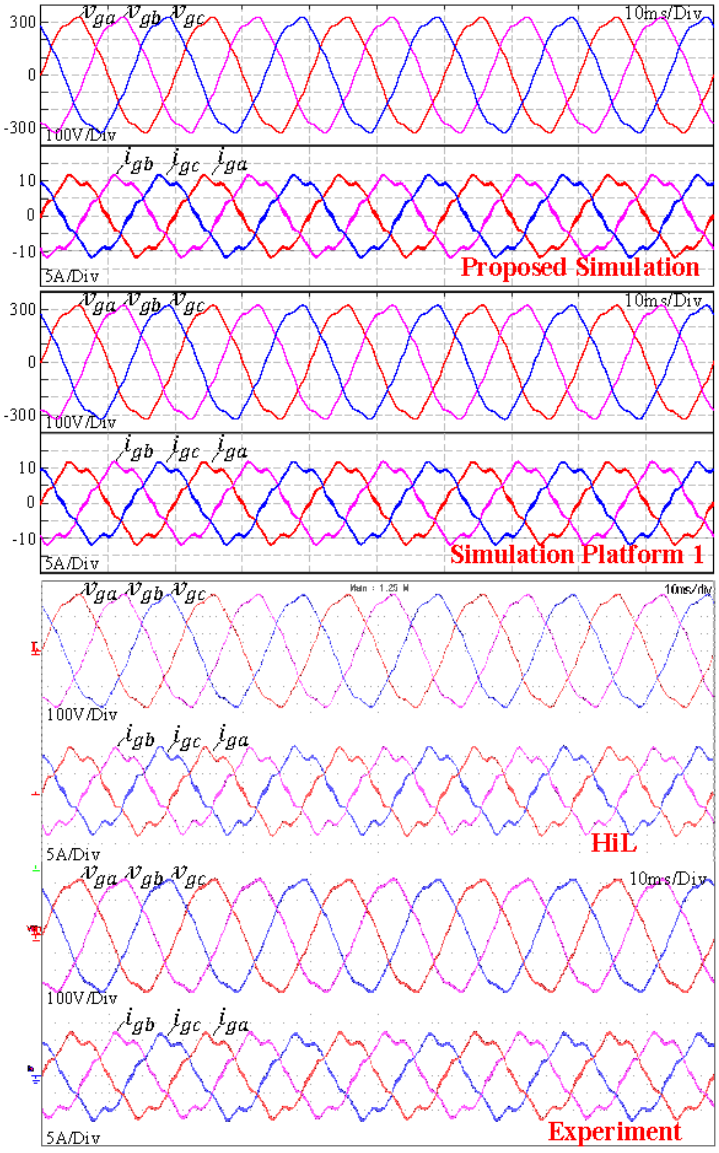


Figure 16. Simulation and experimental results of the VSC without the harmonic compensators under the distorted voltages.

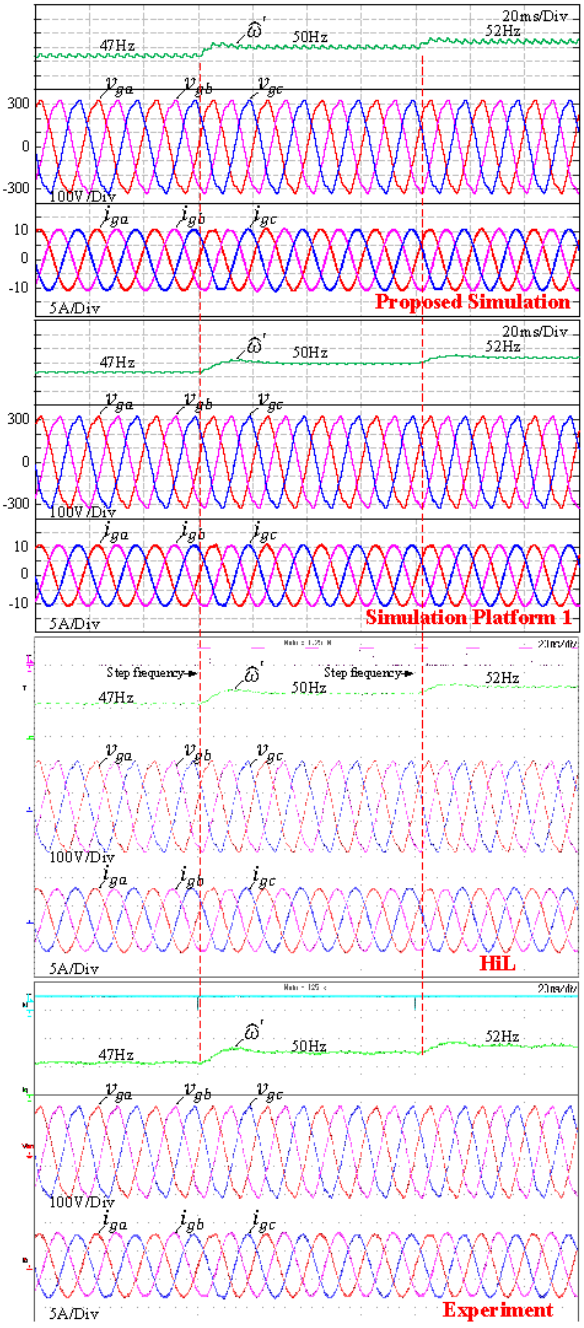


Figure 17. Simulation and experimental results of the VSC with the PIMR controller under the distorted voltages and frequency changes.

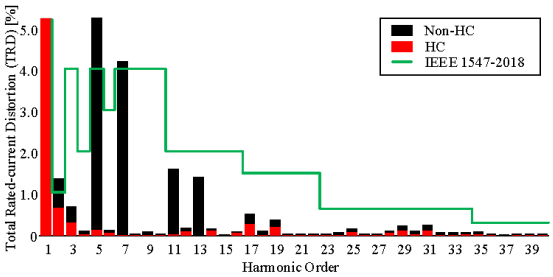


Figure 18. Current harmonic spectrum of the VSC at the nominal power of 5 kW under the distorted grid.

Dynamic performance of the VSC with the PIMR control scheme was validated with step changes in the reference currents as shown in Figure 19. The reference currents are initially set to $i'_{gd,ref} = 0$ p.u. and $i'_{gq,ref} = 0$ p.u.; the reference currents are changed to $i'_{gd,ref} = 0.7$ p.u. and $i'_{gq,ref} = 0$ p.u., and $i'_{gd,ref} = i'_{gq,ref} = 0.7$ p.u., respectively. The experimental results of the grid currents at the steady-state conditions again are close to the proposed simulation method and simulation platform 1. The rising slope of the experimental i_{ga} and i_{gc} for the HiL and hardware implementations at the step changes of the reference currents as circled in Figure 19 are slightly lower than that of the simulation. This is believed to be due to voltage drops in the IGBTs and the grid simulator's internal impedance, which were neglected in the simulation.

It is demonstrated that the proposed simulation technique mimics the converter and control scheme very closely. The results of the proposed simulation technique closely agreed with the results of the simulation platform 1 using the Simscape Electrical toolboxes in the MATLAB/Simulink 2020b, and with the experimental results of the HiL and hardware implementations. The discrete-time control scheme implemented in the interpreted MATLAB function can be easily translated to the C-code for the DSP, from which expensive RCP systems and Simulink coding toolboxes are not required. Furthermore, a HiL simulator is not necessary for the development of a low-power VSC (say up to 20 kW). This platform can be applied to other topologies. Our previous works in interleaved DC-DC converters [41], single-phase stand-alone inverter [42], and single-phase grid-connected VSCs [37,43] were developed using the proposed platform. However, validation of the control scheme with a HiL simulator or a laboratory-scale VSC is a normal practice for the development of a large power converter.

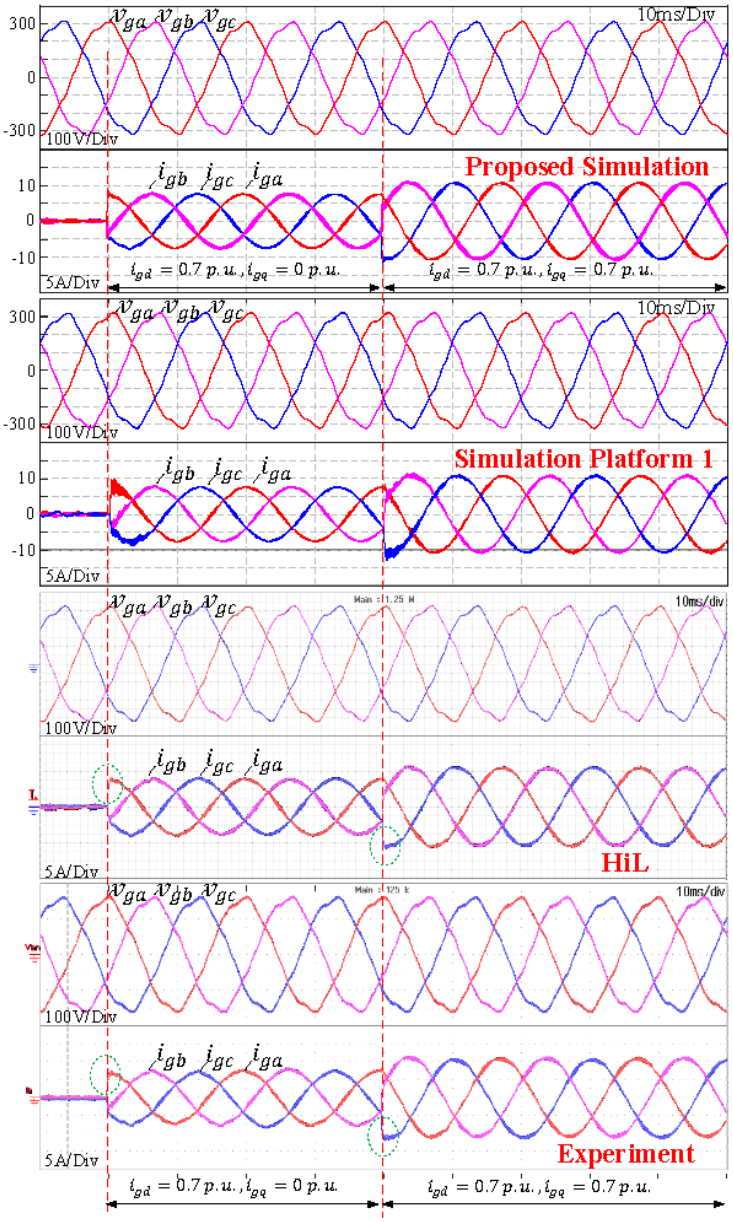


Figure 19. Transient performance of the VSC with the PIMR controller.

7. Conclusions

We propose a simulation technique that emulates the DSP-based control operation of the grid-connected converters. The key features of the proposed platform can be listed as follows.

- Switched-circuit modeling of the power circuit is simulated in the continuous-time domain with the physical unit scale.
- The discrete-time control scheme in the per-unit scale is written in a MATLAB m file function which is executed in synchronous with the switching period.
- The m-file script is then easily translated to the C code for the TMS320F28379D DSP with the same controller parameters.

The proportional-integral with multi-resonant controllers at harmonic orders 6th and 12th in the synchronous reference frame was selected in the study to attenuate the grid voltage harmonics. The proposed platform was validated with an OPAL-RT OP4510 HiL real-time simulator and with 5-kVA 3-phase *LCL*-filtered grid-connected VSC. The experimental results from the HiL simulator and the VSC closely agree with the simulation. The multi-resonant controllers were found to effectively suppress the grid voltage harmonic orders 5th, 7th, 11th, and 13th with the THD of 4.69%. The grid current was found to comply with the IEEE 1547 standard with the THD of 1.08%. The proposed platform requires a basic package of MATLAB/Simulink without dedicated power electronic toolboxes and real-time prototyping systems.

Author Contributions: Conceptualization, S.S. (Sakda Somkun), P.Z., U.K., J.T., D.A. and M.P.; methodology, S.S. (Suparak Srita); validation, S.S. (Suparak Srita); formal analysis, S.S. (Suparak Srita); investigation, S.S. (Suparak Srita); resources, S.S. (Sakda Somkun); data curation, S.S. (Suparak Srita), T.K.; writing—original draft preparation, S.S. (Suparak Srita), and S.S. (Sakda Somkun); writing—review and editing, S.S. (Suparak Srita), and S.S. (Sakda Somkun); visualization, S.S. (Suparak Srita); supervision, S.S. (Sakda Somkun); project administration, S.S. (Sakda Somkun); funding acquisition, W.R. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Naresuan University, grant number R2563C026.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The MATLAB/Simulink models presented in this study are available in "Srita, S.; Somkun, S. 3-Phase LCL-Filtered Grid-Connected VSC Modeling; Mendeley Data: 2022. https://doi.org/10.17632/xbpchksg3k.1 (accessed on 1 February 2022)".

Acknowledgments: Many thanks to PTS combination Co., Ltd., for providing an OPAL-RT OP4510 HiL FPGA real-time simulator used in this study. Suparak Srita is grateful to the Energy Policy and Planning Office (EPPO), Ministry of Energy, Thailand for sponsoring his doctoral study.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

ADC	Analog-to-digital converter
DAC	Digital-to-analog converter
DSP	Digital signal processor
FPGA	Field-programmable gate array
HC	Harmonic controller
HiL	Hardware in the loop
IGBT	Insulated-gate bipolar transistor
ISR	Interrupt service routine

MR	Multiple resonant
PI	Proportional-integral
PIMR	Proportional-integral plus multi-resonant
PLL	Phase-locked loop
PWM	Pulse width modulation
RCP	Rapid control prototyping
SO	Symmetrical optimum
SVM	Space vector modulation
VSC	Voltage source converter
ZOH	Zero-order hold
µC	Microcontroller
d_a, d_b and d_c	Duty ratios
f_s	Sampling frequency
f_{sw}	Switching frequency
f_{LCL}	Resonant frequency of the LCL filter
i_D	VSC DC current
i_{ga}, i_{gb}, and i_{gc}	Grid currents
i_{Ia}, i_{Ib}, and i_{Ic}	VSC currents
i_o	DC bus current
S_a, S_b, and S_c	VSC switching signals
T_d	PWM delay time
T_s	Sampling period
T_{sw}	Switching period
v_D	DC bus voltage
v_{Fa}, v_{Fb} and v_{Fc}	LCL filter voltages
v_{ga}, v_{gb} and v_{gc}	Grid voltages
v_{Ia}, v_{Ib} and v_{Ic}	VSC terminal voltages
θ	Angle of the grid voltage
ϕ_{mi}	Phase margin
ω	Grid angular frequency
ω_{ci}	Cross-over frequency
ω_{gn}	Nominal grid angular frequency
Subscripts	
d and q	Signals in the synchronous reference frame
ref	Refence signals
α and β	Signals in the stationary reference frame
Superscripts	
$'$	Signals in the per unit scale
Symbols	
$\hat{x}$	Peak value or estimated value
$\langle x \rangle$	averaged variables over T_s

References

1. Huang, Z.; Krishnaswami, H.; Yuan, G.; Huang, R. Ubiquitous Power Electronics in Future Power Systems: Recommendations to Fully Utilize Fast Control Capabilities. *IEEE Electrif. Mag.* **2020**, *8*, 18–27. [CrossRef]
2. Chen, M.; Poor, H.V. High-Frequency Power Electronics at the Grid Edge: A Bottom-Up Approach Toward the Smart Grid. *IEEE Electrif. Mag.* **2020**, *8*, 6–17. [CrossRef]
3. Patel, N.; Kumar, A.; Gupta, N.; Ray, S.; Babu, B.C. Optimised PI-4VPI current controller for three-phase grid-integrated photovoltaic inverter under grid voltage distortions. *IET Renew. Power Gener.* **2020**, *14*, 779–792. [CrossRef]
4. Jahanpour-Dehkordi, M.; Vaez-Zadeh, S.; Mohammadi, J. Development of a Combined Control System to Improve the Performance of a PMSG-Based Wind Energy Conversion System Under Normal and Grid Fault Conditions. *IEEE Trans. Energy Convers.* **2019**, *34*, 1287–1295. [CrossRef]
5. Peña Asensio, A.; Gonzalez-Longatt, F.; Arnaltes, S.; Rodríguez-Amenedo, J.L. Analysis of the Converter Synchronizing Method for the Contribution of Battery Energy Storage Systems to Inertia Emulation. *Energies* **2020**, *13*, 1478. [CrossRef]
6. Grasso, E.; Palmieri, M.; Mandriota, R.; Cupertino, F.; Nienhaus, M.; Kleen, S. Analysis and Application of the Direct Flux Control Sensorless Technique to Low-Power PMSMs. *Energies* **2020**, *13*, 1453. [CrossRef]
7. Sun, Q.; Lv, H.; Gao, S.; Wei, K.; Mauersberger, M. Optimized Control of Reversible VSC with Stability Mechanism Study in SMES Based V2G System. *IEEE Appl. Supercond.* **2019**, *29*, 1–6. [CrossRef]

8. Maksimovic, D.; Stankovic, A.M.; Thottuvelil, V.J.; Verghese, G.C. Modeling and simulation of power electronic converters. *Proc. IEEE* **2001**, *89*, 898–912. [CrossRef]
9. Chakraborty, S.; Mazuela, M.; Tran, D.; Corea-Araujo, J.A.; Lan, Y.; Loiti, A.A.; Garmier, P.; Aizpuru, I.; Hegazy, O. Scalable Modeling Approach and Robust Hardware-in-the-Loop Testing of an Optimized Interleaved Bidirectional HV DC/DC Converter for Electric Vehicle Drivetrains. *IEEE Access* **2020**, *8*, 115515–115536. [CrossRef]
10. Adib, A.; Mirafzal, B.; Wang, X.; Blaabjerg, F. On Stability of Voltage Source Inverters in Weak Grids. *IEEE Access* **2018**, *6*, 4427–4439. [CrossRef]
11. Xin, Z.; Wang, X.; Loh, P.C.; Blaabjerg, F. Grid-Current-Feedback Control for LCL-Filtered Grid Converters With Enhanced Stability. *IEEE Trans. Power Electron.* **2017**, *32*, 3216–3228. [CrossRef]
12. Almaguer, J.; Cárdenas, V.; Espinoza, J.; Aganza-Torres, A.; González, M. Performance and Control Strategy of Real-Time Simulation of a Three-Phase Solid-State Transformer. *Appl. Sci.* **2019**, *9*, 789. [CrossRef]
13. Chauhan, S.; Singh, B. Control of solar PV-integrated battery energy storage system for rural area application. *IET Renew. Power Gener.* **2021**, *15*, 1030–1045. [CrossRef]
14. Taul, M.G.; Wu, C.; Chou, S.F.; Blaabjerg, F. Optimal Controller Design for Transient Stability Enhancement of Grid-Following Converters Under Weak-Grid Conditions. *IEEE Trans. Power Electron.* **2021**, *36*, 10251–10264. [CrossRef]
15. Sener, E.; Ertasgin, G. Current-source 1-Ph inverter design for aircraft applications. *Aircr. Eng. Aerosp. Technol.* **2020**, *92*, 1295–1305. [CrossRef]
16. Duran, M.F. Digital Control of a Renewable Energy Resource Interfacing the Distribution Grid. Master's Thesis, Escola Tècnica Superior d'Enginyeria Industrial de Barcelona, Barcelona, Spain, 2018.
17. Estrada, L.; Vázquez, N.; Vaquero, J.; De Castro, Á.; Arau, J. Real-Time Hardware in the Loop Simulation Methodology for Power Converters Using LabVIEW FPGA. *Energies* **2020**, *13*, 373. [CrossRef]
18. Nigam, S.; Ajala, O.; Dominguez-Garcia, A.D. A Controller Hardware-in-the-Loop Testbed: Verification and Validation of Microgrid Control Architectures. *IEEE Electrif. Mag.* **2020**, *8*, 92–100. [CrossRef]
19. Salgado-Herrera, N.M.; Campos-Gaona, D.; Anaya-Lara, O.; Medina-Rios, A.; Tapia-Sánchez, R.; Rodríguez-Rodríguez, J.R. THD Reduction in Wind Energy System Using Type-4 Wind Turbine/PMSG Applying the Active Front-End Converter Parallel Operation. *Energies* **2018**, *11*, 2458. [CrossRef]
20. Zhu, D.; Zou, X.; Zhao, Y.; Peng, T.; Zhou, S.; Kang, Y. Systematic controller design for digitally controlled LCL-type grid-connected inverter with grid-current-feedback active damping. *Int. J. Electr. Power Energy Syst.* **2019**, *110*, 642–652. [CrossRef]
21. Samanes, J.; Urtasun, A.; Gubia, E.; Petri, A. Robust multisampled capacitor voltage active damping for grid-connected power converters. *Int. J. Electr. Power Energy Syst.* **2019**, *105*, 741–752. [CrossRef]
22. Said-Romdhane, M.B.; Naouar, M.W.; Belkhodja, I.S.; Monmasson, E. An Improved LCL Filter Design in Order to Ensure Stability without Damping and Despite Large Grid Impedance Variations. *Energies* **2017**, *10*, 336. [CrossRef]
23. Rodriguez-Diaz, E.; Freijedo, F.D.; Vasquez, J.C.; Guerrero, J.M. Analysis and Comparison of Notch Filter and Capacitor Voltage Feedforward Active Damping Techniques for LCL Grid-Connected Converters. *IEEE Trans. Power Electron.* **2019**, *34*, 3958–3972. [CrossRef]
24. Aravena, J.; Carrasco, D.; Diaz, M.; Uriarte, M.; Rojas, F.; Cardenas, R.; Travieso, J.C. Design and Implementation of a Low-Cost Real-Time Control Platform for Power Electronics Applications. *Energies* **2020**, *13*, 1527. [CrossRef]
25. Liserre, M.; Teodorescu, R.; Blaabjerg, F. Multiple harmonics control for three-phase grid converter systems with the use of PI-RES current controller in a rotating frame. *IEEE Trans. Power Electron.* **2006**, *21*, 836–841. [CrossRef]
26. Teodorescu, R.; Blaabjerg, F.; Liserre, M.; Loh, P.C. Proportional-resonant controllers and filters for grid-connected voltage-source converters. *IEE Proc. Electr. Power Appl.* **2006**, *153*, 750–762. [CrossRef]
27. Xin, Z.; Mattavelli, P.; Yao, W.; Yang, Y.; Blaabjerg, F.; Loh, P.C. Mitigation of Grid-Current Distortion for LCL-Filtered Voltage-Source Inverter With Inverter-Current Feedback Control. *IEEE Trans. Power Electron.* **2018**, *33*, 6248–6261. [CrossRef]
28. Wang, J.; Yan, J.D.; Jiang, L.; Zou, J. Delay-dependent stability of single-loop controlled grid-connected inverters with LCL filters. *IEEE Trans. Power Electron.* **2016**, *31*, 743–757. [CrossRef]
29. Wu, W.; Liu, Y.; He, Y.; Chung, H.S.; Liserre, M.; Blaabjerg, F. Damping Methods for Resonances Caused by LCL-Filter-Based Current-Controlled Grid-Tied Power Inverters: An Overview. *IEEE Trans. Ind. Electron.* **2017**, *64*, 7402–7413. [CrossRef]
30. Dannehl, J.; Wessels, C.; Fuchs, F.W. Limitations of Voltage-Oriented PI Current Control of Grid-Connected PWM Rectifiers With LCL Filters. *IEEE Trans. Ind. Electron.* **2009**, *56*, 380–388. [CrossRef]
31. Holmes, D.G.; Lipo, T.A.; Mcgrath, B.P.; Kong, W.Y. Optimized design of stationary frame three phase AC current regulators. *IEEE Trans. Power Electron.* **2009**, *24*, 2417–2426. [CrossRef]
32. Holmes, D.G.; Lipo, T.A. *Pulse Width Modulation For Power Converters Principles and Practice*; IEEE Press: Manhattan, NY, USA, 2003.
33. Srita, S.; Somkun, S. 3-Phase LCL-Filtered Grid-Connected VSC Modeling. Mendeley Data. 2022. Available online: https://data.mendeley.com/datasets/xbpchksg3k/1 (accessed on 1 February 2022).
34. Golestan, S.; Freijedo, F.D.; Guerrero, J.M. A Systematic Approach to Design High-Order Phase-Locked Loops. *IEEE Trans. Power Electron.* **2015**, *30*, 2885–2890. [CrossRef]
35. Åström, K.J.; Hägglund, T. *PID Controllers: Theory, Design, and Tuning*, 2nd ed.; ISA: Research Triangle Park, NC, USA, 1995.
36. Yepes, A.G.; Freijedo, F.D.; Doval-Gandoy, J.; Lopez, O.; Malvar, J.; Fernandez-Comesana, P. Effects of discretization methods on the performance of resonant controllers. *IEEE Trans. Power Electron.* **2010**, *25*, 1692–1712. [CrossRef]

37. Somkun, S. High performance current control of single-phase grid-connected converter with harmonic mitigation, power extraction and frequency adaptation capabilities. *IET Power Electron.* **2021**, *14*, 352–372. [CrossRef]
38. Provicial Electricity Authority, Provincial Electricity Authority's Regulation on the Power Network System Interconnection Code. 2016. Available online: https://www.pea.co.th/Portals/0/Document/vspp/PEA%20Interconnection%20Code%202016.pdf (accessed on 1 February 2022).
39. *IEEE Std 1547–2018 (Revision of IEEE Std 1547–2003)*; IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces; IEEE: Manhattan, NY, USA, 2018; pp. 1–138. [CrossRef]
40. Trinh, Q.N.; Wang, P.; Tang, Y.; Koh, L.H.; Choo, F.H. Compensation of DC Offset and Scaling Errors in Voltage and Current Measurements of Three-Phase AC/DC Converters. *IEEE Trans. Power Electron.* **2018**, *33*, 5401–5414. [CrossRef]
41. Somkun, S.; Sirisamphanwong, C.; Sukchai, S. A DSP-based interleaved boost DC-DC converter for fuel cell applications. *Int. J. Hydrogen Energy* **2015**, *40*, 6391–6404. [CrossRef]
42. Somkun, S. Unbalanced synchronous reference frame control of singe-phase stand-alone inverter. *Int. J. Electr. Power Energy Syst.* **2019**, *107*, 332–343. [CrossRef]
43. Somkun, S.; Chunkag, V. Unified unbalanced synchronous reference frame current control for single-phase grid-connected voltage-source converters. *IEEE Trans. Ind. Electron.* **2016**, *63*, 5425–5436. [CrossRef]

Int. J. Electron. Commun. (AEÜ) 161 (2023) 154552

Contents lists available at ScienceDirect

Int. J. Electron. Commun. (AEÜ)

journal homepage: www.elsevier.com/locate/aeue

Regular paper

Implementation and performance comparison of harmonic mitigation schemes for three-phase grid-connected voltage-source converter under grid voltage distortion: HiL and experimental validation

Suparak Srita [a,b], Sakda Somkun [a,*]

[a] School of Renewable Energy and Smart Grid Technology, Naresuan University, Phitsanulok, 65000, Thailand
[b] Electrical Engineering Department, Rajamangala University of Technology Lanna, Chiang Mai, 50300, Thailand

ARTICLE INFO

Keywords:
Multi-resonant controllers (MR)
Multiple synchronous reference frame (MSR) controllers
Harmonic compensators (HCs)
Voltage-source converter (VSC)
Hardware-in-the-loop (HiL)
LCL-filter

ABSTRACT

This paper presents an implementation methodology for a current harmonic compensation technique of three-phase grid-connected voltage-source converter (VSC), which was applied under the grid voltage distortion and frequency variation. The proportional–integral plus multi-resonant controllers (PIMR) were used to mitigate the high-order harmonic current. The harmonic compensators were used in the synchronous reference frame at harmonic orders 6th and 12th for suppression of the grid voltage harmonic orders 5th, 7th, 11th, and 13th with a total harmonic distortion of 4.69%. The PIMR controller was transformed to the discrete-time domain and implemented on a TMS320F28379D digital signal processor. The PIMR controller was compared with the conventional multiple synchronous reference frame (PIMSR) controller. The two control schemes were validated with a hardware-in-the-loop (HiL) and with a 5 kW three-phase *LCL*-filtered grid-connected VSC. The PIMR and PIMSR controllers exhibited excellent harmonic rejection on the grid current with a total harmonic distortion close to 1%, which complied with the IEEE 1547 standard. The grid current can track the reference command with a fast dynamic response. Moreover, the PIMR controller consumed a computational time of 1.625 μs, 35% of the PIMSR controller.

1. Introduction

Distributed generation (DG) powered by renewable energy sources has gained more popularity due to the limited fossil fuel sources. Power electronic converters have been the crucial parts in interfacing DG with renewable energy resources [1–5]. Voltage-source converters (VSCs) are the most popular topology in DG systems for AC–DC power conversion with a bidirectional power flow. The VSCs play a vital role in low voltage grid-connected applications such as photovoltaic grid-connected inverters [6], EV chargers [7], battery energy storage systems, and active power filters. Meanwhile, the increasing energy demand has imposed problems on the grid, such as grid stability and power quality. Moreover, nonlinear loads such as diode/thyristor rectifiers cause power quality problems due to harmonic currents injected into the grid, which causes voltage distortions at the point of common coupling (PCC) due to the presence of the grid impedance. This effect is significantly prominent if the nonlinear loads are connected far from the distributed transformer [8,9].

The VSC is usually controlled to feed currents with low-order harmonics in compliance with standards such as IEEE 1547-2018 [10]. However, grid voltage harmonics are the disturbances of the VSC'os grid current control loop, which distorts the VSC currents injected into the grid. Furthermore, the grid current harmonics become more pronounced when the frequency deviates from the nominal grid frequency [11,12]. Thus, harmonic current (HC) controllers with a frequency adaptation capability are essential for the VSC operated under grid voltage distortion.

Proportional–integral (PI) regulators implemented on the synchronous reference frame are widely employed in the VSC current control thanks to the zero-steady state error, power decoupled capability, and adaptation with the inherent grid frequency through the axis transformations [13–16]. However, the grid current waveforms distort when the grid voltages contain harmonic components. Therefore, integral regulators on the multiple synchronous reference frames at selective harmonic frequencies implemented in parallel with the fundamental controller successfully attenuate the grid voltage harmonics [17,18]. This multiple synchronous reference frame control is herein called the PIMSR control, which has been reported in the active power filter [17,19–23], grid-forming inverter [24], and grid-connected inverter applications [25,26]. However, the PIMSR control requires a large

* Corresponding author.
E-mail address: sakdaso@nu.ac.th (S. Somkun).

https://doi.org/10.1016/j.aeue.2023.154552
Received 25 October 2022; Accepted 18 January 2023
Available online 20 January 2023

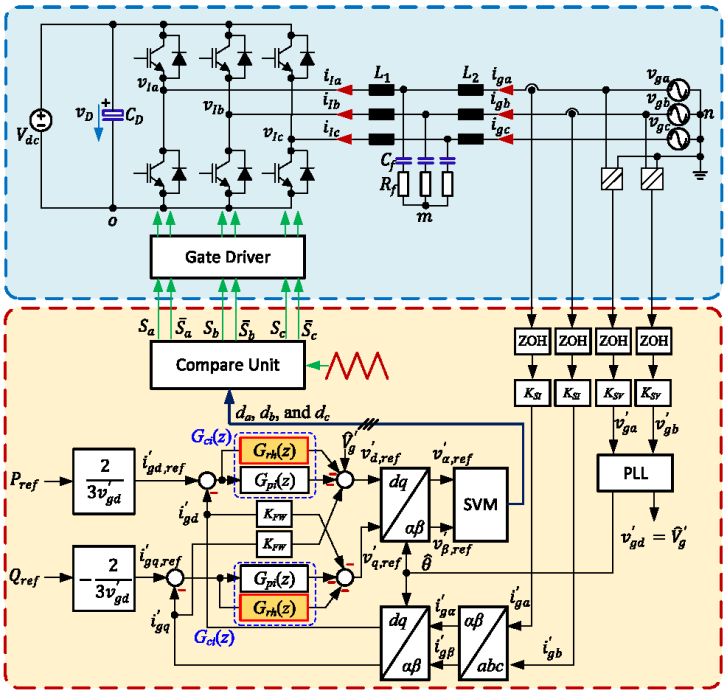


Fig. 1. Diagram of a three-phase grid-connected voltage-source converter with the harmonic compensation of the current control loop.

number of axis transformations, which poses a heavy computational burden on a digital signal processor (DSP) [17,25].

Proportional-resonant (PR) regulators implemented on the stationary reference frame are also widely employed in the VSC current control loop, which provides a zero steady-state error [27–30]. The PR controllers are used for the control of both the single-phase system and the three-phase system [11,27,31]. This stationary frame PR control demands a low computation resource. The PR regulator has to be implemented with a damping coefficient to maintain the control performance with the variable grid frequency [32]. Therefore, the resonant regulator with the double integrator structure is adopted to adapt the resonant frequency with the grid frequency employing the estimated frequency from the phased-locked loop (PLL) [33–35]. However, the current components in the stationary frame with the PR control lack the instantaneous active and reactive power extraction capability, which requires an additional power calculation scheme. Selective harmonic mitigation is achieved by adding multiple resonant controllers in parallel with the fundamental component controller, which is herein called the proportional-multiple-resonant (PMR) controller. A repetitive controller (RC) based on the internal model principle is another stationary reference frame controller suitable for periodic signals. The RC controller is equivalent to a set of multiple resonant regulators, which has been applied for the single-phase and three-phase VSCs [11,36,37]. However, frequency adaptation capability is the main drawback of the RC regulator. Therefore, complicated measures such as multi-rate sampling techniques or using Lagrange interpolating-polynomial-based filters have been proposed for the RC regulator [11].

Proportional–integral plus multi-resonant (PIMR) controllers implemented on the synchronous reference frame were proposed in [27]. The PI controllers in the dq-frame regulate the fundamental component currents. Meanwhile, the harmonic components $(1\pm h)$ in the stationary reference frame are translated to orders $\pm h$ in the synchronous reference frame, where $h = 6, 12, \cdots$. Each resonant controller regulates the input signal both in the positive and negative sequences. Therefore, the PIMR control scheme employs a smaller number of resonant regulators than the PMR scheme on the stationary reference frame. Moreover, the power decoupling property is preserved due to the implementation in the synchronous reference frame. The frequency adaptation capability is also maintained if the resonant controllers are implemented with the double-integrator structure.

This paper evaluates the implementation and control performance of the PIMR controllers on the synchronous reference frame for current control of the three-phase grid-connected LCL-filtered VSC under grid voltage distortion and grid frequency variation as shown in Fig. 1. Controller design, stability analysis, and discrete-time implementation are elaborated. The PIMR control scheme was compared with the conventional PIMSR control method. The two control schemes were both implemented on a 32-bit TMS320F28379D microcontroller. Computational burdens of the two control schemes on the TMS320F28379D microcontroller were estimated. A hardware-in-the-loop (HiL) real-time simulator and a 5-kVA insulated-gate bipolar transistor (IGBT) VSC validated the performance of the PIMR and PIMSR control systems.

2. Implementation of current control techniques for three-phase VSC

2.1. Proportional–integral plus multi-resonant (PIMR) controllers

The PIMR control scheme in Fig. 2(a) shown the dq-frame current controllers G_{ci}, which is used to control the dq-frame current i'_{gd}

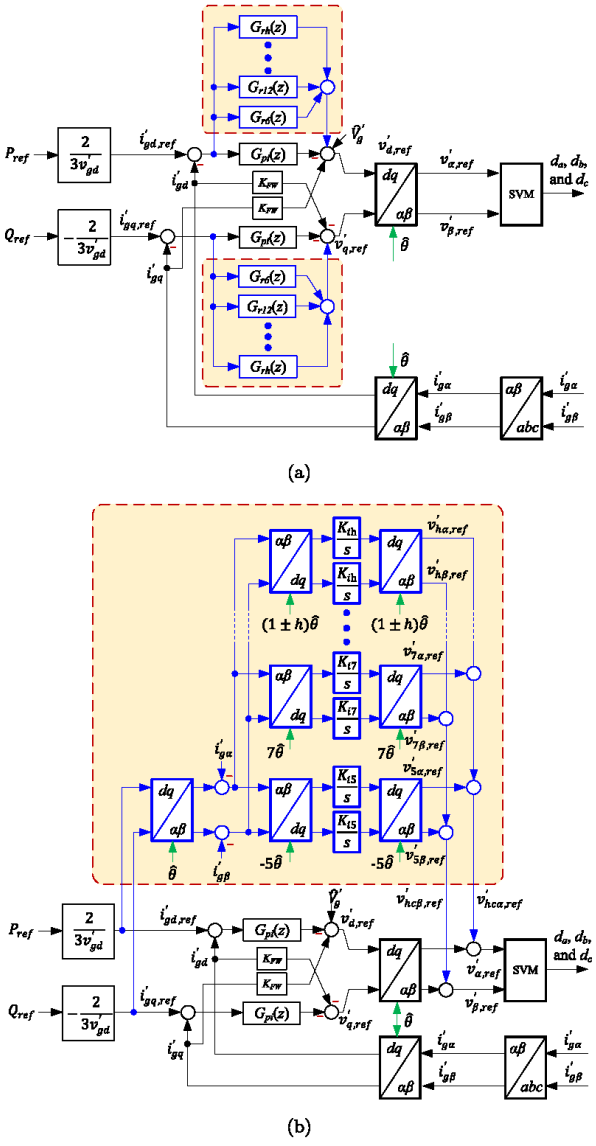


Fig. 2. The grid current control schemes used in this study. (a) PIMR scheme. (b) PIMSR scheme.

and i'_{gq}. The superscript "′" denotes the signals in p.u. scale. The proportional–integral (PI) controller regulates the DC quantities caused by the transformation of the fundamental component currents into the dq-axes. The multi-resonant (MR) controllers regulate the AC quantities of both negative and positive sequence components in dq-frame [27, 32], which is used to eliminate harmonic currents caused by the distorted grid voltage. The PIMR transfer function in the continuous-time domain is given by

$$G_{ci}(s) = \underbrace{K_p + \frac{K_{i1}}{s}}_{G_{pi}(s)} + \underbrace{\sum_{h=6,12,\ldots} \frac{K_{rh}s}{s^2 + \left(h\omega_n\right)^2}}_{G_{rh}(s)} \tag{1}$$

where K_p and K_{i1} are the proportional and integral gains of the fundamental component controller, K_{rh} is the resonant gain of each

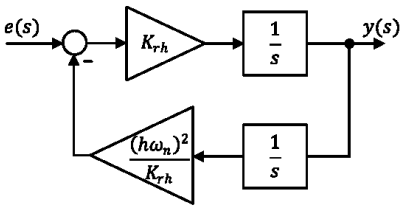


Fig. 3. The double integrator structure of resonant controller in continuous time-domain.

HC, and ω_n is the nominal grid frequency. The stationary frame equivalence $G^s_{ci}(s)$ of the synchronous reference frame controller $G_{ci}(s)$ is determined from

$$G^s_{ci}(s) = G_{ci}(s + j\omega_n) + G_{ci}(s - j\omega_n). \tag{2}$$

Substitution of (1) into (2) leads to

$$G^s_{ci}(s) = \underbrace{K_p + \frac{2K_{i1}}{s^2 + \omega_n^2}}_{G^s_{pi}(s)} + \underbrace{\sum_{h=6,12,\ldots} \frac{K_{rh}s}{s^2 + (1 \pm h)^2\omega_n^2}}_{G^s_{rh}(s)}. \tag{3}$$

The fundamental component controller $G^s_{pi}(s)$ of (3) regulates the fundamental component currents. Meanwhile, the HCs $G^s_{rh}(s)$ suppress the grid voltage harmonic orders $(1 \pm h)$ of the balanced three-phase system.

2.2. Proportional–integral plus multiple synchronous reference frame (PIMSR) controllers

Fig. 2(b) shows the PIMSR control structure, which has the same characteristic as the PIMR controller in the stationary frame [27]. The PIMSR scheme has a fundamental current controller identical to that of the PIMR control scheme. However, the selective HCs are implemented with the integral regulators in the synchronous reference frames corresponding to the grid voltage harmonic components [17,19–23]. As seen in Fig. 2(b), the reference currents $i'_{gd,ref}$ and $i'_{gq,ref}$, obtained from the active and reactive power commands, are converted to the stationary reference frame by the inverse Park transformation for the harmonic compensators. The reference currents $i'_{gq,ref}$ is obtained from the reactive power control loop or by setting $i'_{gq,ref} = 0$ for a unity power factor. The grid currents $i'_{g\alpha}$ and $i'_{g\beta}$ are determined from two grid current sensors using the Clarke transformation as follows $i'_{g\alpha} = i'_{ga}$, $i'_{g\beta} = (i'_{ga} + 2i'_{gb})/\sqrt{3}$. Then, the grid current errors in the $\alpha\beta$-axes are converted into the dq-axes again using both the positive-sequence and negative-sequence transformations at the harmonic orders $(1 \pm h)$ using the grid angles $(1 \pm h)\theta$ obtained from PLL. The dc component errors of each order in the dq-axes are then compensated by the integral regulators on the multiple synchronous reference frames at the selective harmonic frequencies. The integral regulator's outputs are transformed to the stationary reference frame using inverse Park transformation. Finally, the VSC reference voltage of the harmonic compensators $v'_{HC\alpha\beta,ref}$ are obtained by adding together all the integral regulators given by

$$\vec{v}'_{HC\alpha\beta,ref} = \sum_{h=5,7,\ldots} \left(v'_{h\alpha,ref} + jv'_{h\beta,ref}\right) = \sum_{h=5,7,\ldots} \left(v'_{hd,ref} + jv'_{hq,ref}\right) \cdot e^{jh\theta}. \tag{4}$$

The reference voltages in the $\alpha\beta$-frame of the harmonic compensators are then combined with those of the fundamental component controller.

2.3. Current controller design

The PIMR and PIMSR control schemes are identical in the stationary reference frame. Thus, they can apply the same control design methodology. In this study, the fundamental component controller is designed in the frequency domain using the design methodology in [38]. The stationary frame open-loop transfer function of the LCL-filtered VSC can be written as

$$G^s_o(s) = \underbrace{G^s_{ci}(s)}_{\text{Controller}} \cdot \underbrace{\frac{V_{dc}}{2} e^{-sT_d}}_{\text{VSC\&PWM}} \cdot \underbrace{G_{LCL}(s)}_{\text{LCL-filter}} \tag{5}$$

where $G_{LCL}(s)$ is the transfer function of the LCL filter given by

$$G_{LCL}(s) = \frac{i_{gabc}}{v_{Iabc}} = \frac{sC_fR_f + 1}{C_fL_1L_2s^3 + C_f(L_1 + L_2)R_fs^2 + C_f(L_1 + L_2)s}. \tag{6}$$

The loop bandwidth is normally chosen to be lower than the resonant frequency of the LCL filter. Thus, the LCL filter can be simplified as the L filter below [39]

$$G_{LCL}(s) \approx \frac{1}{sL_t + R_t}. \tag{7}$$

where L_t is total inductance of the filter $L_1 + L_2$. The simplified LCL filter in (7) leads to the open-loop transfer function in the dq-axes as

$$G_o(s) \approx \underbrace{K_p + \frac{K_{i1}}{s}}_{\text{Controller}} \cdot \underbrace{\frac{V_{dc}}{2} e^{-sT_d}}_{\text{VSC\&PWM}} \cdot \underbrace{\frac{1}{sL_t + R_t}}_{\text{LCL-filter}} \tag{8}$$

According to [38], the parameter K_p and K_{i1} of the PI controller for fundamental component current obtain as follows

$$K_p \approx \omega_{ci,max}\frac{L_t}{Z_b} \tag{9}$$

$$K_{i1} \approx \frac{\omega^2_{ci,max}L_t}{10Z_b}. \tag{10}$$

where $Z_b = V_b/I_b$ is the impedance base in per-unit scale with the base voltage V_b and base current I_b. Meanwhile, $\omega_{ci,max}$ is the maximum cross-over frequency at a chosen phase margin ϕ_{mi}, which is given by

$$\omega_{ci,max} = \frac{\pi/2 - \phi_{mi}}{T_d} \tag{11}$$

where $T_d = 2T_s$ is the sampling and the transport delays caused by the digital control process with T_s as the sampling time. The resonant controllers' gains of the PIMR scheme, orders 6th and 12th, are added to eliminate the voltage harmonics, orders 5th, 7th, 11th, and 13th, whose resonant gains are set at $K_{r6} = K_{r12} = K_{i1}/3$. The integral gains of the PIMSR controller are then set at $K_{i5} = K_{i7} = K_{i11} = K_{i13} = K_{i1}/3$.

2.4. Stability analysis

Table 1 summarizes the parameters of the VSC and controllers. The fundamental component was designed from the simplified transfer function given in (8) with a conservative phase margin of 60°. Fig. 4 compares the Bode diagrams of the simplified open-loop transfer function with the fundamental component and the PIMR controllers. The fundamental component controller exhibits a DC loop gain of 100 dB which is large enough to track the reference currents with a zero steady-state error. For the PIMR controller, the DC loop gain and the loop gains at harmonic orders 6th and 12th are greater than 100 dB. Meanwhile, the phase margin of PIMR controller is 48°which is still large enough to guarantee control stability.

Fig. 5 illustrates the frequency response of the stationary frame open-loop transfer function plotted from (5), which is applied for the PIMR and PIMSR controllers. The full-order transfer function of the LCL filter in (3) and (6) are considered in this analysis. The magnitudes at resonant peaks at orders 5^5, 7^7,^{11}, and 13^{13} are greater than 100 dB, which will suppress the corresponding voltage harmonics. The phase

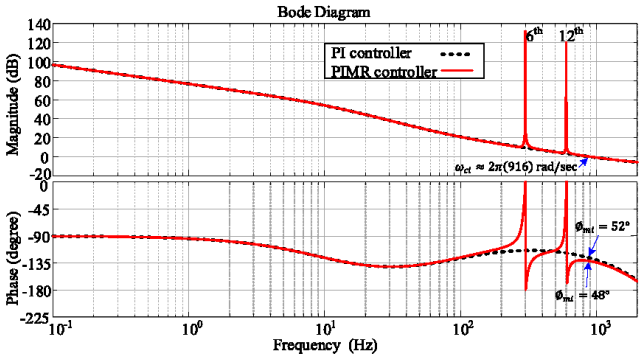


Fig. 4. Frequency response of the simplified open-loop transfer function.

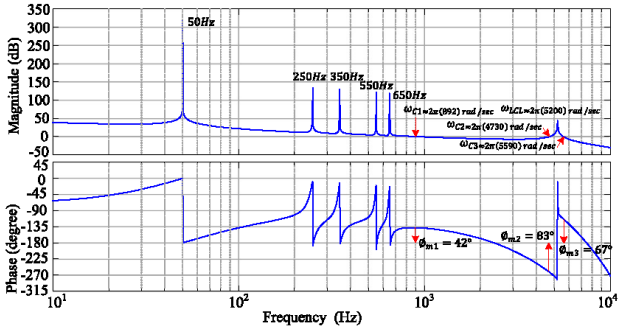


Fig. 5. Frequency response of the stationary reference frame open-loop transfer function.

Table 1
The VSC parameter.

Parameters	Value
Nominal grid voltage	Three-phase 380V_{LL}, 50 Hz
Converter-side inductor, L_1	1.5 mH
Winding resistance of L_1, R_1	0.11 Ω
Grid-side inductor, L_2	0.75 mH
Winding resistance of L_2, R_2	0.042 Ω
Filter capacitor, C_f	2 μF
Series resistor, R_f	0.001 Ω
DC bus capacitor, C_D	780 μF
Switching frequency, f_{sw}	10 kHz
Sampling frequency, f_s	20 kHz
Base voltage, V_b	310.27 V
Base current, I_b	10.74 A
Base impedance, Z_b	28.89 Ω
K_p	0.4079
K_{i1}	213.59
$K_{i5}, K_{i7}, K_{i11}, K_{i13}$	71.20
K_{r5}, K_{r12}	71.20
a_{26}, a_{212}	0.003560
a_{36}	2.495232
a_{312}	9.980928

margin ϕ_{m1} =42°is still sufficient to guarantee the stability. Moreover, there are two phase margins ϕ_{m2} =83°and ϕ_{m3} =67°around the resonant frequency of the LCL filter, which satisfies the stability criterion of the grid current feedback control [33].

2.5. Implementation of the current controllers with HCs

The PI regulators of the fundamental current controller and the integral regulators of the PIMSR controllers were discretized using the backward Euler approximation. The resonant controller transfer function of $G_{rh}(s)$ is constructed from the double integrator configuration as shown in Fig. 3. For the discrete-time transformation of the resonant controller, the forward Euler method $s = (1 - z^{-1})/T_s z^{-1}$ and the backward Euler method $s = (1 - z^{-1})/T_s$ are used for the forward and feedback integrator [40]. Therefore, the control scheme of the multi-resonant controllers at the harmonic orders 6th and 12th can be rewritten in the discrete-time domain according to Fig. 6 and the discrete-time domain transfer function of the resonant controller can be expressed as

$$G_{rh}(z) = \frac{K_{rh}T_s\left(z^{-1} - z^{-2}\right)}{1 + \left(T_s^2 h^2 \omega_n^2 - 2\right) z^{-1} + z^{-2}}. \tag{12}$$

The integrator coefficients of each resonant controllers in Fig. 6 can be written as $a_{2h} = K_{rh}T_s$, $a_{3h} = (h\omega_n)^2 T_s/K_{rh}$.

The resonant frequencies at the harmonic orders 6th and 12th are kept tuned with the estimated frequency $\hat{\omega}'$ from PLL for grid frequency adaptation. The fundamental current control has the intrinsic frequency adaptation capability through the Park transformation.

For programming of the multi-resonant controllers, each HC is converted to a simple pseudo-code as described in Fig. 7. This code is executed each sampling time period of the simulation software or DSP.

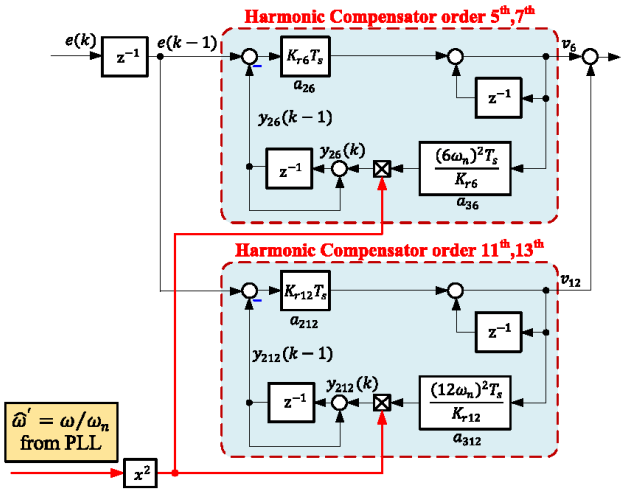


Fig. 6. Discrete-time implementation of harmonic compensation with frequency adaptation.

```
%Resonant Controller for Order 6th
v6(k) = a26*(e(k-1)-y26(k-1)) + v6(k-1);
y26(k) = a36*v6(k)*wn^2 + y26(k-1);
e(k-1) = e(k);
%Resonant Controller for Order 12th
v12(k) = a212*(e(k-1)-y212(k-1)) + v12(k-1);
y212(k) = a312*v12(k)*wn^2 + y212(k-1);
e(k-1) = e(k);
```

Fig. 7. Pseudo-code of the harmonic compensators.

3. Experimental verification

3.1. Experimental setup

The simulation model of the VSC developed in MATLAB/Simulink 2022b is provided in [41], which has been presented in our previous work [33]. Moreover, the proposed control technique was verified through the hardware-in-the-loop (HiL) implementation and the hardware implementation. Figs. 8 and 9 depict the experimental setup. The VSC was modeled in an OPAL-RT OP4510 real-time simulator, where the power circuit of the VSC was implemented on FPGA-based via eHS toolbox in MATLAB/Simulink with a time step 220 ns. The control schemes were implemented on a Texas Instruments TMS320F28379D 32-bit DSP. The grid voltage, grid current, and dc bus voltage were scaled down to connect to the DSP, and the gate signals from the DSP were sent back to the HiL system as shown in Fig. 8(a). The simulated signals were measured by an oscilloscope via the analog outputs of the HiL system as shown in Fig. 8(b). Fig. 9(a) depicts the laboratory hardware implementation. The VSC was connected to a Chroma 61850 regenerative grid simulator, which provided the three-phase distorted grid voltage and changing frequency. The DC side of the VSC was set to be a 700 V constant voltage by a Chroma 62150H-1000S DC power supply. A 5 kW *LCL*-filtered 2-level VSC was used in the hardware prototype as shown in Fig. 9(b). A Yokogawa WT-3000E power analyzer was used to measure the grid current parameters of the prototype VSC. The VSC was controlled by the same DSP used for HiL with the same voltage and current sensor gains.

Note that the 5-kW VSC in this study can be validated with the hardware prototype alone without the need for the HiL real-time simulator. Considering the VSC alone, the validation with a HiL real-time simulator is costly and unnecessary. However, the OP4510 HiL simulator used in this study can emulate the distorted grid voltages with frequency variation, and the DC voltage source. Furthermore, an OP4510 HiL simulator is much cheaper than a grid simulator and programmable DC source. Thus, validation with a HiL simulator is an alternative and cost-effective choice for research on VSC control. This experimental setup is preliminary work for our future study in inverter-based power systems.

3.2. Harmonic mitigation

The VSC with the PIMR and PIMSR control schemes was evaluated under the sinusoidal and distorted grid voltages with a nominal steady-state power of 5 kW. The harmonic components V_5, V_7, V_{11}, and V_{13} were added to the fundamental grid voltage V_1 as shown in Table 2 with a total harmonic distortion (THD_v) of 4.69%. The grid frequency was tested under the allowable range of the Thailand grid: the nominal

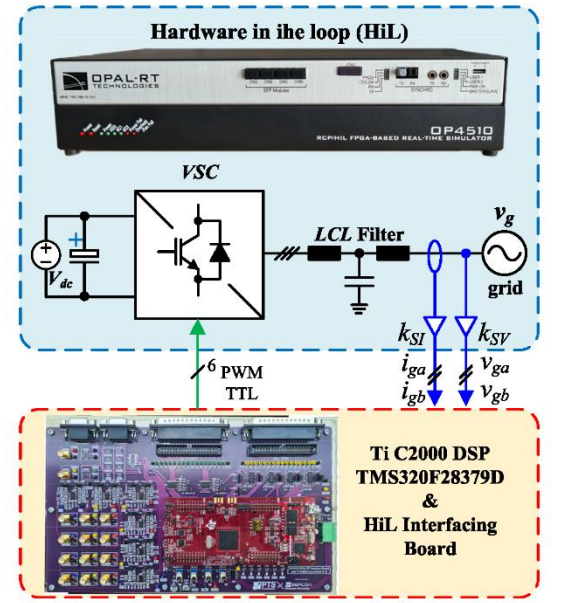


Fig. 8. Experimental setup. (a) HiL configuration scheme. (b) Hardware implementation.

value of 50 Hz, the minimum value of 47 Hz, and the maximum value of 52 Hz. Fig. 10 shows the simulation and experimental results the grid currents with the fundamental component controller under the distorted grid voltages at the nominal frequency. The HiL and hardware experimental results are very similar to the simulation results. The grid voltage harmonics distort the grid current waveforms with a THD_i of 10.84%. Fig. 11 compares the current harmonic components of the fundamental component controller without the HCs (black) with those of the PIMR (red) and PIMSR (blue) control schemes at the nominal grid frequency. The harmonic orders 5th and 7th of the fundamental component controller exceed the IEEE 1547 standard (magenta line) [10]. Moreover, the current harmonic orders 11th and 13th are still noticed. On the other hand, the HCs of the PIMR and PIMSR controllers suppress the current harmonic orders 5th, 7th, 11th, and 13th close to zero, which complies with the IEEE 1547 standard.

Table 3 summarizes the THD_i values of the fundamental component controller, the PIMR controller with/without frequency adaptation, and the PIMSR controller under the sinusoidal and distorted grid voltages at the frequencies of 47 Hz, 50 Hz, and 52 Hz. The PIMR controller without frequency adaptation manages to suppress the voltage harmonics at the nominal grid frequency, compared with the fundamental component controller under the sinusoidal grid voltages. However, the THD_i values deteriorate when the grid frequency deviates from the nominal value. The resonant frequencies of the PIMR controller updated from PLL keep the THD_i values lower 1.15%. Meanwhile,

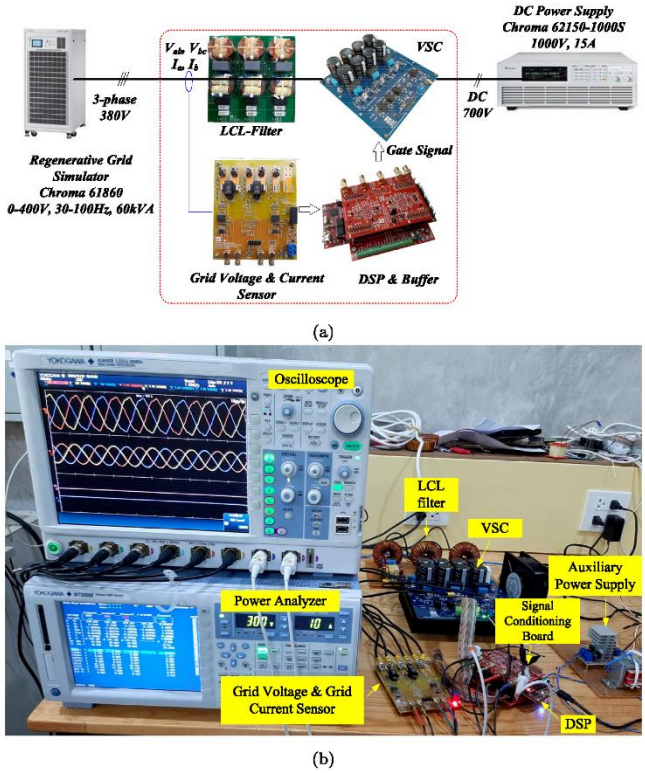


Fig. 9. Experimental setup. (a) 5 kW VSC prototyping configuration scheme. (b) Laboratory-scale environment.

Table 2
Simulated grid voltage harmonics.

V_1	V_5	V_7	V_{11}	V_{13}	THD_v
220 V_{rms}	4%	2%	1%	1%	4.69%

the PIMSR controller has an inherent frequency adaptation capability, which exhibits a similar harmonic attenuation to the PIMR with frequency adaptation.

3.3. Transient performance and power extraction capability

This section validates the transient performance and the power extraction capability of the PIMR and the PIMSR control schemes. Fig. 12 shows the dynamic response of the VSC when the reference current suddenly changes under distorted grid voltage, as shown in Table 2. Initially, both the reference currents were set to zero ($i'_{gd,ref}$ = 0 p.u. and $i'_{gq,ref}$ = 0 p.u.). Then, the reference currents were suddenly changed to $i'_{gd,ref}$ = −0.7 p.u., and $i'_{gq,ref}$ = 0 p.u.. At this time, the VSC feeds an active power of 3.5 kW into the grid. After that, the VSC injects a reactive power of 3.5 kVar (set $i'_{gq,ref}$ = −0.7 p.u.). The experimental results show that the behavior of the grid current waveforms tracks the reference currents. The distorted voltage does not affect the transient response of the grid currents. The grid currents of the PIMR and the PIMSR schemes at the steady-state conditions are close to the sinusoidal waveform. The zoomed areas in Figs. 12(c) and 12(d) indicate that the PIMR controller exhibits a transient response very close to the PIMSR controller because of their identical stationary frame transfer function as shown in (3) The simulation results, the experimental results of HiL, and the hardware implementations are in close agreement. However, there is still a slight difference in the rising edge of the grid current step. The oscillation of the grid current during the transient of the simulation result is slightly higher than that of the HiL and hardware experimental results. This is believed to be due to voltage drops in the IGBTs and the grid simulator's internal impedance, which were neglected in the simulation. The instantaneous active and reactive power can be calculated from the dq-axes currents directly.

3.4. Performance under grid frequency and voltage variation

This section validates the frequency adaptation capability of the PIMR and PIMSR controllers under the sinusoidal and distorted grid voltages. Fig. 13 shows the grid current waveforms of the PIMR control scheme under the sinusoidal voltages when the grid frequency changes from 47 Hz to 50 Hz, and from 50 Hz to 52 Hz. The grid current THDi values with the PIMR controller are 0.88%, 0.90%, and 0.81%

Table 3
Total harmonic distortion of the grid current at the nominal output power of 5 kW.

Control schemes	Sinusoidal grid voltages			Distorted grid voltages		
	47 Hz	50 Hz	52 Hz	47 Hz	50 Hz	52 Hz
Fundamental component controller	1.21%	1.40%	1.14%	10.97%	10.54%	10.77%
PIMR without frequency adaptation	1.05%	0.97%	1.11%	7.85%	1.08%	8.92%
PIMR	0.88%	0.91%	0.81%	0.96%	1.15%	0.90%
PIMSR	0.93%	0.95%	0.82%	0.93%	1.09%	0.83%

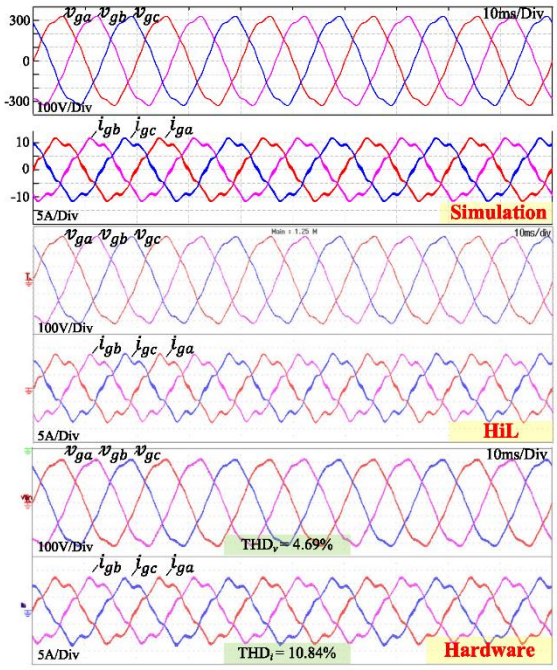


Fig. 10. Simulation and experimental results of the VSC without the harmonic compensators under the distorted voltages.

because there is no harmonic disturbance from the grid voltages. Fig. 14(a) and Fig. 14(b) indicate the grid current waves of the PIMR and PIMSR control schemes under the distorted grid voltages when the grid frequency changes from 47 Hz to 50 Hz, and from 50 Hz to 52 Hz. The grid current waveforms of the PIMR controller and the PIMSR controller are very close to those under the sinusoidal voltage in Fig. 13 at all the changing frequencies, which has a slight distortion in the edge of the frequencies, as illustrated in Fig. 14(a). The PIMR scheme without the frequency adaptation depicted in Fig. 14(b) cannot mitigate the effects of distorted grid voltage when the frequency deviates from the nominal value. Meanwhile, the PIMSR controller exhibits the inherent frequency adaptation capability through the axis transformations The PIMR controller without the frequency adaptation has the THD_i of 7.85% at 47 Hz and 8.92% at 52 Hz, which exceeds IEEE 1547 standard [10]. On the other hand, the PIMR controller with frequency adaptation and the PIMSR controller maintain low THD_i values at the frequencies of 47 Hz and 52 Hz. The grid current has a THD_i approximately 1% that complies with the IEEE 1547 standard. The experimental results from HiL in Fig. 14(a) are very close to those of the hardware implementation in Fig. 14(b).

Fig. 15 shows the experimental performance of the PIMR and PIMSR control schemes under the ±10% sag/swell of the distorted grid voltages. The two controllers again exhibit close transient responses, which regulate the grid currents back to the reference values within 10 ms.

4. Discussion

Table 4 compares the estimated computational effort of the PIMR and PIMSR controllers for the TMS320F28379D DSP. The PISMR controller requires a substantial computational task for the multiplications and Trigonometric function operations for the harmonic orders, 5th, 7th, 11th, and 13th. Meanwhile, the PIMR controller requires the Trigonometric functions only at the fundamental component, while the resonant controllers at orders, 6th, 12th, use only the additions,

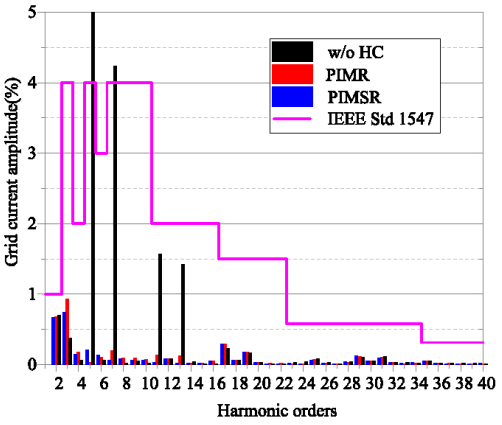


Fig. 11. Grid current harmonic spectrum of the VSC at the nominal power of 5 kW under the distorted grid voltage.

Table 4
Computational effort of the control schemes.

Mathematical operations	Control methodology	
	PIMR	PIMSR
Additions/subtractions	35	49
Multiplications	198	384
Trigonometric functions (Sin/Cosine)	78	468
Saturation limits	14	14
Execution cycles	325	915
Execution time (0.005 μs/cycle)	1.625 μs	4.575 μs

subtractions, and multiplications. The PIMR controller presented in this study poses a one-third computational effort of the PIMSR controller while maintaining the frequency adaptation and power extraction capability. Thus, the PIMSR controller is suggested for the three-phase VSC current control.

Although the reduction in the computation time of 2.950 μs with the PIMR scheme seems insignificant when implemented on a powerful TMS320F28379D DSP with a sampling frequency of 20 kHz, the PIMR control scheme will be more beneficial with higher switching and sampling frequencies for wide bandgap devices. For example, the PIMR regulator will be helpful for the multi-loop grid-forming control of the VSCs in inverter-based electric power systems [42]. Moreover, discretization of the resonant controller is crucial for high switching frequency applications with a significant computation delay [43].

Multiple resonant regulators in series with a fundamental current controller with the deadbeat control have been recently proposed in [44]. Meanwhile, in this study, the multiple resonant regulators are placed in parallel with the fundamental component PI controller. Thus, it would be interesting to compare the harmonic rejection performance and control stability of the parallel and series configuration of the harmonic controller.

5. Conclusion

This paper elaborates the implementation methodology of the proportional–integral plus multi-resonant (PIMR) harmonic compensation scheme with frequency adaptation for a three-phase grid-connected VSC under the voltage distortion. Discretization of the multi-resonant controllers and implementation techniques on a 32-bit TMS320F283 79D DSP controller are explained. The PIMR control scheme was compared the conventional multiple synchronous reference frame (PIMSR)

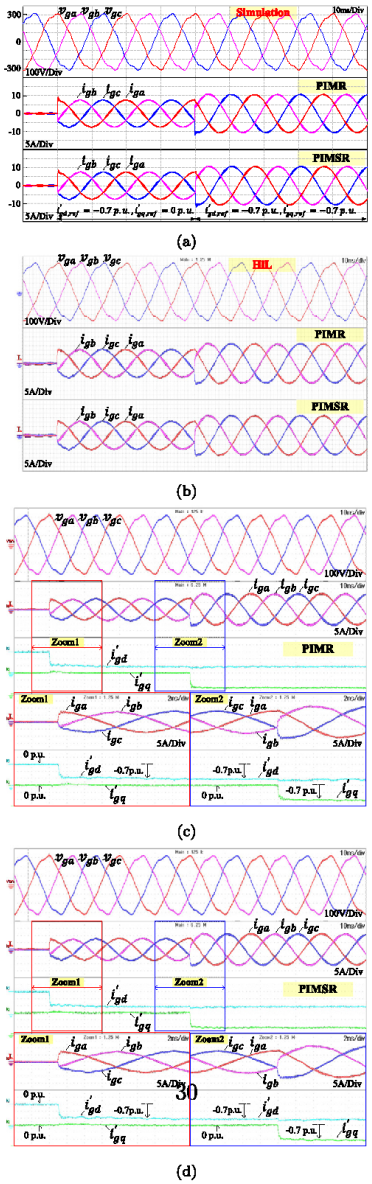


Fig. 12. Transient response of the grid current under the distorted voltage. (a) Simulation. (b) HIL prototype. (c) Hardware prototype with the PIMR controller. (d) Hardware prototype with the PIMSR controller.

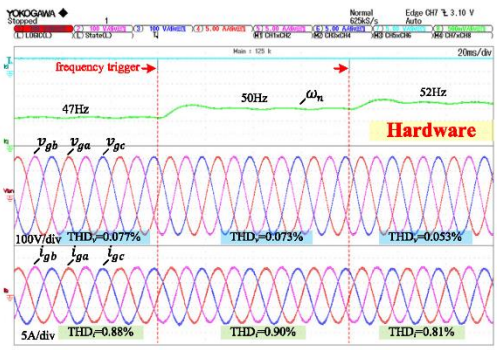


Fig. 13. Performance of the PIMR control scheme under the sinusoidal grid voltages with the changing grid frequency.

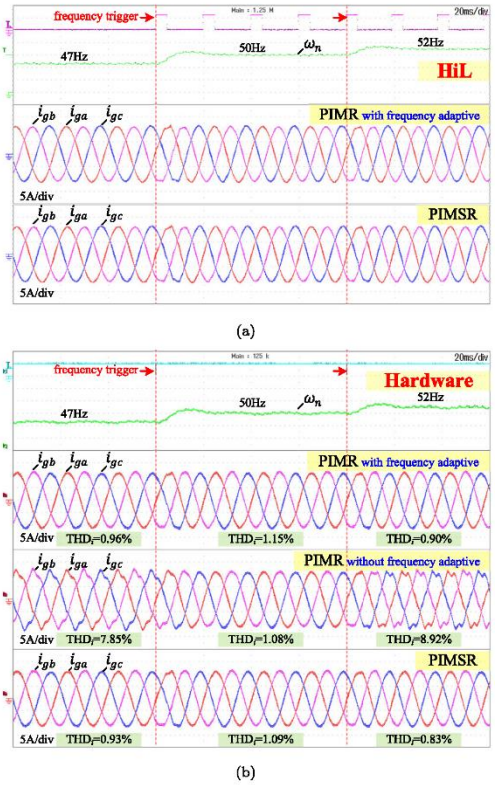


Fig. 14. Performance of the PIMR and PIMSR control schemes under the distorted grid voltages with the changing grid frequency: (a) HiL system, (b) Hardware prototype.

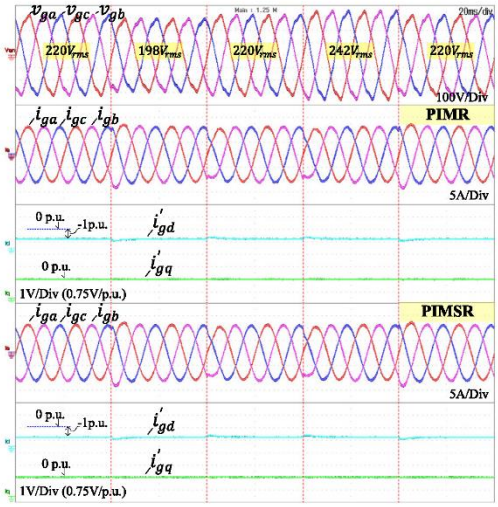


Fig. 15. Performance of the PIMR and PIMSR control scheme under the grid voltage sag and swell from the hardware prototype.

controller. The simulation and experimental results from a HiL simulator and hardware prototype indicate that the two control schemes attenuated the grid current with a total harmonic distortion approximately of 1% under the grid voltage orders 5th, 7th, 11th, and 13th with a total harmonic distortion of 4.69% in the frequency range of 47–52 Hz, which is in compliance with the IEEE 1547 standard. The PIMR controller exhibited identical performance to the conventional PIMSR scheme. Meanwhile, the computation time for the PIMR controller was estimated to be 1.625 μs, 35% of the conventional PIMSR controller.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Suparak Srita reports financial support was provided by Energy Policy and Planning office (EPPO), Ministry of Energy, the Royal Thai Government.

Data availability

Data will be made available on request.

Acknowledgments

Suparak Srita is grateful to the Energy Policy and Planning Office (EPPO) Ministry of Energy, the Royal Thai Government for sponsoring his doctoral study. Also, the authors thank PTS Combination Co., Ltd. for supporting an OPAL-RT in this project. A preliminary version of this work has been published in ETCI-CON 2022 [35].

References

[1] Zhang G, Jin N, Yu SS, Zhang Y. An X-shaped-switching-network high-step-up converter for grid integration of renewable energy sources. AEU - Int J Electron Commun 2021;136:153776. http://dx.doi.org/10.1016/j.aeue.2021.153776.

[2] Bulut EB, Gulbahce MO, Kocabas DA. Analysis of a GaN based PWM AC-AC converter with an improved switch loss model. AEU - Int J Electron Commun 2021;131:153578. http://dx.doi.org/10.1016/j.aeue.2020.153578.

[3] Sen D, Saha TK, Dey J. Development, implementation and performance analysis of decoupler based control of dual source DC-DC converter. AEU - Int J Electron Commun 2020;117:153136. http://dx.doi.org/10.1016/j.aeue.2020.153136.
[4] Pahlavandust M, Yazdani MR. Single-switch boost DC-DC converter with zero-current-switching, high power density and low electromagnetic interference. AEU - Int J Electron Commun 2020;121:153229. http://dx.doi.org/10.1016/j.aeue.2020.153229.
[5] zhi Zhou S, zhen Gong Y, Li X, Hu S, Chen H. Operation of a semi dual-bridge resonant converter with a tunable resonant tank. AEU - Int J Electron Commun 2022;152:154261. http://dx.doi.org/10.1016/j.aeue.2022.154261.
[6] Gayen P. An enhanced high-boost active-switched quasi Z-source inverter having shorter range of shoot-through duty ratio for solar energy conversion applications. AEU - Int J Electron Commun 2021;137:153822. http://dx.doi.org/10.1016/j.aeue.2021.153822.
[7] Rivera S, Kouro S, Vazquez S, Goetz SM, Lizana R, Romero-Cadaval E. Electric vehicle charging infrastructure: From grid to battery. IEEE Ind Electron Mag 2021;15(2):37–51. http://dx.doi.org/10.1109/MIE.2020.3039039.
[8] Li YW, He J. Distribution system harmonic compensation methods: An overview of DG-interfacing inverters. IEEE Ind Electron Mag 2014;8(4):18–31. http://dx.doi.org/10.1109/MIE.2013.2295421.
[9] Dionise TJ, Lorch V. Voltage distortion on an electrical distribution system. IEEE Ind Appl Mag 2010;16(2):48–55. http://dx.doi.org/10.1109/MIAS.2009.935498.
[10] IEEE standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces. IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003), 2018, p. 1–138. http://dx.doi.org/10.1109/IEEESTD.2018.8332112.
[11] Yang Y, Zhou K, Blaabjerg F. Enhancing the frequency adaptability of periodic current controllers with a fixed sampling rate for grid-connected power converters. IEEE Trans Power Electron 2016;31(10):7273–85. http://dx.doi.org/10.1109/TPEL.2015.2507545.
[12] Somkun S. High performance current control of single-phase grid-connected converter with harmonic mitigation, power extraction and frequency adaptation capabilities. IET Power Electron 2021;14(2):352–72. http://dx.doi.org/10.1049/pel2.12038.
[13] Hu J, Nian H, Xu H, He Y. Dynamic modeling and improved control of DFIG under distorted grid voltage conditions. IEEE Trans Energy Convers 2011;26(1):163–75. http://dx.doi.org/10.1109/TEC.2010.2071875.
[14] Lascu C, Asiminoaei L, Boldea I, Blaabjerg F. High performance current controller for selective harmonic compensation in active power filters. IEEE Trans Power Electron 2007;22(5):1826–35. http://dx.doi.org/10.1109/TPEL.2007.904060.
[15] Lascu C, Asiminoaei L, Boldea I, Blaabjerg F. Frequency response analysis of current controllers for selective harmonic compensation in active power filters. IEEE Trans Ind Electron 2009;56(2):337–47. http://dx.doi.org/10.1109/TIE.2008.2006953.
[16] Blaabjerg F, Teodorescu R, Liserre M, Timbus AV. Overview of control and grid synchronization for distributed power generation systems. IEEE Trans Ind Electron 2006;53(5):1398–409. http://dx.doi.org/10.1109/TIE.2006.881997.
[17] Campos-Gaona D, Peña-Alzola R, Monroy-Morales JL, Ordonez M, Anaya-Lara O, Leithead WE. Fast selective harmonic mitigation in multifunctional inverters using internal model controllers and synchronous reference frames. IEEE Trans Ind Electron 2017;64(8):6338–49. http://dx.doi.org/10.1109/TIE.2017.2682003.
[18] Newman MJ, Zmood DN, Holmes DG. Stationary frame harmonic reference generation for active filter systems. IEEE Trans Ind Appl 2002;38(6):1591–9. http://dx.doi.org/10.1109/TIA.2002.804739.
[19] Asiminoael L, Blaabjerg F, Hansen S. Detection is key - harmonic detection methods for active power filter applications. IEEE Ind Appl Mag 2007;13(4):22–33. http://dx.doi.org/10.1109/MIA.2007.4283506.
[20] Bao L, Xia J, Dong Z, Deng Y, Lu Y, Yang Y. An improved three-phase four-wire harmonic detection algorithm based on multi-synchronous rotating frame transformation. In: IECON 2019 - 45th annual conference of the IEEE industrial electronics society. Vol. 1, 2019, p. 2115–20. http://dx.doi.org/10.1109/IECON.2019.8927561.
[21] Bhattacharya S, Frank TM, Divan DM, Banerjee B. Active filter system implementation. IEEE Ind Appl Mag 1998;4(5):47–63. http://dx.doi.org/10.1109/2943.715508.
[22] Mattavelli P. A closed-loop selective harmonic compensation for active filters. IEEE Trans Ind Appl 2001;37(1):81–9. http://dx.doi.org/10.1109/28.903130.
[23] Uz-Logoglu E, Salor O, Ermis M. Online characterization of interharmonics and harmonics of AC electric arc furnaces by multiple synchronous reference frame analysis. IEEE Trans Ind Appl 2016;52(3):2673–83. http://dx.doi.org/10.1109/TIA.2016.2524455.
[24] Moral CG, Guerrero JM, Fernández D, Reigosa D, Pereda CR, Briz F. Realizable reference antiwindup implementation for parallel controller structures. IEEE J Emerg Selected Top Power Electron 2021;9(4):5055–68. http://dx.doi.org/10.1109/JESTPE.2020.3021035.
[25] Guerrero-Rodríguez NF, Rey-Boué AB, Reyes-Archundia E. Overview and comparative study of two control strategies used in 3-phase grid-connected inverters for renewable systems. Renew Energy Focus 2017;19–20:75–89. http://dx.doi.org/10.1016/j.ref.2017.05.007.
[26] Khan RA, Ashraf MN, Choi W. A harmonic compensation method using a lock-in amplifier under non-sinusoidal grid conditions for single phase grid connected inverters. Energies 2021;14(3):597.
[27] Liserre M, Teodorescu R, Blaabjerg F. Multiple harmonics control for three-phase grid converter systems with the use of PI-RES current controller in a rotating frame. IEEE Trans Power Electron 2006;21(3):836–41. http://dx.doi.org/10.1109/TPEL.2006.875566.
[28] Kisacikoglu MC, Kesler M, Tolbert LM. Single-phase on-board bidirectional PEV charger for V2G reactive power operation. IEEE Trans Smart Grid 2015;6(2):767–75. http://dx.doi.org/10.1109/TSG.2014.2360685.
[29] Xia J, Guo Y, Zhang X, Jatskevich J, Amiri N. Robust control strategy design for single-phase grid-connected converters under system perturbations. IEEE Trans Ind Electron 2019;66(11):8892–901. http://dx.doi.org/10.1109/TIE.2019.2902791.
[30] Zhou S, Zhang Y, Liu Z, Liu J, Zhou L. Implementation of cross-coupling terms in proportional-resonant current control schemes for improving current tracking performance. IEEE Trans Power Electron 2021;36(11):13248–60. http://dx.doi.org/10.1109/TPEL.2021.3080131.
[31] Liserre M, Teodorescu R, Blaabjerg F. Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values. IEEE Trans Power Electron 2006;21(1):263–72. http://dx.doi.org/10.1109/TPEL.2005.861185.
[32] Teodorescu R, Blaabjerg F, Liserre M, Loh PC. Proportional-resonant controllers and filters for grid-connected voltage-source converters. IEE Proc: Electr Power Appl 2006;153(5):750–62.
[33] Srita S, Somkun S, Kaewchum T, Rakwichian W, Zacharias P, Kamnarn U, et al. Modeling, simulation and development of grid-connected voltage source converter with selective harmonic mitigation: HiL and experimental validations. Energies 2022;15(7). http://dx.doi.org/10.3390/en15072535.
[34] Rodriguez P, Bueno E, Aredes M, Rolim L, Neves F, Cavalcanti M. Discrete-time implementation of second order generalized integrators for grid converters. In: 2008 34th annual conference of IEEE industrial electronics. 2008, p. 176–81. http://dx.doi.org/10.1109/IECON.2008.4757948.
[35] Srita S, Somkun S. Implementation of harmonic compensation for three-phase grid-connected voltage-source converter under grid voltage distortion. In: 2022 19th international conference on electrical engineering/electronics, computer, telecommunications and information technology (ECTI-CON). 2022, p. 1–5. http://dx.doi.org/10.1109/ECTI-CON54298.2022.9795533.
[36] Zhou K, Yang Y, Blaabjerg F, Wang D. Optimal selective harmonic control for power harmonics mitigation. IEEE Trans Ind Electron 2015;62(2):1220–30. http://dx.doi.org/10.1109/TIE.2014.2336629.
[37] Yang Y, Zhou K, Wang H, Blaabjerg F. Analysis and mitigation of dead-time harmonics in the single-phase full-bridge PWM converter with repetitive controllers. IEEE Trans Ind Appl 2018;54(5):5343–54. http://dx.doi.org/10.1109/TIA.2018.2825941.
[38] Holmes DG, Lipo TA, McGrath BP, Kong WY. Optimized design of stationary frame three phase AC current regulators. IEEE Trans Power Electron 2009;24(11):2417–26. http://dx.doi.org/10.1109/TPEL.2009.2029548.
[39] Dannehl J, Wessels C, Fuchs FW. Limitations of voltage-oriented PI current control of grid-connected PWM rectifiers with *LCL* filters. IEEE Trans Ind Electron 2009;56(2):380–8. http://dx.doi.org/10.1109/TIE.2008.2008774.
[40] Yepes AG, Freijedo FD, Doval-Gandoy J, López, Malvar J, Fernandez-Comesaña P. Effects of discretization methods on the performance of resonant controllers. IEEE Trans Power Electron 2010;25(7):1692–712. http://dx.doi.org/10.1109/TPEL.2010.2041256.
[41] Srita S, Somkun S. 3-phase LCL-filtered grid-connected VSC modeling. Mendeley Data 2022. http://dx.doi.org/10.17632/xbpchksg3k.2.
[42] Quan X. Improved dynamic response design for proportional resonant control applied to three-phase grid-forming inverter. IEEE Trans Ind Electron 2021;68(10):9919–30. http://dx.doi.org/10.1109/TIE.2020.3021654.
[43] Husev O, Roncero-Clemente C, Makovenko E, Pimentel SP, Vinnikov D, Martins J. Optimization and implementation of the proportional-resonant controller for grid-connected inverter with significant computation delay. IEEE Trans Ind Electron 2020;67(2):1201–11. http://dx.doi.org/10.1109/TIE.2019.2898616.
[44] Tang C, Zhou K, Shu Y, He Q, Chen Q. Analysis and design of multiple resonant current control for grid-connected converters. IEEE J Emerg Selected Top Power Electron 2022;10(2):2539–46. http://dx.doi.org/10.1109/JESTPE.2021.3138934.

BIOGRAPHY

Name-Surname	SUPARAK SRITA
Date of Birth	26 March 1986
Address	331/45, Village No.3, Hangdong Sup-District, Hangdong District, Chiangmai Province, 50230
Work Experience	2010 - present, Lecturer with Department of Electrical Engineering, Faculty of Engineering, Rajamangala University of Technology Lanna (RMUTL), Chiang Mai, Thailand.
Current Position	Lecturer with Department of Electrical Engineering, Faculty of Engineering, Rajamangala University of Technology Lanna (RMUTL), Chiang Mai, Thailand.
Education Background	2009 - Bachelor of Engineering (Electrical Engineering) (Second Class Honors), Rajamangala University of Technology Lanna (RMUTL), Chiang Mai, Thailand. 2016 - Master of Engineering (Electrical Engineering), Chiang Mai University, Chiang Mai, Thailand.