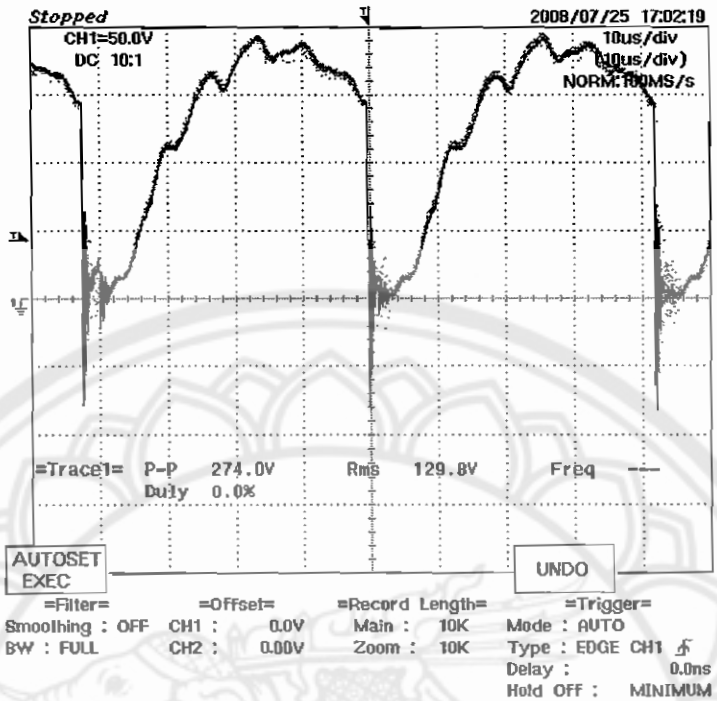
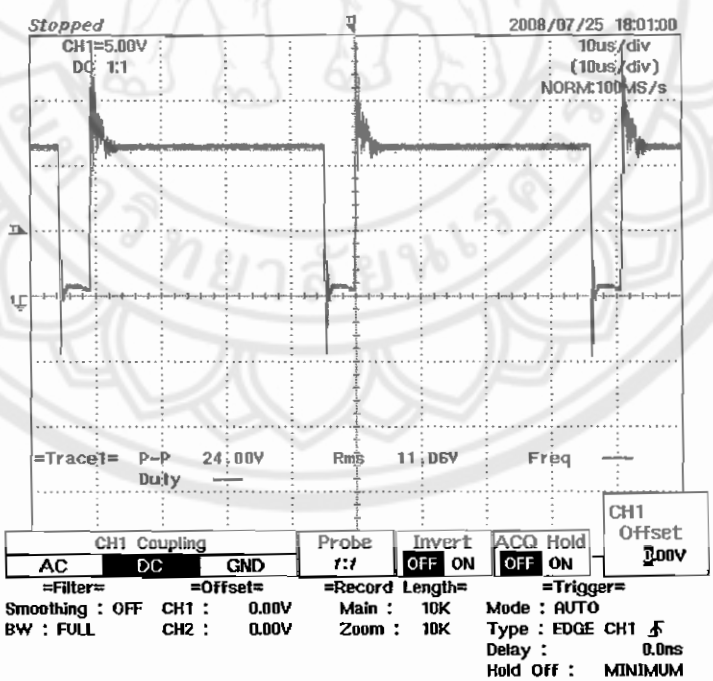
ภาคผนวก

ภาคผนวก ก
รูปสัญญาณแรงดัน

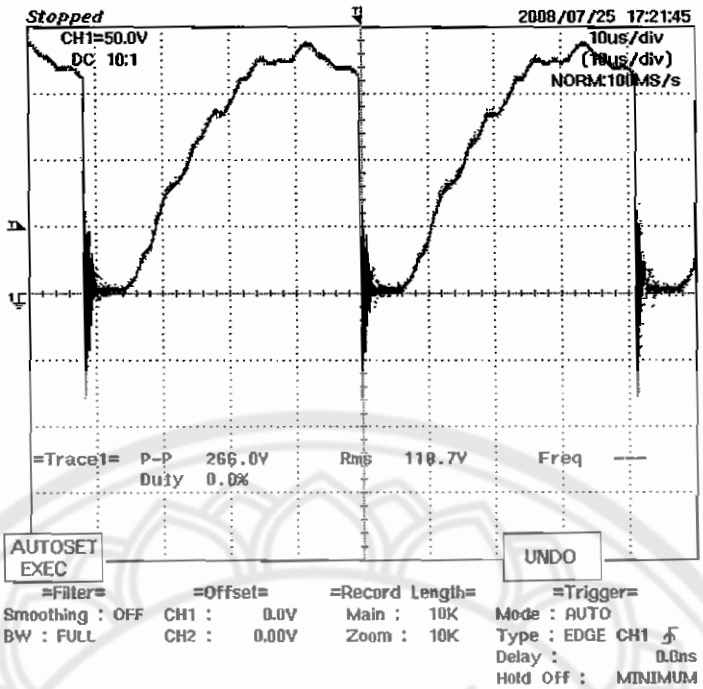
ก.1 รูปสัญญาณแรงดันของสัญญาณรูปคลื่นสี่เหลี่ยม



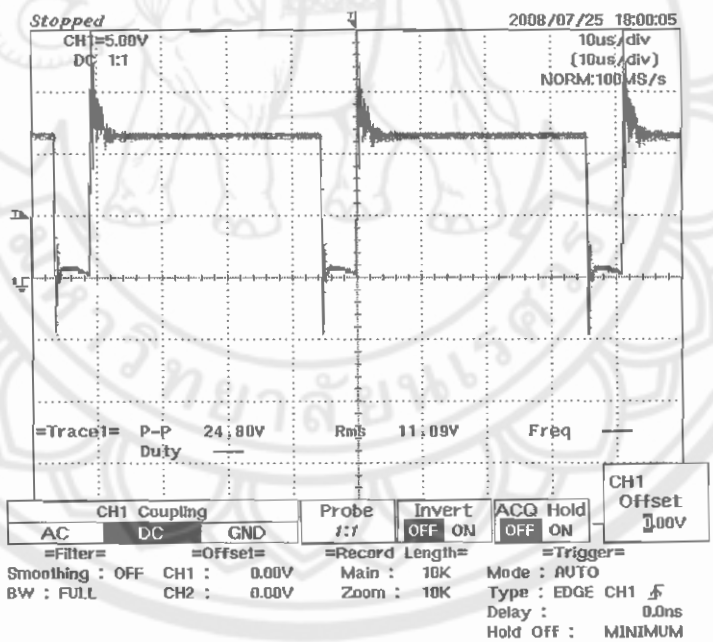
รูปที่ ก-1 รูปแรงดันขาออกที่ดิวตี้ไซเคิล 90%



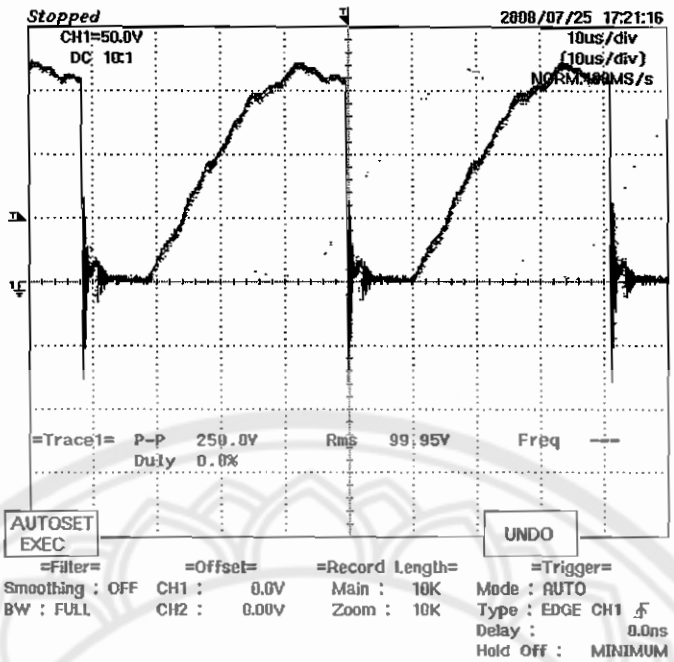
รูปที่ ก-2 รูปแรงดันที่ขาเกตซอสที่ดิวตี้ไซเคิล 90%



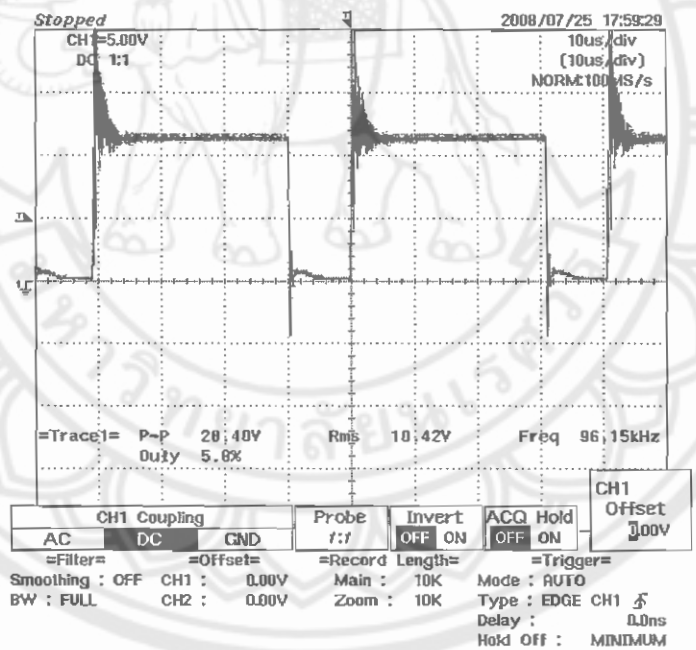
รูปที่ ก-3 รูปแรงดันขาออกที่ดิวตี้ไซเคิล 80%



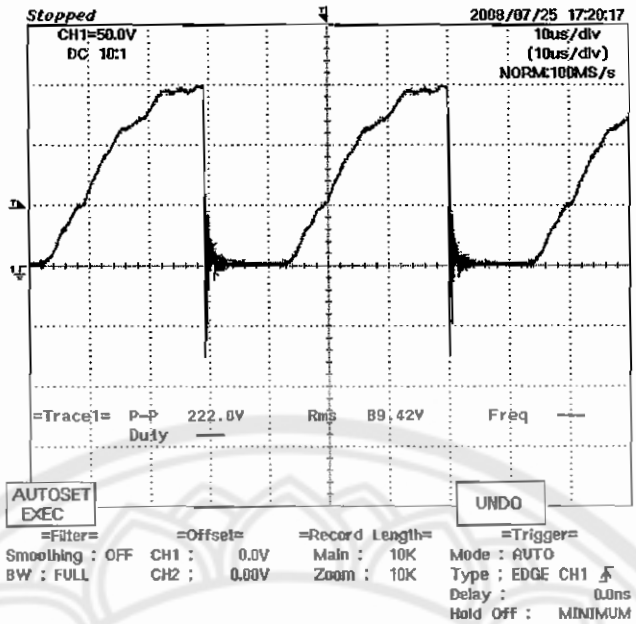
รูปที่ ก-4 รูปแรงดันที่ขาเกตซอสที่ดิวตี้ไซเคิล 80%



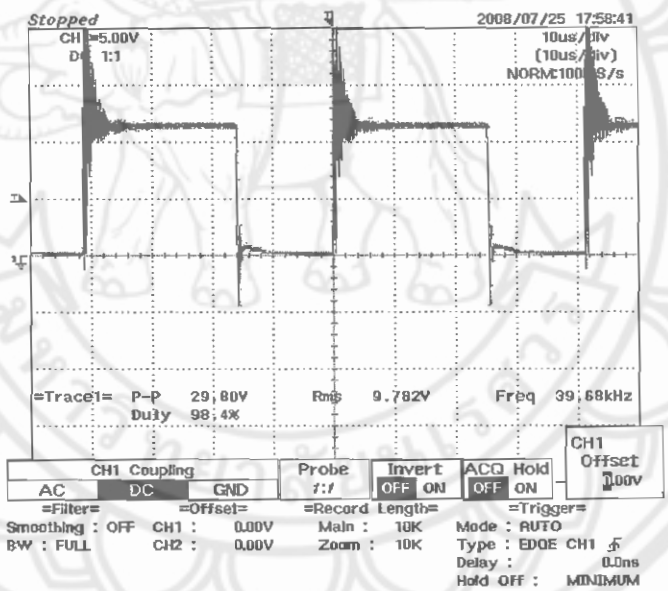
รูปที่ ก-5 รูปแรงดันขาออกที่ดิวตี้ไซเคิล 70%



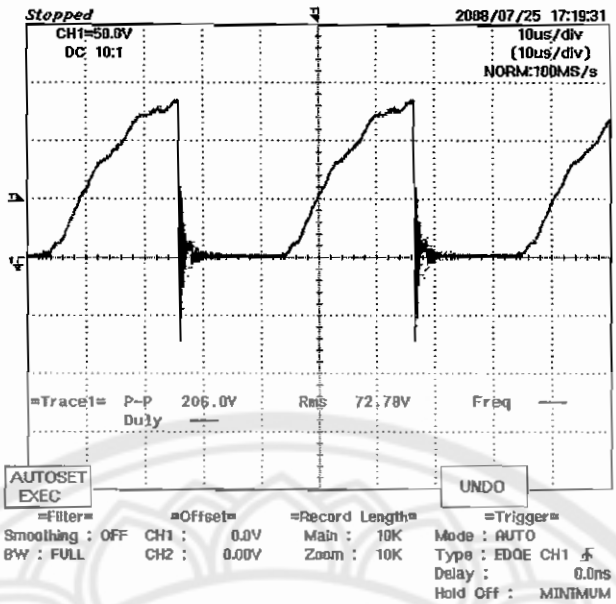
รูปที่ ก-6 รูปแรงดันที่ขาเกตซอสที่ดิวตี้ไซเคิล 70%



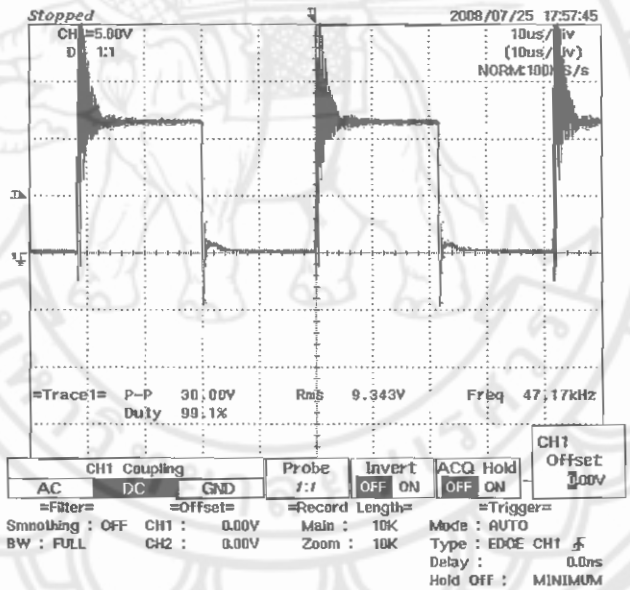
รูปที่ ก-7 รูปแรงดันขาออกที่ดิวตี้ไซเคิล 60%



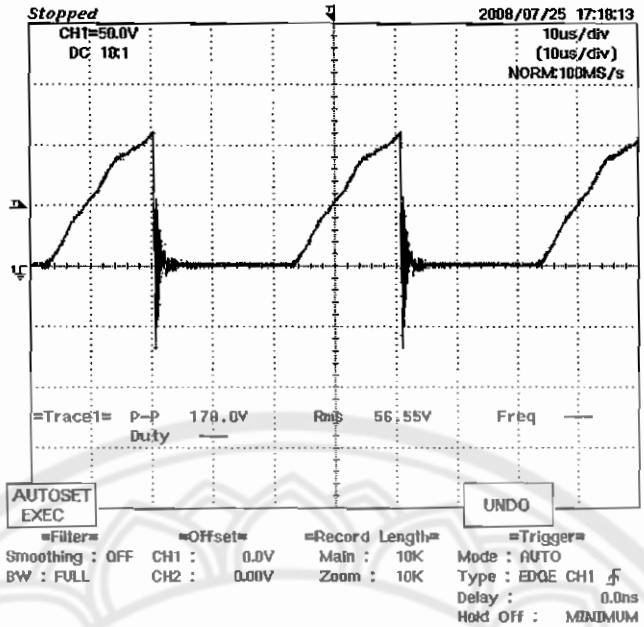
รูปที่ ก-8 รูปแรงดันที่ขาเกตซอสที่ดิวตี้ไซเคิล 60%



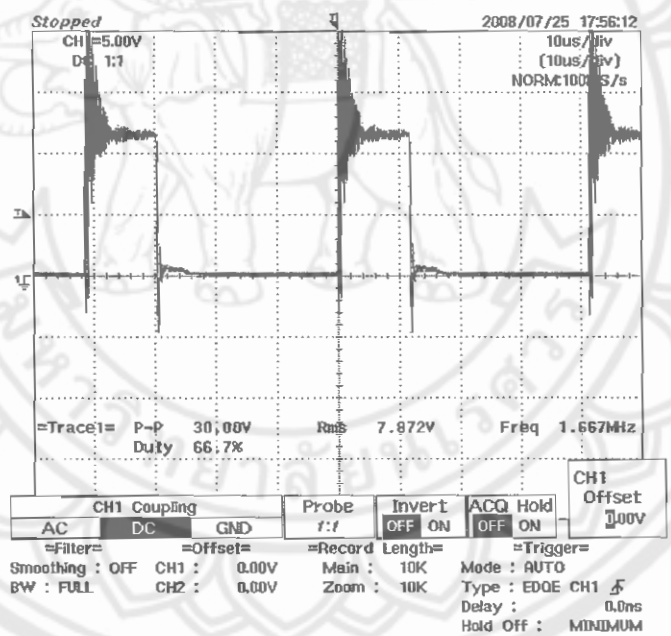
รูปที่ ก-9 รูปแรงดันขาออกที่ดิวตี้ไซเคิล 50%



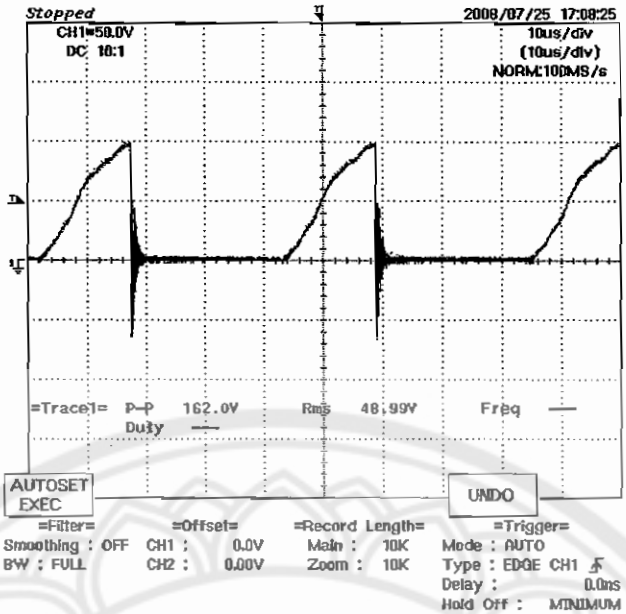
รูปที่ ก-10 รูปแรงดันที่ขาเกตซอสที่ดิวตี้ไซเคิล 50%



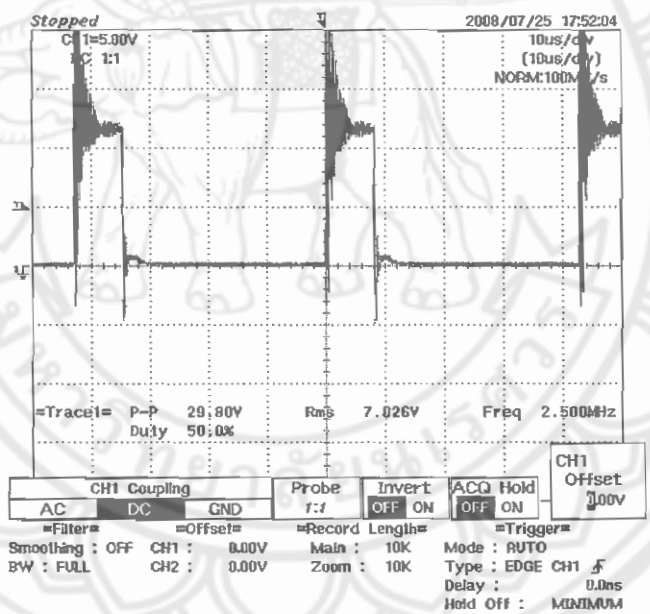
รูปที่ ก-11 รูปแรงดันขาออกที่ดิวตี้ไซเคิล 40%



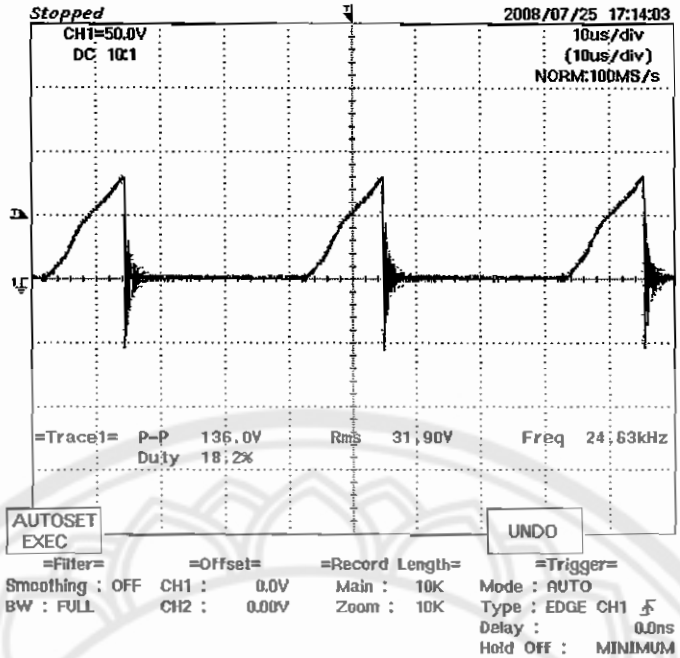
รูปที่ ก-12 รูปแรงดันที่ขาเกตซอสที่ดิวตี้ไซเคิล 40%



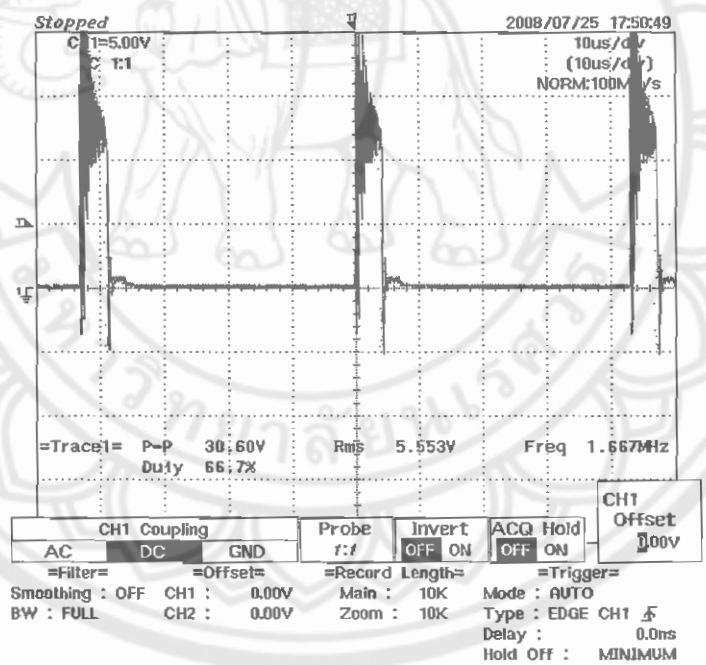
รูปที่ ก-13 รูปแรงดันขาออกที่ดิวตี้ไซเคิล 30%



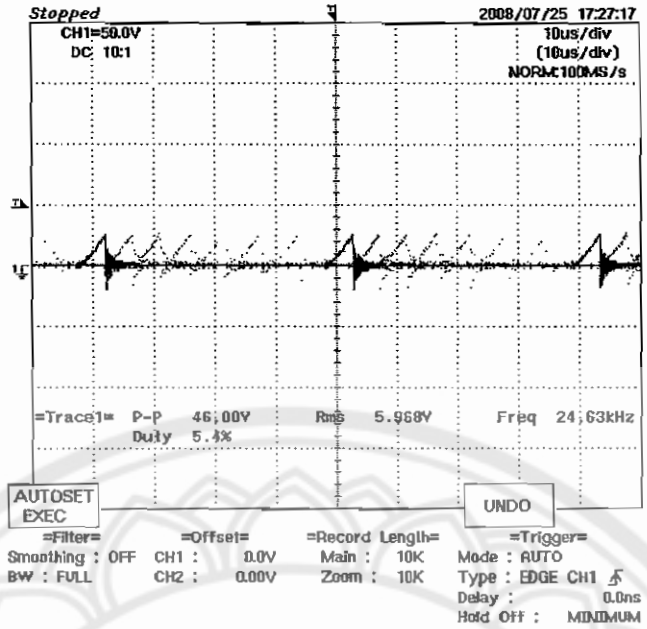
รูปที่ ก-14 รูปแรงดันที่ขาเกตซอสที่ดิวตี้ไซเคิล 30%



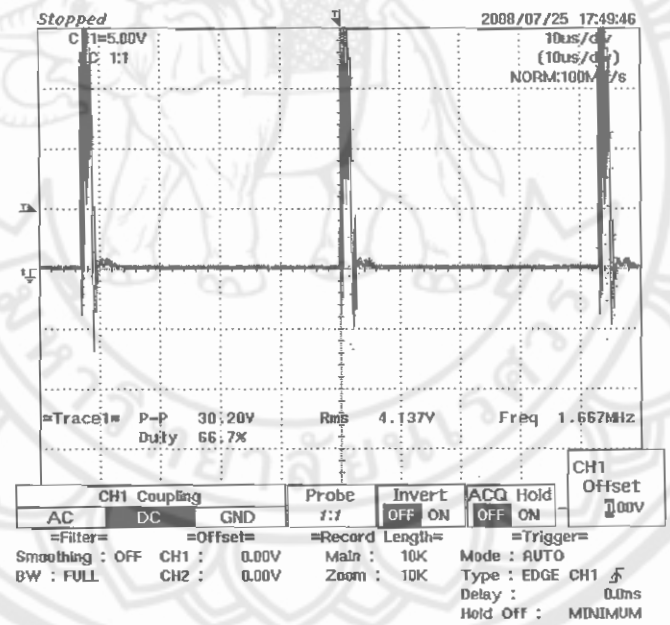
รูปที่ ก-15 รูปแรงดันขาออกที่ดิวตี้ไซเคิล 20%



รูปที่ ก-16 รูปแรงดันที่ขาเกตซอสที่ดิวตี้ไซเคิล 20%

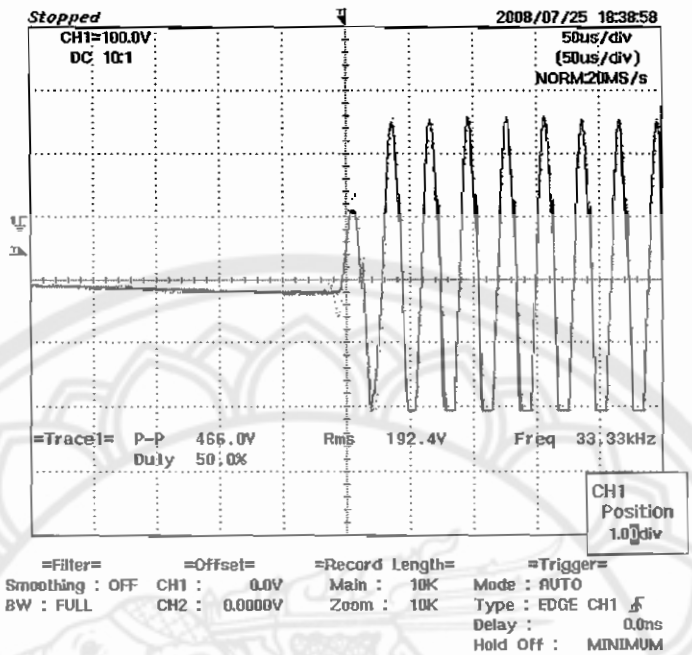


รูปที่ ก-17 รูปแรงดันขาออกที่ดิวตี้ไซเคิล 10%



รูปที่ ก-18 รูปแรงดันที่ขาเกตซอสที่ดิวตี้ไซเคิล 10%

ก.2 รูปสัญญาณแรงดันของสัญญาณรูปคลื่นซายน์

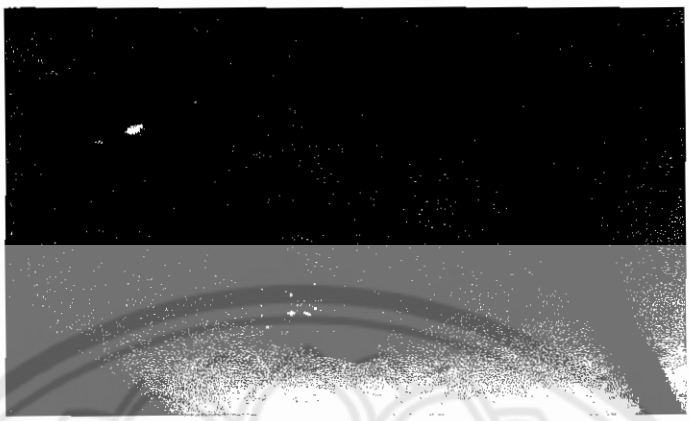


รูปที่ ก-19 รูปแรงดันขาออก

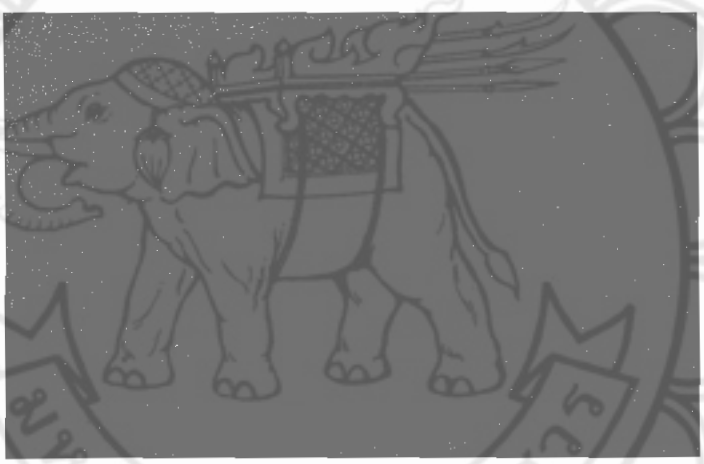
ภาคผนวก ข

รูปแสดงผลการทำความสะอาด

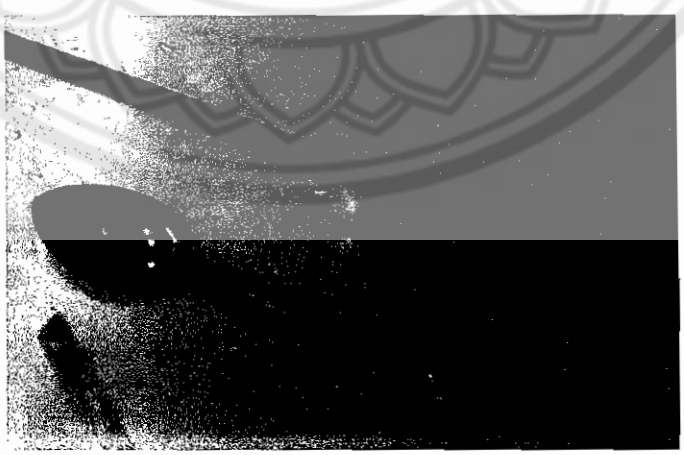
ข.1 ผลการทำความสะอาดกับวัสดุทดสอบ

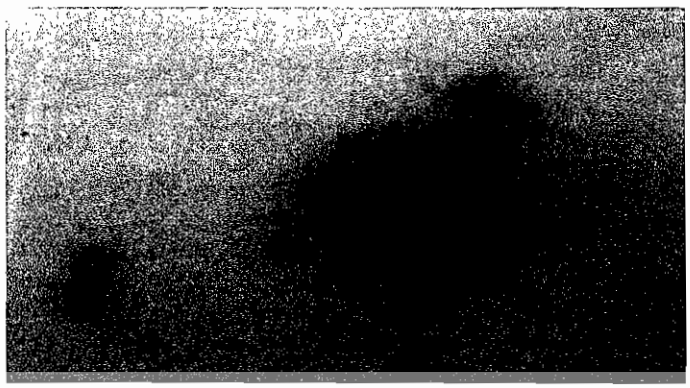


รูปที่ ข-1 แสดงผลการทำความสะอาดคราบไขมันและคราบสนิมนาทีที่ 1

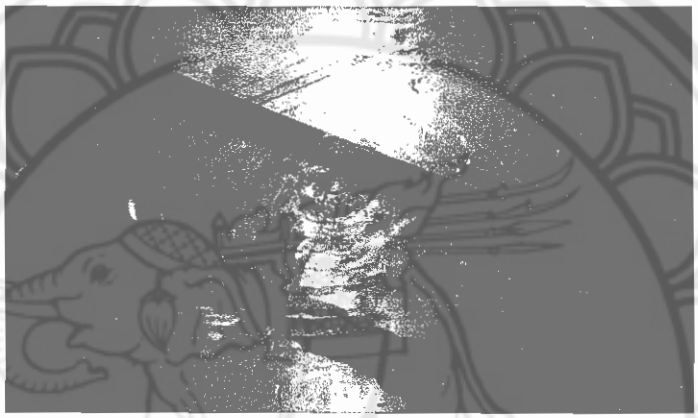


รูปที่ ข-2 แสดงผลการทำความสะอาดคราบน้ำมันเครื่องนาทีที่ 1

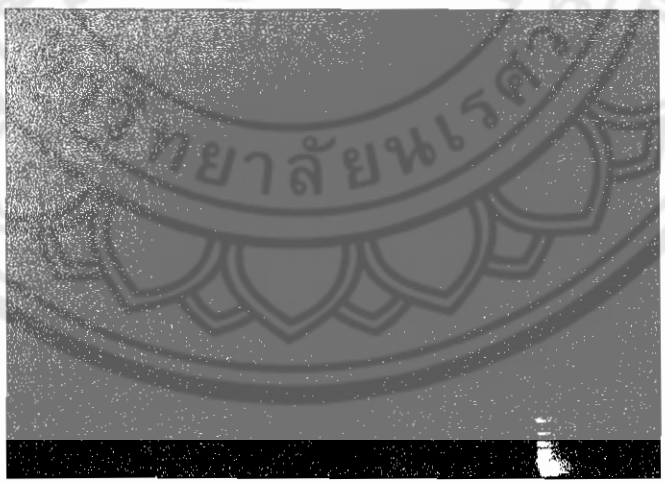




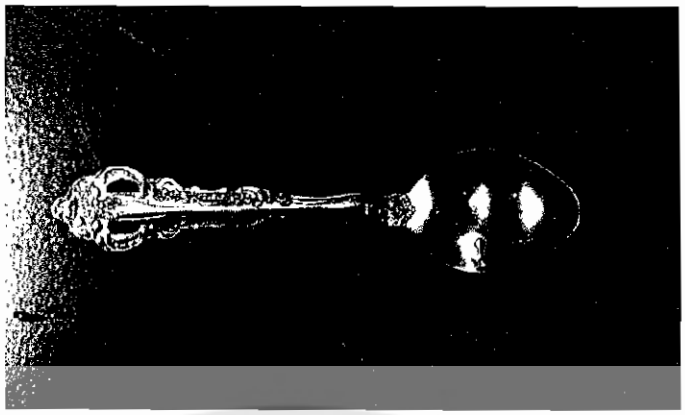
รูปที่ ข-4 แสดงผลการทำความสะอาดคราบน้ำมันเครื่องนาทีที่ 5



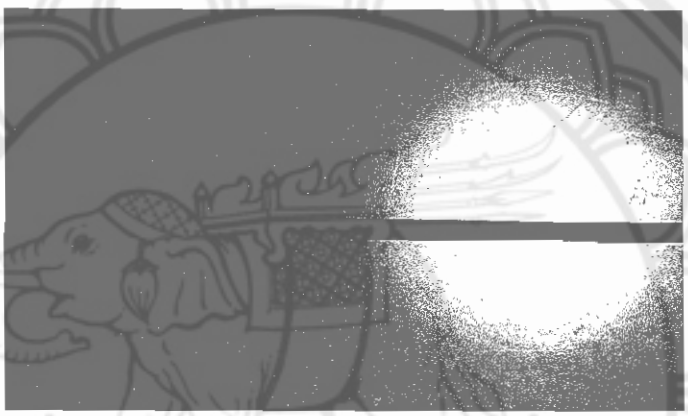
รูปที่ ข-5 แสดงผลการทำความสะอาดคราบไขมันและคราบสนิมนาทีที่ 10



รูปที่ ข-6 แสดงผลการทำความสะอาดคราบน้ำมันเครื่องนาทีที่ 10



รูปที่ ข-7 แสดงผลการทำความสะอาดคราบไขมันนาทีที่ 20

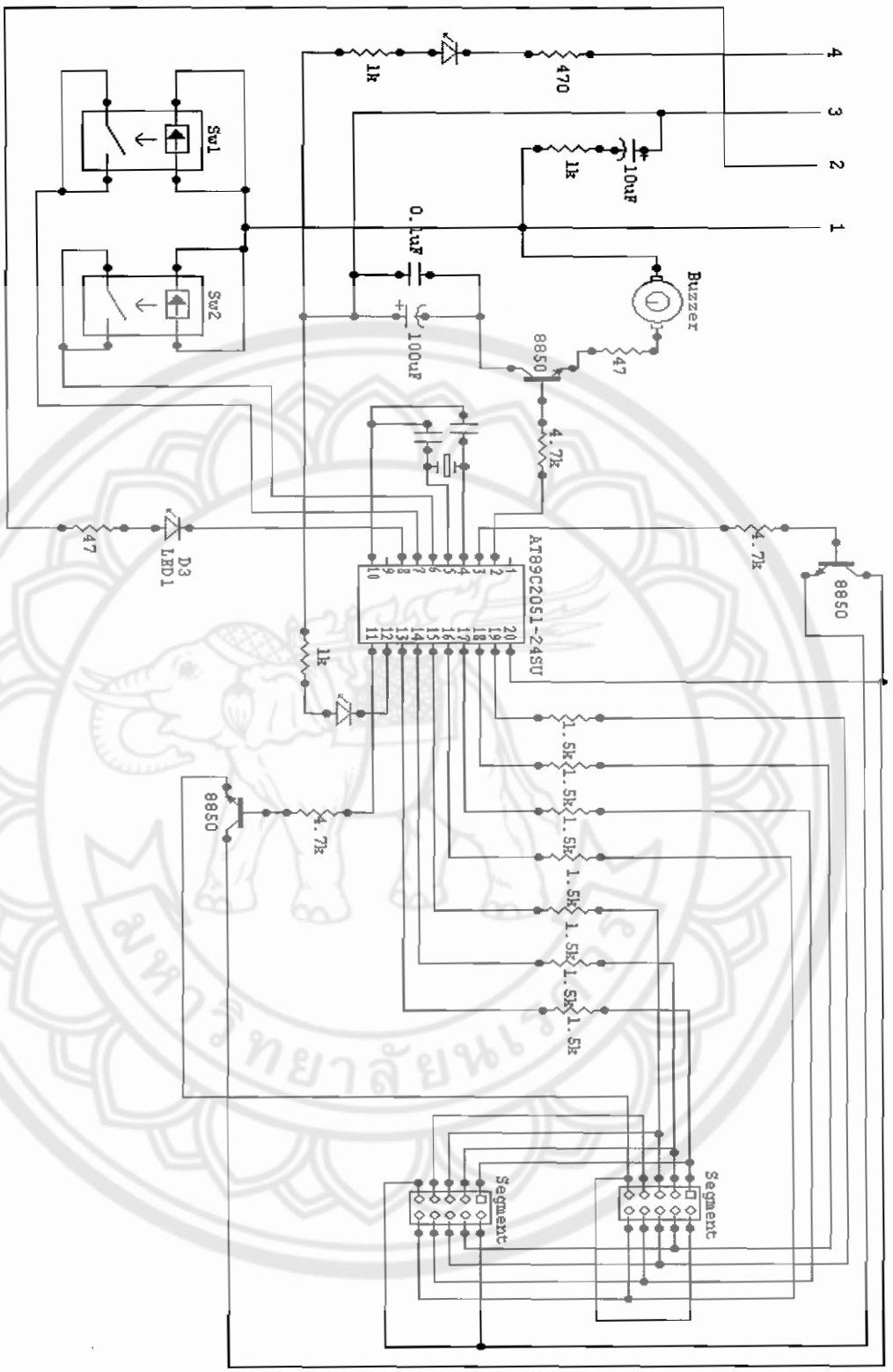


รูปที่ ข-8 แสดงผลการทำความสะอาดคราบสนิมนาทีที่ 20

รูปที่ ข-9 แสดงผลการทำความสะอาดคราบน้ำมันเครื่องนาทีที่ 20

ภาคผนวก ค

วงจรควบคุมการทำงาน



รูปที่ ค-1 วงจรควบคุมการทำงานของวงจร

ภาคผนวก ง

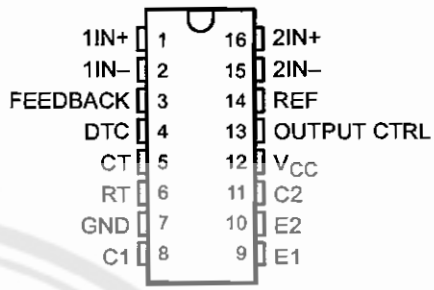
ข้อมูลไอซี TL494

TL494
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS074D – JANUARY 1983 – REVISED MAY 2002

- **Complete PWM Power-Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance**
- **Circuit Architecture Allows Easy Synchronization**

D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



description

The TL494 incorporates all the functions required in the construction of a pulse-width-modulation (PWM) control circuit on a single chip. Designed primarily for power-supply control, this device offers the flexibility to tailor the power-supply control circuitry to a specific application.

The TL494 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from –0.3 V to V_{CC} – 2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can drive the common circuits in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 provides for push-pull or single-ended output operation, which can be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL494C is characterized for operation from 0°C to 70°C. The TL494I is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

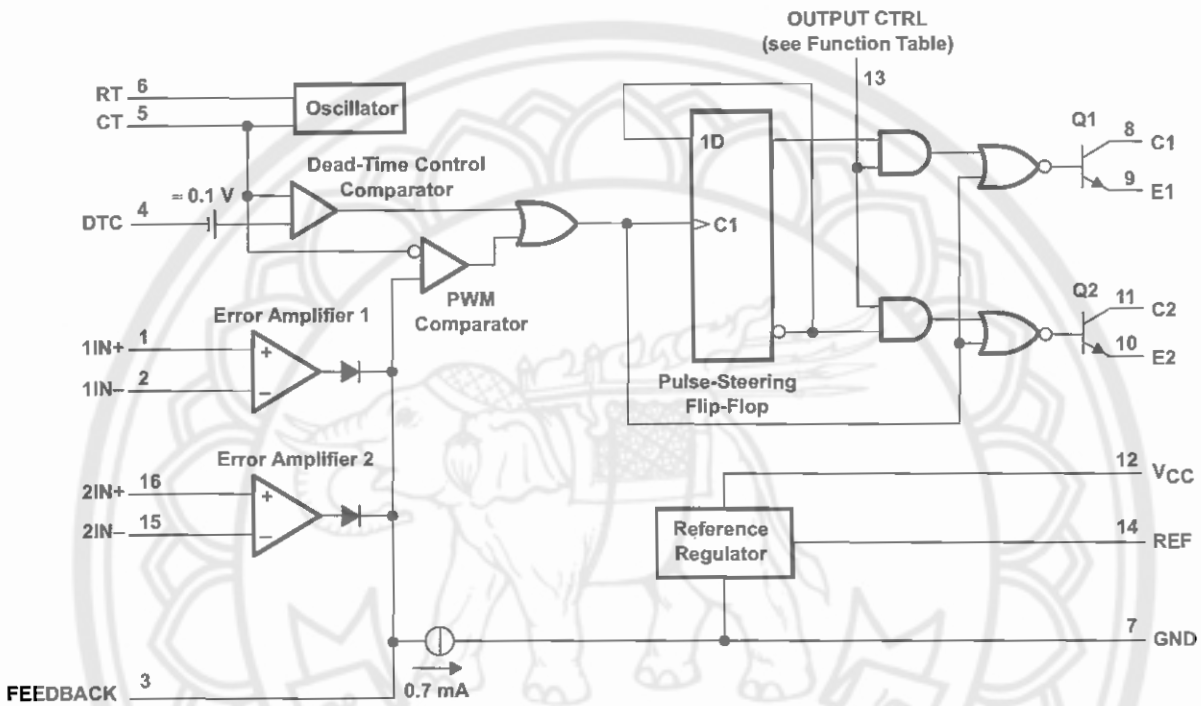
T_A	PACKAGED DEVICES				
	SMALL OUTLINE (D)	PLASTIC DIP (N)	SMALL OUTLINE (NS)	SHRINK SMALL OUTLINE (DB)	THIN SHRINK SMALL OUTLINE (PW)
0°C to 70°C	TL494CD	TL494CN	TL494CNS	TL494CDB	TL494CPW
–40°C to 85°C	TL494ID	TL494IN	—	—	—

The D, DB, NS, and PW packages are available taped and reeled. Add the suffix R to device type (e.g., TL494CDR).

FUNCTION TABLE

INPUT TO OUTPUT CTRL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
V_I = V_{ref}	Normal push-pull operation

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 41 V
Amplifier input voltage, V_I ..... V_{CC} + 0.3 V
Collector output voltage, V_O ..... 41 V
Collector output current, I_O ..... 250 mA
Package thermal impedance, θ_{JA} (see Note 2 and 3): D package ..... 73°C/W
DB package ..... 82°C/W
N package ..... 67°C/W
NS package ..... 64°C/W
PW package ..... 108°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		7	40	V
V_I	Amplifier input voltage		–0.3	V_{CC}–2	V
V_O	Collector output voltage			40	V
	Collector output current (each transistor)			200	mA
	Current into feedback terminal			0.3	mA
f_{osc}	Oscillator frequency		1	300	kHz
C_T	Timing capacitor		0.47	10000	nF
R_T	Timing resistor		1.8	500	kΩ
T_A	Operating free-air temperature	TL494C	0	70	°C
		TL494I	–40	85	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	TL494C, TL494I			UNIT
		MIN	TYP‡	MAX	
Output voltage (REF)	I_O = 1 mA	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V		2	25	mV
Output regulation	I_O = 1 mA to 10 mA		1	15	mV
Output voltage change with temperature	ΔT_A = MIN to MAX		2	10	mV/V
Short-circuit output current§	REF = 0 V		25		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for parameter changes with temperature, are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.

oscillator section, C_T = 0.01 µF, R_T = 12 kΩ (see Figure 1)

PARAMETER	TEST CONDITIONS†	TL494, TL494I			UNIT
		MIN	TYP‡	MAX	
Frequency			10		kHz
Standard deviation of frequency¶	All values of V_{CC}, CT, RT, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1		Hz/kHz
Frequency change with temperature#	ΔT_A = MIN to MAX			10	Hz/kHz

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for parameter changes with temperature, are at T_A = 25°C.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

Temperature coefficient of timing capacitor and timing resistor are not taken into account.

error-amplifier section (see Figure 2)

PARAMETER	TEST CONDITIONS			TL494, TL494I			UNIT
				MIN	TYP‡	MAX	
Input offset voltage	V_O (FEEDBACK) = 2.5 V				2	10	mV
Input offset current	V_O (FEEDBACK) = 2.5 V				25	250	nA
Input bias current	V_O (FEEDBACK) = 2.5 V				0.2	1	µA
Common-mode input voltage range	V_{CC} = 7 V to 40 V			–0.3 to V_{CC}–2			V
Open-loop voltage amplification	ΔV_O = 3 V,	R_L = 2 kΩ,	V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V,		R_L = 2 kΩ		800		kHz
Common-mode rejection ratio	ΔV_O = 40 V,	T_A = 25°C		65	80		dB
Output sink current (FEEDBACK)	V_{ID} = –15 mV to –5 V,		V (FEEDBACK) = 0.7 V	0.3	0.7		mA
Output source current (FEEDBACK)	V_{ID} = 15 mV to 5 V,		V (FEEDBACK) = 3.5 V	–2			mA

‡ All typical values, except for parameter changes with temperature, are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Collector off-state current		V_{CE} = 40 V,	V_{CC} = 40 V		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40 V,	V_E = 0			−100	μA
Collector-emitter saturation voltage	Common emitter	V_E = 0,	I_C = 200 mA		1.1	1.3	V
	Emitter follower	$V_{O(C1 \text{ or } C2)}$ = 15 V,	I_E = −200 mA		1.5	2.5	
Output control input current		V_I = V_{ref}				3.5	mA

† All typical values except for temperature coefficient are at T_A = 25°C.

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input bias current (DEAD-TIME CTRL)	V_I = 0 to 5.25 V		−2	−10	μA
Maximum duty cycle, each output	V_I (DEAD-TIME CTRL) = 0, C_T = 0.01 μF, R_T = 12 kΩ		45%		
Input threshold voltage (DEAD-TIME CTRL)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

† All typical values except for temperature coefficient are at T_A = 25°C.

PWM comparator section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (FEEDBACK)	Zero duty cycle		4	4.5	V
Input sink current (FEEDBACK)	V (FEEDBACK) = 0.7 V	0.3	0.7		mA

† All typical values except for temperature coefficient are at T_A = 25°C.

total device

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Standby supply current	RT = V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		6	10	mA
		V_{CC} = 40 V		9	15	
Average supply current	V_I (DEAD-TIME CTRL) = 2 V,	See Figure 1		7.5		mA

† All typical values except for temperature coefficient are at T_A = 25°C.

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Rise time	Common-emitter configuration,	See Figure 3		100	200	ns
Fall time				25	100	ns
Rise time	Emitter-follower configuration,	See Figure 4		100	200	ns
Fall time				40	100	ns

† All typical values except for temperature coefficient are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

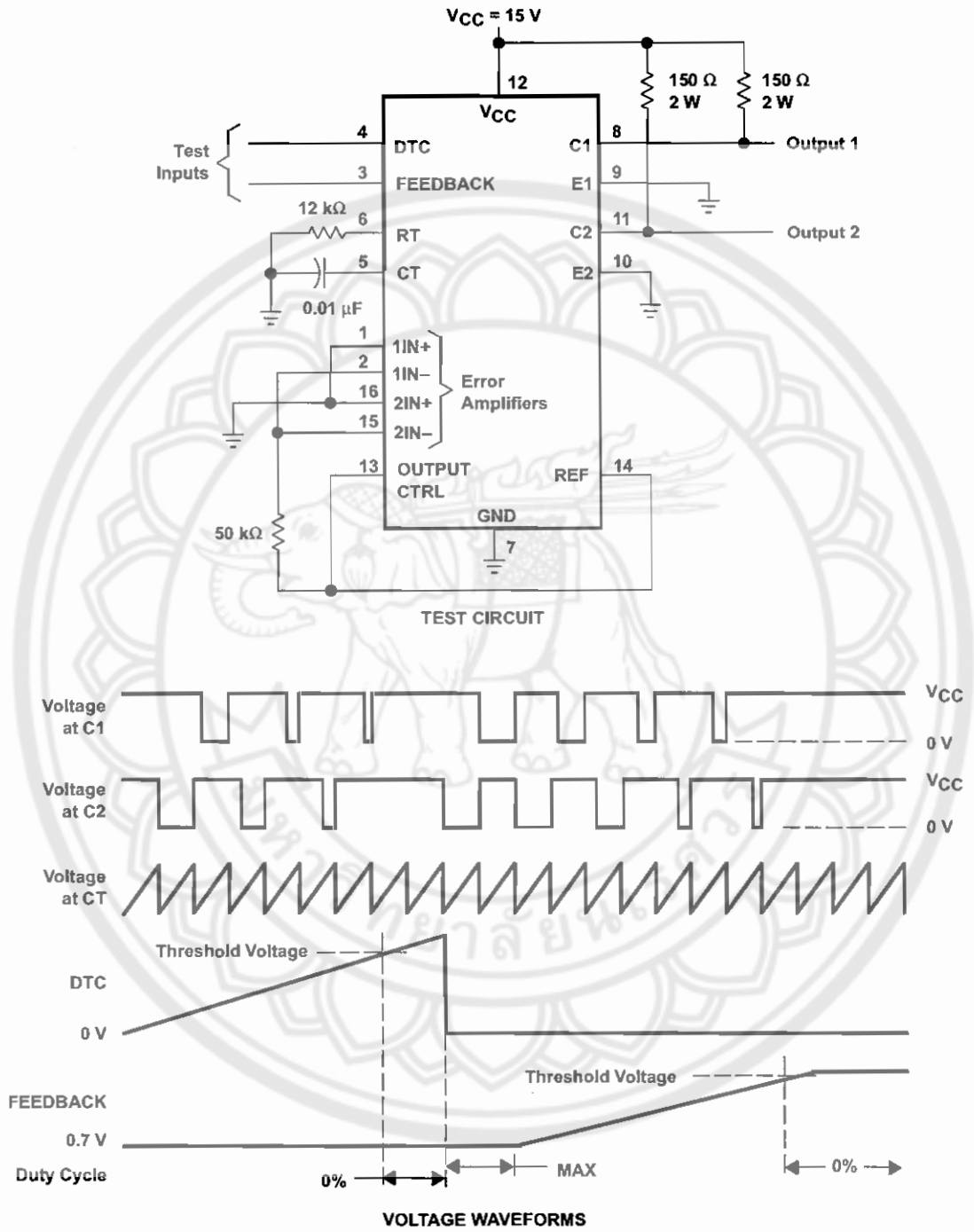


Figure 1. Operational Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

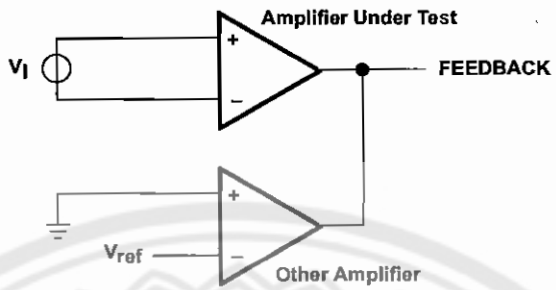
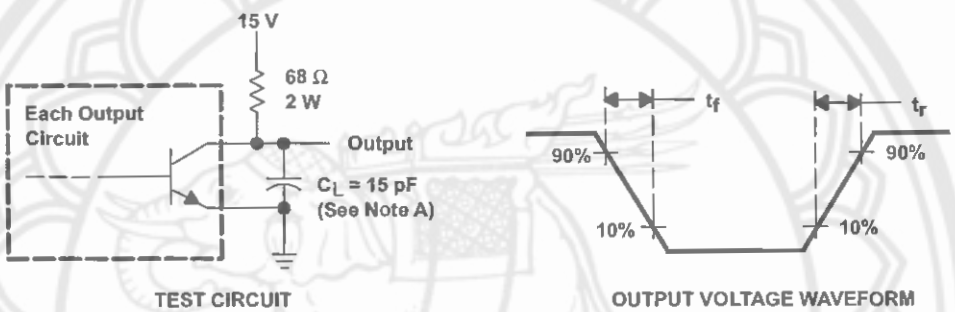
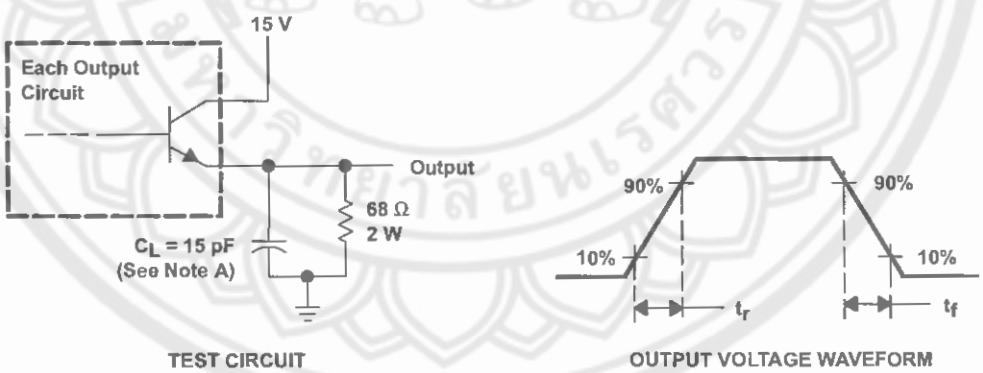


Figure 2. Amplifier Characteristics



NOTE A: C_L includes probe and jig capacitance.

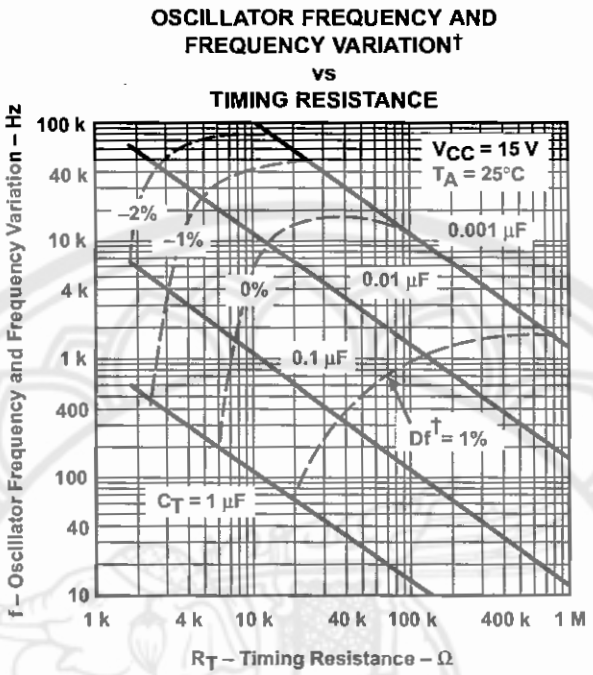
Figure 3. Common-Emitter Configuration



NOTE A: C_L includes probe and jig capacitance.

Figure 4. Emitter-Follower Configuration

TYPICAL CHARACTERISTICS



† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

Figure 5

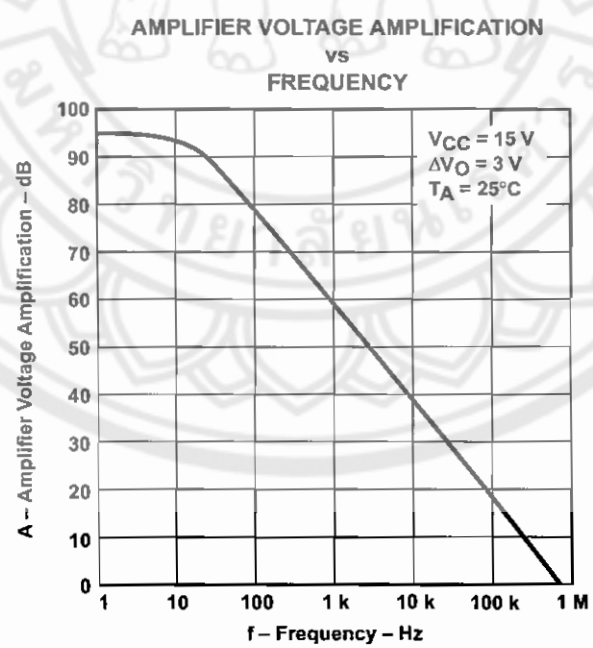


Figure 6

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ภาคผนวก จ

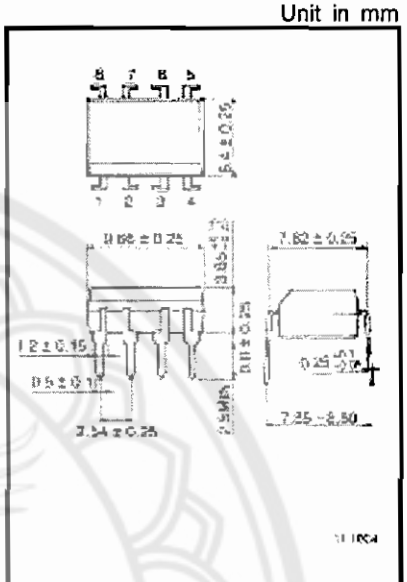
ข้อมูลไอซี TLP250

TOSHIBA Photocoupler GaAlAs Ired & Photo-IC

TLP250

Transistor Inverter
Inverter For Air Conditionor
IGBT Gate Drive
Power MOS FET Gate Drive

Unit in mm



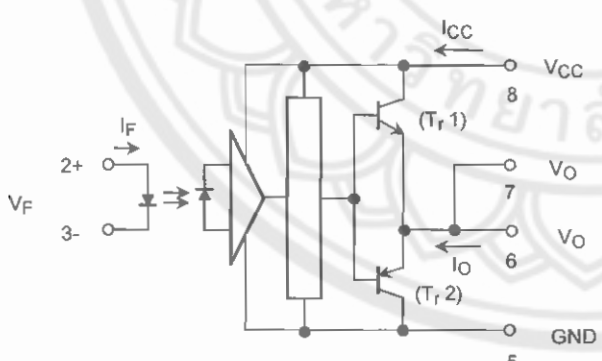
TOSHIBA 11-10C4
Weight: 0.54 g

The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.
This unit is 8-lead DIP package.
TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: I_F=5mA(max.)
- Supply current (I_{CC}): 11mA(max.)
- Supply voltage (V_{CC}): 10-35V
- Output current (I_O): ±1.5A (max.)
- Switching time (t_{pLH}/t_{pHL}): 1.5μs(max.)
- Isolation voltage: 2500V_{rms}(min.)
- UL recognized: UL1577, file No.E67349
- Option (D4) type
  VDE approved: DIN VDE0884/06.92,certificate No.76823
  Maximum operating insulation voltage: 630V_{PK}
  Highest permissible over voltage: 4000V_{PK}

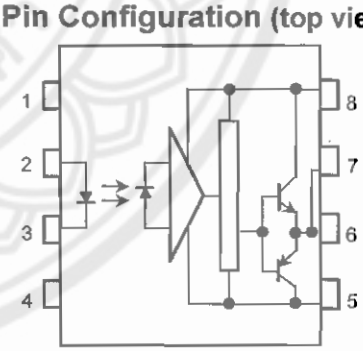
  (Note) When a VDE0884 approved type is needed, please designate the "option (D4)"
- Creepage distance: 6.4mm(min.)
  Clearance: 6.4mm(min.)

Schmatic



A 0.1μF bypass capcitor must be connected between pin 8 and 5 (See Note 5).

Pin Configuration (top view)



1 : N.C.
2 : Anode
3 : Cathode
4 : N.C.
5 : GND
6 : V_O (Output)
7 : V_O
8 : V_{CC}

Truth Table

		Tr1	Tr2
Input LED	On	On	Off
	Off	Off	On

Absolute Maximum Ratings (Ta = 25°C)

	Characteristic		Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Forward current derating (Ta ≥ 70°C)		$\Delta I_F / \Delta Ta$	−0.36	mA / °C
	Peak transient forward curent	(Note 1)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Junction temperature		Tj	125	°C
Detector	"H"peak output current (P_W ≤ 2.5μs,f ≤ 15kHz)	(Note 2)	I_{OPH}	−1.5	A
	"L"peak output current (P_W ≤ 2.5μs,f ≤ 15kHz)	(Note 2)	I_{OPL}	+1.5	A
	Output voltage	(Ta ≤ 70°C)	V_O	35	V
		(Ta = 85°C)		24	
	Supply voltage	(Ta ≤ 70°C)	V_{CC}	35	V
		(Ta = 85°C)		24	
	Output voltage derating (Ta ≥ 70°C)		$\Delta V_O / \Delta Ta$	−0.73	V / °C
	Supply voltage derating (Ta ≥ 70°C)		$\Delta V_{CC} / \Delta Ta$	−0.73	V / °C
	Junction temperature		Tj	125	°C
Operating frequency		(Note 3)	f	25	kHz
Operating temperature range			T_{opr}	−20~85	°C
Storage temperature range			T_{stg}	−55~125	°C
Lead soldering temperature (10 s)		(Note 4)	T_{sol}	260	°C
Isolation voltage (AC, 1 min., R.H.≤ 60%)		(Note 5)	BV_S	2500	Vrms

Note 1: Pulse width P_W ≤ 1μs, 300pps

Note 2: Exporenential wavefom

Note 3: Exporenential wavefom, I_{OPH} ≤ −1.0A(≤ 2.5μs), I_{OPL} ≤ +1.0A(≤ 2.5μs)

Note 4: It is 2 mm or more from a lead root.

Note 5: Device considerd a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 6: A ceramic capacitor(0.1μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching proparty. The total lead length between capacitor and coupler should not exceed 1cm.

Recommended Operating Conditions

Characteristic		Symbol	Min.	Typ.	Max.		Unit
Input current, on	(Note 7)	$I_{F(ON)}$	7	8	10		mA
Input voltage, off		$V_{F(OFF)}$	0	—	0.8		V
Supply voltage		V_{CC}	15	—	30	20	V
Peak output current		I_{OPH}/I_{OPL}	—	—	±0.5		A
Operating temperature		T_{opr}	−20	25	70	85	°C

Note 7: Input signal rise time (fall time) < 0.5 μs.

Electrical Characteristics (Ta = –20~70°C, unless otherwise specified)

Characteristic		Symbol	Test Cir–cuit	Test Condition		Min.	Typ.*	Max.	Unit
Input forward voltage		V_F	—	I_F = 10 mA , Ta = 25°C			1.6	1.8	V
Temperature coefficient of forward voltage		$\Delta V_F / \Delta Ta$	—	I_F = 10 mA		—	–2.0	—	mV / °C
Input reverse current		I_R	—	V_R = 5V, Ta = 25°C			—	10	μA
Input capacitance		C_T	—	V = 0 , f = 1MHz , Ta = 25°C		—	45	250	pF
Output current	"H" level	I_{OPH}	3	V_{CC} = 30V (*1)	I_F = 10 mA V_{8-6} = 4V	–0.5	–1.5	—	A
	"L" level	I_{OPL}	2		I_F = 0 V_{6-5} = 2.5V	0.5	2	—	
Output voltage	"H" level	V_{OH}	4	V_{CC1} = +15V, V_{EE1} = –15V R_L = 200Ω, I_F = 5mA		11	12.8	—	V
	"L" level	V_{OL}	5	V_{CC1} = +15V, V_{EE1} = –15V R_L = 200Ω, V_F = 0.8V		—	–14.2	–12.5	
Supply current	"H" level	I_{CCH}	—	V_{CC} = 30V, I_F = 10mA Ta = 25°C		—	7	—	mA
				V_{CC} = 30V, I_F = 10mA		—	—	11	
	"L" level	I_{CCL}	—	V_{CC} = 30V, I_F = 0mA Ta = 25°C		—	7.5	—	
				V_{CC} = 30V, I_F = 0mA		—	—	11	
Threshold input current	"Output L→H"	I_{FLH}	—	V_{CC1} = +15V, V_{EE1} = –15V R_L = 200Ω, V_O > 0V		—	1.2	5	mA
Threshold input voltage	"Output H→L"	I_{FHL}	—	V_{CC1} = +15V, V_{EE1} = –15V R_L = 200Ω, V_O < 0V		0.8	—	—	V
Supply voltage		V_{CC}	—			10	—	35	V
Capacitance (input–output)		C_S	—	V_S = 0 , f = 1MHz Ta = 25• •		—	1.0	2.0	pF
Resistance(input–output)		R_S	—	V_S = 500V , Ta = 25°C R.H.≤ 60%		1×10^{12}	10^{14}	—	Ω

* All typical values are at Ta = 25°C (*1): Duration of I_O time ≤ 50μs

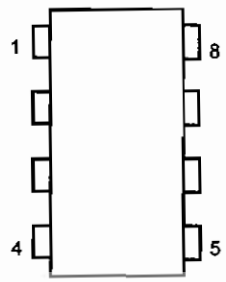
Switching Characteristics (Ta = −20~70°C , unless otherwise specified)

Characteristic		Symbol	Test Cir-cuit	Test Condition	Min.	Typ.*	Max.	Unit
Propagation delay time	L→H	t_{pLH}	6	I_F = 8mA (Note 7) V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω	—	0.15	0.5	μs
	H→L	t_{pHL}			—	0.15	0.5	
Output rise time		t_r			—	—	—	
Output fall time		t_f			—	—	—	
Common mode transient immunity at high level output		C_{MH}	7	V_{CM} = 600V, I_F = 8mA V_{CC} = 30V, Ta = 25°C	−5000	—	—	V / μs
Common mode transient immunity at low level output		C_{ML}	7	V_{CM} = 600V, I_F = 0mA V_{CC} = 30V, Ta = 25°C	5000	—	—	V / μs

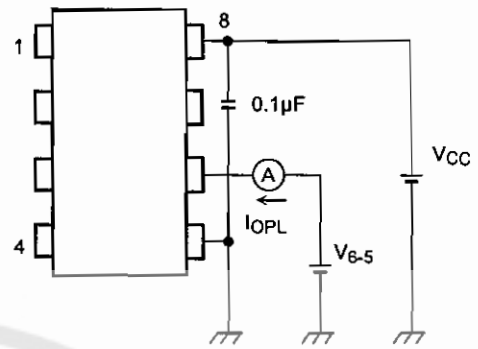
* All typical values are at Ta = 25°C

Note 7: Input signal rise time (fall time) < 0.5 μs.

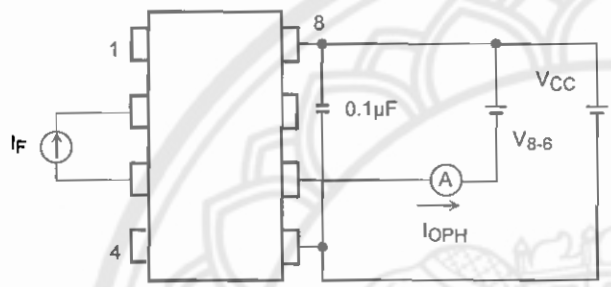
Test Circuit 1 :



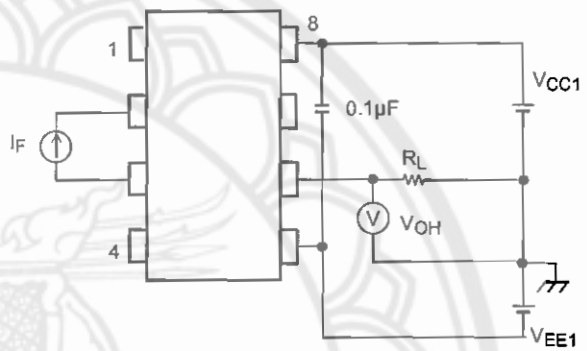
Test Circuit 2 : IOPL



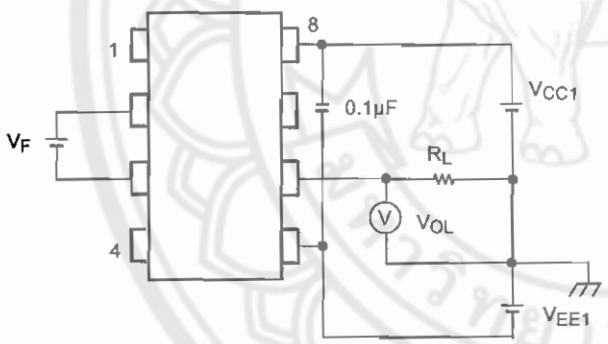
Test Circuit 3 : IOPH



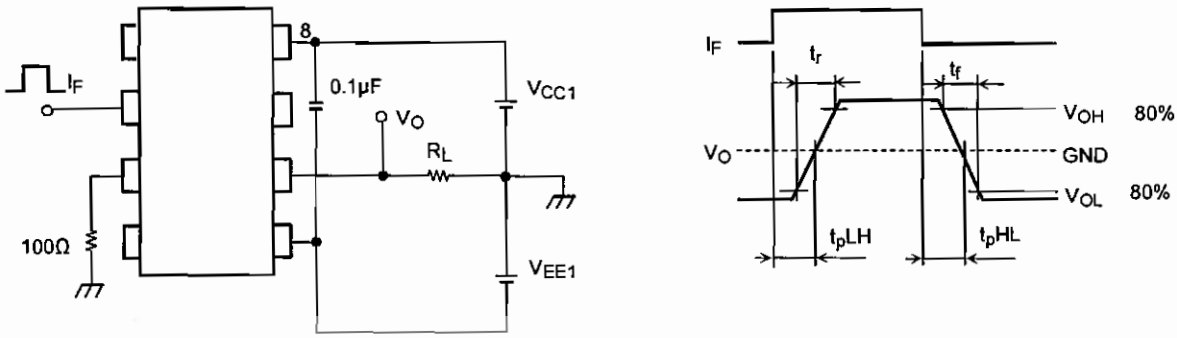
Test Circuit 4 : VOH



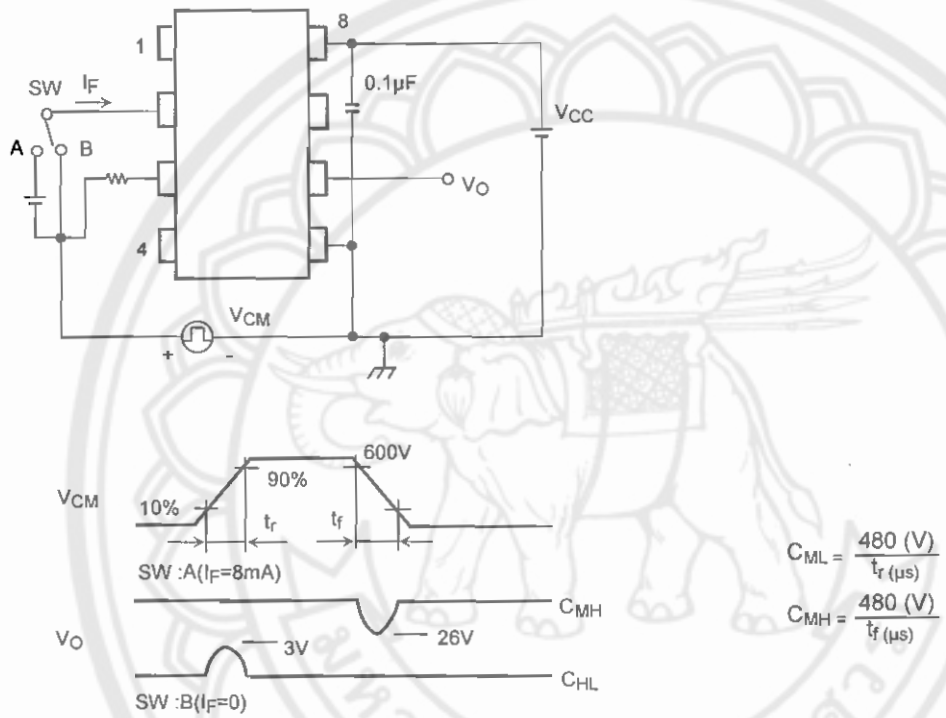
Test Circuit 5 : V_{OL}



Test Circuit 6: t_{pLH}, t_{pHL}, t_r t_f



Test Circuit 7: C_{MH}, C_{ML}

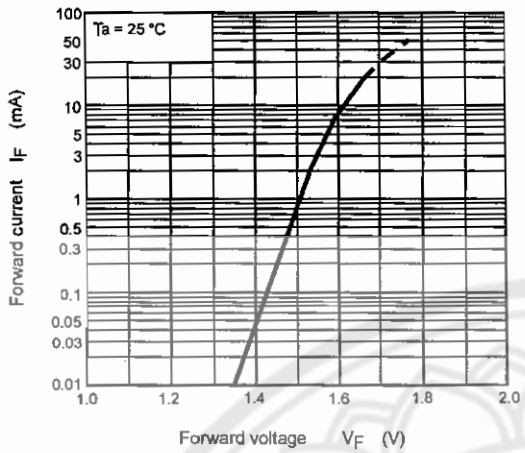


$$C_{ML} = \frac{480\ (V)}{t_{r\ (\mu s)}}$$

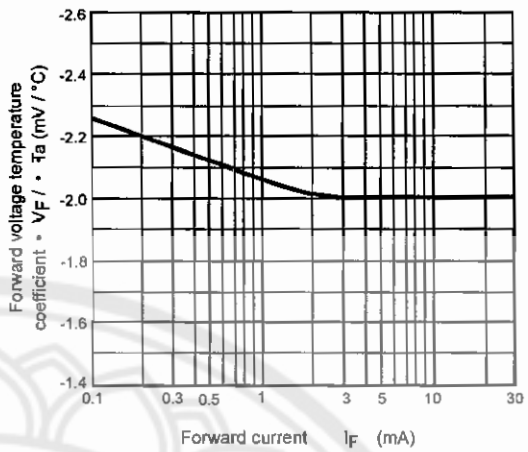
$$C_{MH} = \frac{480\ (V)}{t_{f\ (\mu s)}}$$

C_{ML}(C_{MH}) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

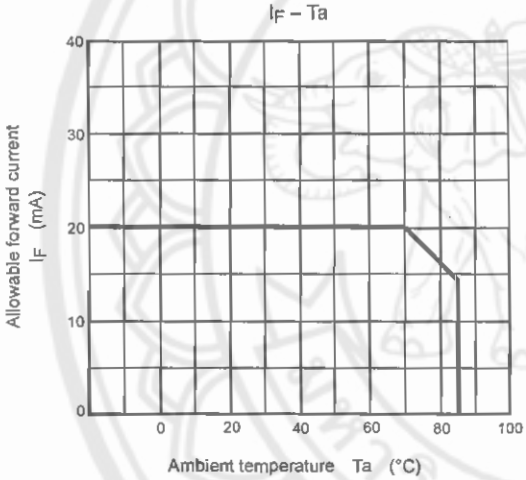
$I_F - V_F$



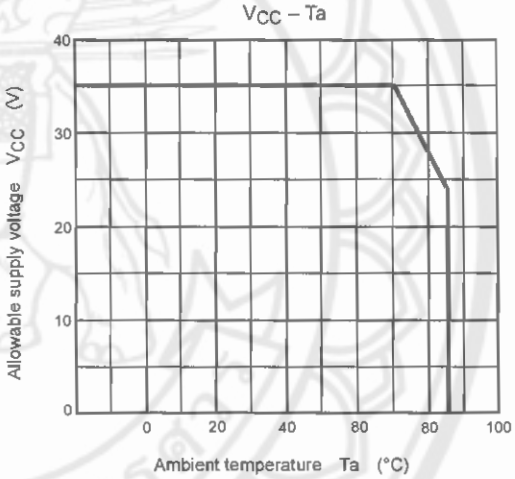
$\Delta V_F / \Delta Ta - I_F$



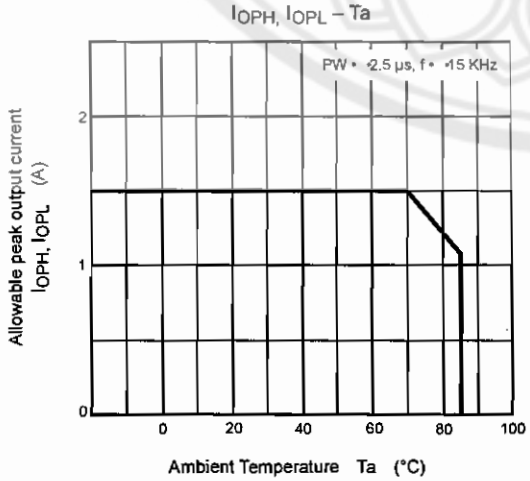
$I_F - Ta$



$V_{CC} - Ta$



$I_{OPH}, I_{OPL} - Ta$



ภาคผนวก ฉ

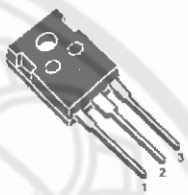
ข้อมูลมอสเฟตกำลัง IRFP450

IRFP450

N - CHANNEL 500V - 0.33Ω - 14A - TO-247
PowerMESH™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRFP450	500 V	< 0.4 Ω	14 A

- TYPICAL $R_{DS(on)}$ = 0.33 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED



TO-247

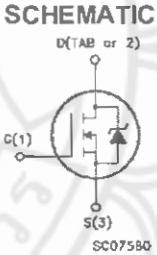
DESCRIPTION

This power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

APPLICATIONS

- HIGH CURRENT SWITCHING
- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- DC/DC COVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	500	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	14	A
I_D	Drain Current (continuous) at T_c = 100 °C	8.7	A
I_{DM}(•)	Drain Current (pulsed)	56	A
P_{tot}	Total Dissipation at T_c = 25 °C	190	W
	Derating Factor	1.5	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤14 A, di/dt ≤ 130 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, Tj ≤ T_{JMAX}

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	0.66	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	30	oC/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.1	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	14	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	800	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	500			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 8.4 A		0.33	0.4	Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ V_{GS} = 10 V	14			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ I_D = 8.4 A	9.3	13		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		2600 330 40		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	V_{DD} = 250 V I_D = 7A		24		ns
t_r	Rise Time	R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 1)		14		ns
Q_g	Total Gate Charge	V_{DD} = 400 V I_D = 14A V_{GS} = 10 V		75		nC
Q_{gs}	Gate-Source Charge			13.5		nC
Q_{gd}	Gate-Drain Charge			27		nC

SWITCHING OFF

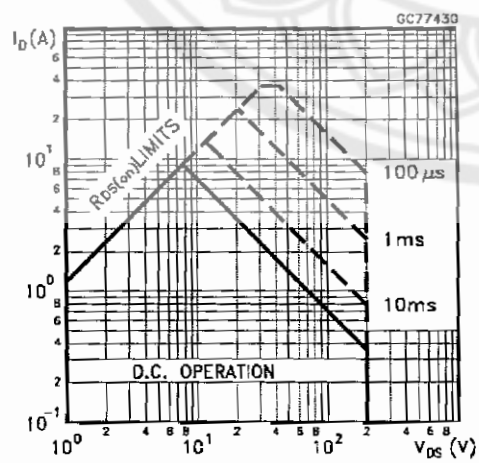
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 400 V I_D = 14 A		15		ns
t_f	Fall Time	R_G = 4.7 Ω V_{GS} = 10 V		25		ns
t_c	Cross-over Time	(see test circuit, figure 3)		35		ns

SOURCE DRAIN DIODE

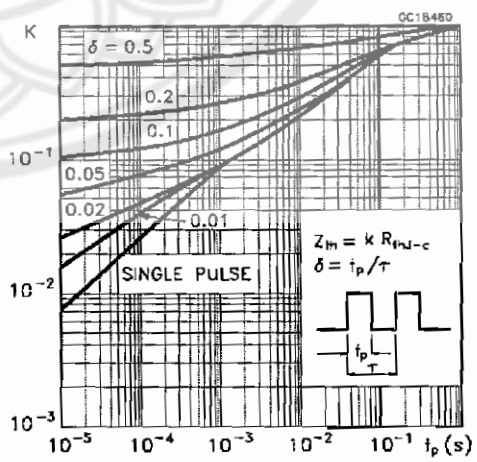
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				14	A
I_{SDM}(•)	Source-drain Current (pulsed)				56	A
V_{SD} (*)	Forward On Voltage	I_{SD} = 14 A V_{GS} = 0			1.4	V
t_{rr}	Reverse Recovery Time	I_{SD} = 14 A di/dt = 100 A/µs V_{DD} = 100 V T_j = 150 °C		680		ns
Q_{rr}	Reverse Recovery Charge	(see test circuit, figure 3)		9		µC
I_{RRM}	Reverse Recovery Current			26		A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

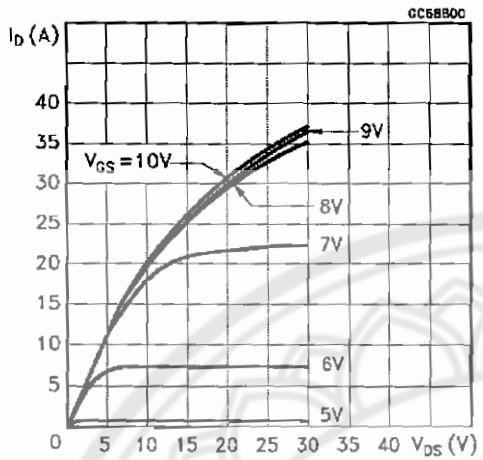
Safe Operating Area



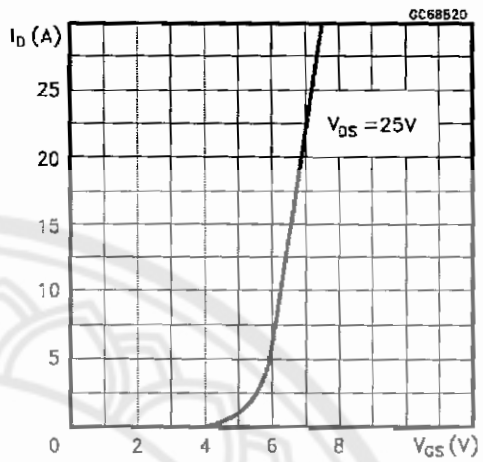
Thermal Impedance



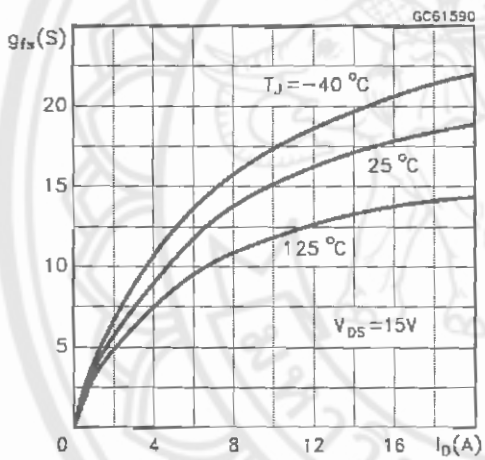
Output Characteristics



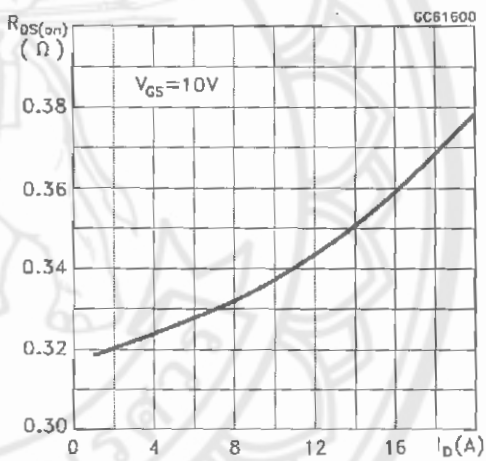
Transfer Characteristics



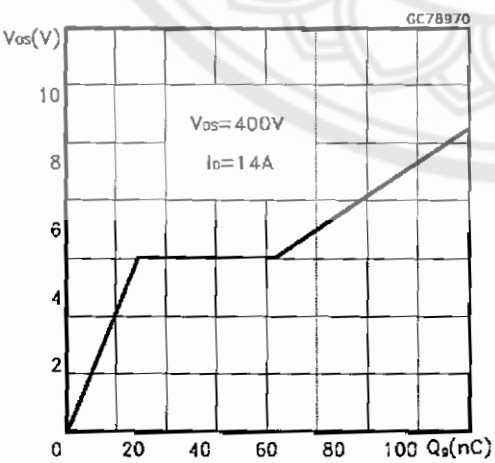
Transconductance



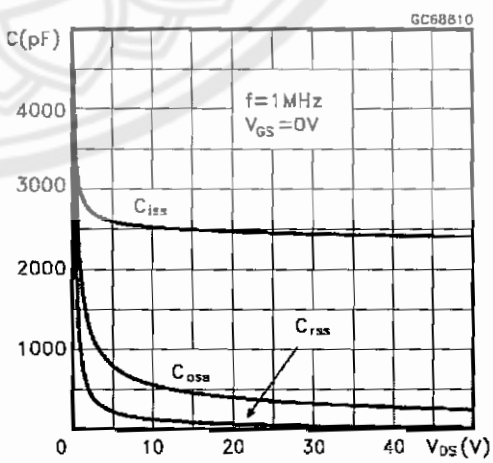
Static Drain-source On Resistance



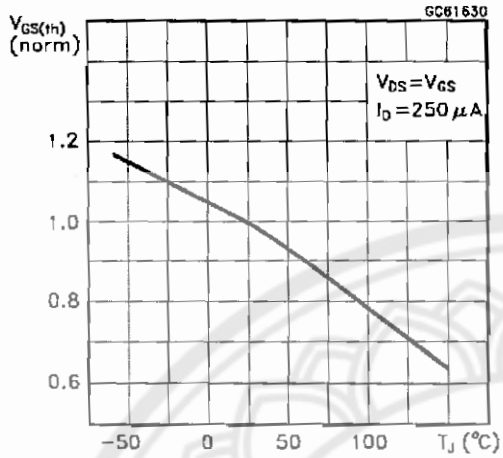
Gate Charge vs Gate-source Voltage



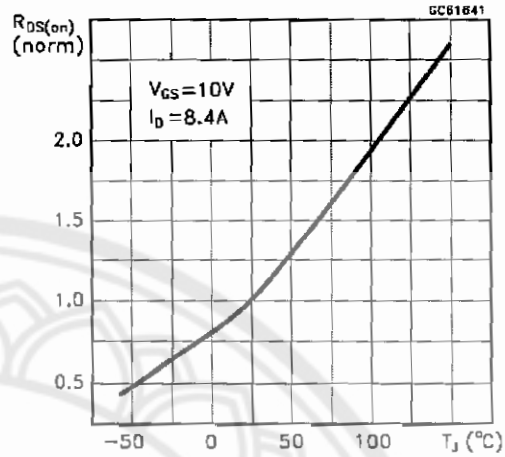
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

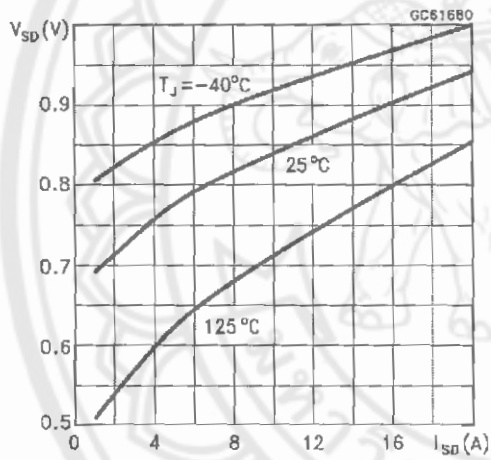


Fig. 1: Unclamped Inductive Load Test Circuit

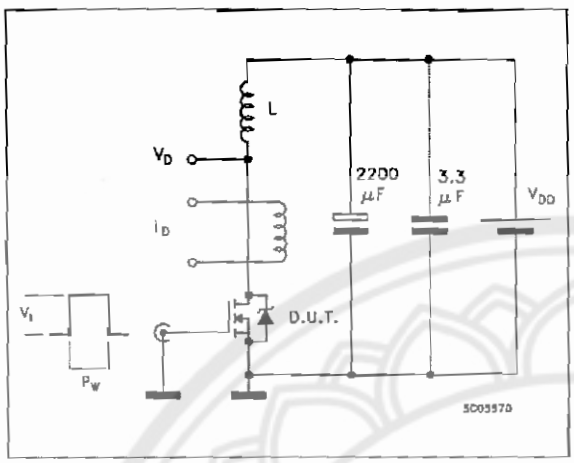


Fig. 1: Unclamped Inductive Waveform

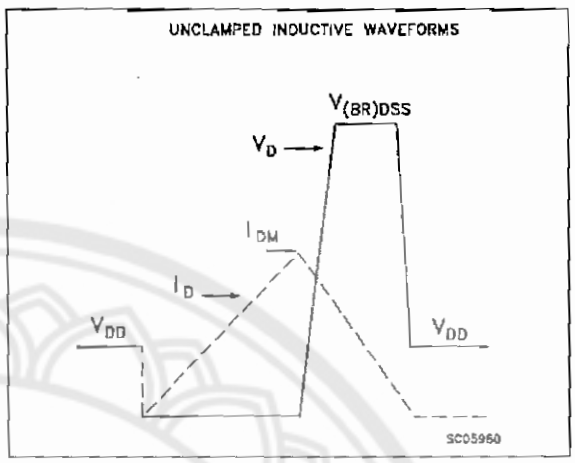


Fig. 3: Switching Times Test Circuits For Resistive Load

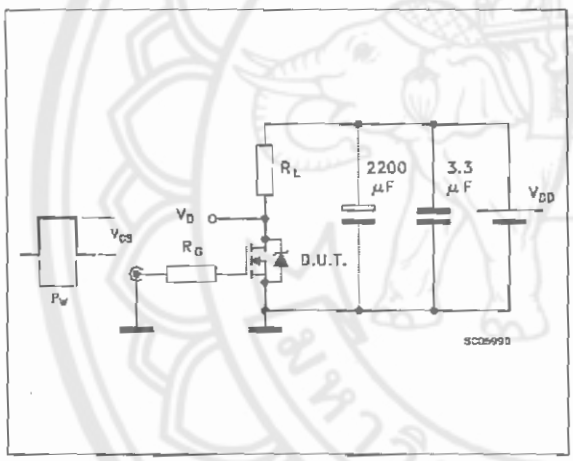


Fig. 4: Gate Charge test Circuit

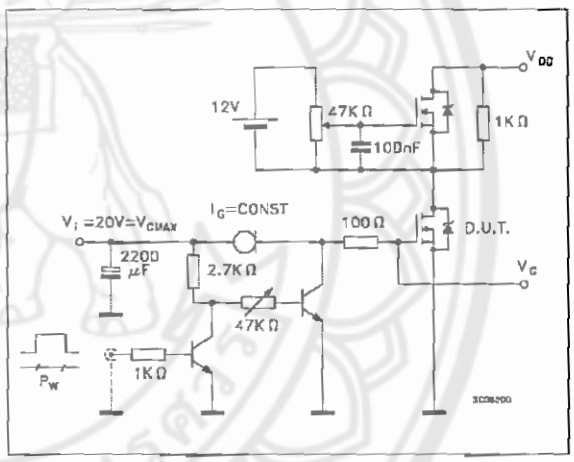
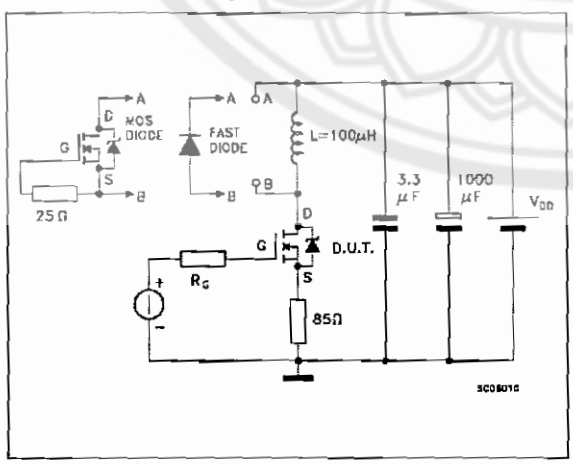


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559	0.413	0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118
Dia	3.55		3.65	0.140		0.144