ภาคผนวก

ChipCorder®
TECHNOLOGY BY ISD

ISD2560/75/90/120 Products

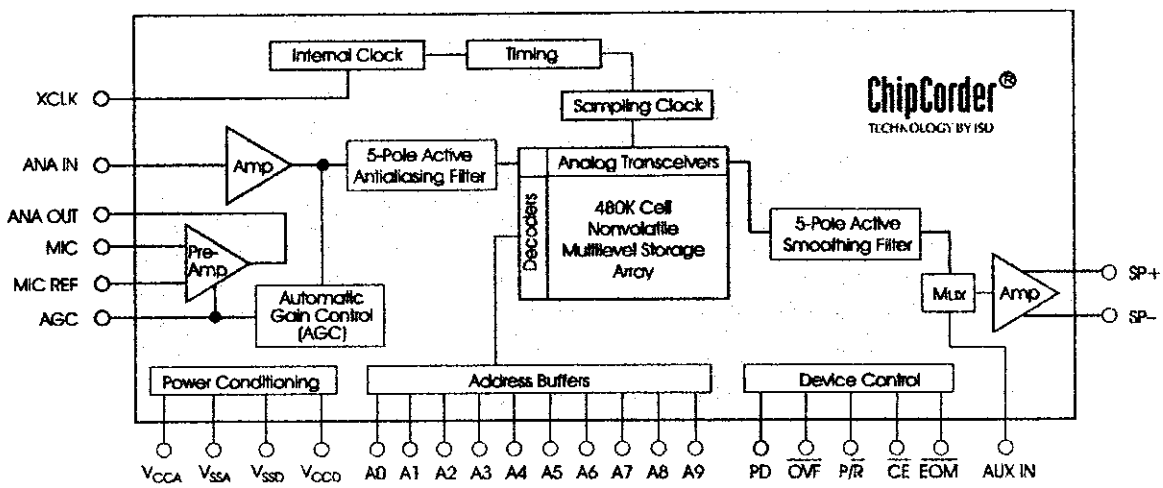
Single-Chip Voice Record/Playback Devices 60-, 75-, 90-, and 120-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD2500 ChipCorder® Series provides high-quality, single-chip record/playback solutions for 60- to 120-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, speaker amplifier, and high density multilevel storage array. In addition, the ISD2500 is microcontroller compatible, allowing complex messaging and addressing to be achieved.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure: ISD2560/75/90/120 Device Block Diagram



FEATURES

- Easy-to-use single-chip voice record/playback solution
- High-quality, natural voice/audio reproduction
- Manual switch or microcontroller compatible playback can be edge- or level-activated
- Single-chip durations of 60, 75, 90, and 120 seconds
- Directly cascadable for longer durations
- Automatic Power-Down (Push-Button Mode)
  - Standby current 1 μA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- Programmer support for play-only applications
- Single +5 volt power supply
- Available in die form, DIP, and TSOP packaging
- Industrial temperature (–40°C to +85°C) versions available

Table: ISD2560/75/90/120 Product Summary

Part Number	Duration (Seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.3	2.3
ISD25120	120	4.0	1.7

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FIGURES, CHARTS, AND TABLES IN THE ISD2560/75/90/120 PRODUCTS DATASHEET

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD2500 series includes devices offered at 4.0, 5.3, 6.4, and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects sound quality. Please refer to the ISD2560/75/90/120 Product Summary table on page *ii* to compare filter pass band and product durations.

The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state digital solutions.

DURATION

To meet end system requirements, the ISD2500 series offers single-chip solutions at 60, 75, 90, and 120 seconds. Parts may also be cascaded together for longer durations.

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

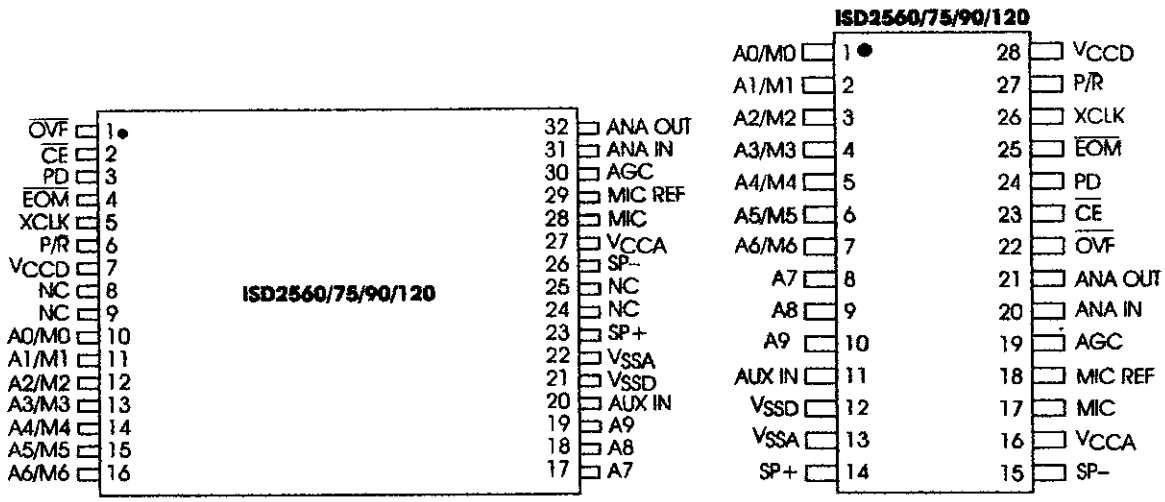
MICROCONTROLLER INTERFACE

In addition to its simplicity and ease of use, the ISD2500 series includes all the interfaces necessary for microcontroller-driven applications. The address and control lines can be interfaced to a microcontroller and manipulated to perform a variety of tasks, including message assembly, message concatenation, predefined fixed message segmentation, and message management.

PROGRAMMING

The ISD2500 series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via an ISD programmer.

Figure 1: ISD2560/75/90/120 Device Pinouts



PIN DESCRIPTIONS

VOLTAGE INPUTS (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

GROUND INPUTS (V_{SSA}, V_{SSD})

The ISD2500 series of devices utilizes separate analog and digital ground busses. These pins should be connected separately through a low-impedance path to power supply ground.

POWER DOWN INPUT (PD)

When not recording or playing back, the PD pin should be pulled HIGH to place the part in a very low power mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the record/playback space. The PD pin has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

CHIP ENABLE INPUT ($\overline{CE}$)

The $\overline{CE}$ pin is taken LOW to enable all playback and record operations. The address inputs and playback/record input (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

PLAYBACK/RECORD INPUT (P/$\overline{R}$)

The P/$\overline{R}$ input is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address inputs provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, an End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue past an $\overline{EOM}$ marker in an Operational Mode, or if $\overline{CE}$ is held LOW in address mode. (See page 5 for more Operational Modes).

END-OF-MESSAGE / RUN OUTPUT ($\overline{EOM}$)

A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message.

In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5 V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in playback-only mode.

When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH RUN signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for a visual indicator of a record or playback operation in process.

OVERFLOW OUTPUT ($\overline{OVF}$)

This signal pulses LOW at the end of memory space, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.

MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See Application Information for additional information on low-frequency cutoff calculation.

MICROPHONE REFERENCE INPUT (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.

AUTOMATIC GAIN CONTROL INPUT (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic on page 18) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.

ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

ANALOG INPUT (ANA IN)

The analog input pin transfers its signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD2500 devices has an internal pull-down device. These devices are configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. The internal clock has a ±5 percent tolerance over the industrial temperature and voltage range. A regulated power supply is recommended for industrial temperature range parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 1: External Clock Sample Rates

Part Number	Sample Rate	Required Clock
ISD2560	8.0 KHz	1024 KHz
ISD2575	6.4 KHz	819.2 KHz
ISD2590	5.3 KHz	682.7 KHz
ISD25120	4.0 KHz	512 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. **If the XCLK is not used, this input must be connected to ground.**

SPEAKER OUTPUTS (SP+/SP–)

All devices in the ISD2500 series include an on-chip differential speaker driver, capable of driving 50 mW into 16 Ω from AUX IN (12.2 mW from memory).

The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers.

NOTE *Connection of speaker outputs in parallel may cause damage to the device.*

A single output may be used alone (including a coupling capacitor between the SP pin and the speaker). These outputs may be used individually with the output signal taken from either pin. Using the differential outputs results in a 4 to 1 improvement in output power.

NOTE *Never ground or drive an unused speaker output.*

AUXILIARY INPUT (AUX IN)

The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH, P/$\overline{R}$ is HIGH, and playback is currently not active or if the device is in playback overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.

ADDRESS/MODE INPUTS (AX/MX)

The Address/Mode Inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address (A8 and A9).

If either or both of the two MSBs are LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{CE}$.

If both MSBs are HIGH, the Address/Mode Inputs are interpreted as Mode bits according to the Operational Mode table. There are six Operational Modes (M0..M6) available as indicated in the table. It is possible to use multiple Operational Modes simultaneously. Operational Modes are sampled on each falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.

OPERATIONAL MODES

The ISD2500 series is designed with several built-in Operational Modes that provide maximum functionality with minimum additional components. These are described in detail below. The Operational Modes use the address pins on the ISD2500 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH (A8 and A9), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, Operational Modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using Operational Modes. First, all operations begin initially at address 0, which is the beginning of the ISD2500 address space. Later operations can begin at other address locations, depending on the Operational Mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback, playback to record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when $\overline{CE}$ goes LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current address/mode levels are sampled and executed.

Table 2: Operational Modes Table

Mode Control	Function	Typical Use	Jointly Compatible[1]
M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from Address 0	M1, M5, M6
M4	Consecutive addressing	Record/play multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

1. Additional Operational Modes can be used simultaneously with the given mode.

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

M0 — MESSAGE CUEING

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for playback only, and is typically used with the M4 Operational Mode.

M1 — DELETE $\overline{EOM}$ MARKERS

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one $\overline{EOM}$ marker set at the end of the final message. When this Operational Mode is configured, messages recorded sequentially are played back as one continuous message.

M2 — UNUSED

When Operational Modes are selected, the M2 pin should be LOW.

M3 — MESSAGE LOOPING

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message can completely fill the ISD2500 device and will loop from beginning to end without $\overline{OVF}$ going LOW.

M4 — CONSECUTIVE ADDRESSING

During normal operations, the address pointer will reset when a message is played through to an $\overline{EOM}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{EOM}$, allowing messages to be played back consecutively.

M5 — $\overline{CE}$-LEVEL ACTIVATED

The default mode for ISD2500 devices is for $\overline{CE}$ to be edge-activated on playback and level-activated on record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during playback. This is specifically useful for terminating playback operations using the $\overline{CE}$ signal.

In this mode, $\overline{CE}$ LOW begins a playback cycle, at the beginning of the device memory. The playback cycle continues as long as $\overline{CE}$ is held LOW. When $\overline{CE}$ goes HIGH, playback will immediately end. A new $\overline{CE}$ LOW will restart the message from the beginning unless M4 is also HIGH.

M6 — PUSH-BUTTON MODE

The ISD2500 series of devices contain a Push-Button Operational Mode. The Push-Button mode is used primarily in very low-cost applications and is designed to minimize external circuitry and components, thereby reducing system cost. In order to configure the device in Push-Button Operational Mode, the two most significant address bits must be HIGH, and the M6 mode pin must also be HIGH. A device in this mode always powers down at the end of each playback or record cycle after $\overline{CE}$ goes HIGH.

When this Operational Mode is implemented, several of the pins on the device have alternate functionality:

Table 3: Alternate Functionality in Pins

Pin Name	Alternate Functionality in Push-Button Mode
$\overline{CE}$	Start/Pause Push-Button (LOW pulse-activated)
PD	Stop/Reset Push-Button (HIGH pulse activated)
$\overline{EOM}$	Active-HIGH Run Indicator

$\overline{CE}$ PIN (START/PAUSE)

In Push-Button Operational Mode, $\overline{CE}$ acts as a LOW-going pulse-activated START/PAUSE signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a playback or a record cycle according to the level on the P/$\overline{R}$ pin. A subsequent pulse on the $\overline{CE}$ pin, before an End-Of-Message is reached in playback or an overflow condition occurs, will cause the device to pause. The address counter is not reset, and another $\overline{CE}$ pulse will cause the device to continue the operation from the place where it was paused.

PD PIN (STOP/RESET)

In push-button Operational Mode, PD acts as a HIGH-going pulse-activated STOP/RESET signal. When a playback or record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated and the address pointer is reset to address 0, the beginning of the message space.

$\overline{EOM}$ PIN (RUN)

In Push-Button Operational Mode, $\overline{EOM}$ becomes an active-HIGH RUN signal which can be used to drive an LED or other external device. It is HIGH whenever a record or playback operation is in progress.

Recording in Push-Button Mode

1. The PD pin should be LOW, usually using a pull-down resistor.
2. The P/$\overline{R}$ pin is taken LOW.
3. The $\overline{CE}$ pin is pulsed LOW. Recording starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. The $\overline{CE}$ pin is pulsed LOW. Recording pauses, $\overline{EOM}$ goes back LOW. The internal address pointers are not cleared, but an EOM marker is stored in memory to point to the message end. The P/$\overline{R}$ pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.
5. The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set EOM marker. $\overline{EOM}$ goes back HIGH.

NOTE *If the M1 Operational Mode pin is also HIGH, the just previously written EOM bit is erased, and recording starts at that address.)*

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6. When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set EOM marker.

Playback in Push-Button Mode

1. The PD pin should be LOW.
2. The P/$\overline{R}$ pin is taken HIGH.
3. The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. If the $\overline{CE}$ pin is pulsed LOW or an EOM marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The P/$\overline{R}$ pin may be changed at this time. A subsequent record operation would not reset the address pointers and the recording would begin where playback ended.
5. $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.
6. Playback continues as in steps 4 and 5 until PD is pulsed HIGH or overflow occurs.
7. If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address 0.

NOTE *Push-button mode can be used in conjunction with modes M0, M1, and M3.*

GOOD AUDIO DESIGN PRACTICES

ISD products are very high-quality single-chip voice recording and playback systems. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling be followed. See the ISD Application Notes in this book for details.

ISD1000A COMPATIBILITY

The ISD2500 series of devices is designed to provide upward compatibility with the ISD1000A family. When designing with the ISD2500 series, the following differences should be noted.

ADDRESSING

The ISD2560/75/90/120 devices have 480K storage cells designed to provide 60 seconds of storage at a sampling rate of 8.0 KHz. This is approximately four times the storage of the ISD1000A family. To enable the same addressing resolution, two additional address pins have been added. The address space of each device is divisible into 600 increments with valid addressing from 00 to 257 Hex. Some higher addresses are mapped into the Operational Modes. All other addresses are invalid.

OVERFLOW

The ISD1000A series combined two functions on the $\overline{EOM}$ pin: end-of-message indication and overflow. The ISD2500 separates these two functions. Pin 25 (PDIP package) remains as $\overline{EOM}$, but outputs only the EOM signal indication. Pin 22 (PDIP package) becomes $\overline{OVF}$ and pulses LOW only when the device reaches its end of memory, or is "full." This change allows easy message cueing and addressability across device boundaries. This also means that the M2 Operational Mode found in the ISD1000A family is not implemented in the ISD2500 series.

PUSH-BUTTON MODE

The ISD2500 series includes an additional Operational Mode called Push-Button mode. This provides an alternative interface to the record and playback functions of the part. The $\overline{CE}$ and PD pins become redefined as edge-activated "push-buttons." A pulse on $\overline{CE}$ initiates a cycle, and if triggered again, pauses the current cycle without resetting the address pointer (i.e., a Start or Pause function). PD stops any current cycle and resets the address pointer to the beginning of the message space (i.e., a Stop and Reset function). Additionally, the $\overline{EOM}$ pin functions as an active-HIGH run indicator, and can be used to drive an LED indicating a record or playback operation is in progress. Devices in the Push-Button mode cannot be cascaded.

LOOPING MODE

The ISD2500 series can loop with a message that completely fills the memory space.

NOTE *Additional descriptions of ISD2500 device functionality and application examples are provided in the ISD Application Notes in this book.*

TIMING DIAGRAMS

Figure 2: Record

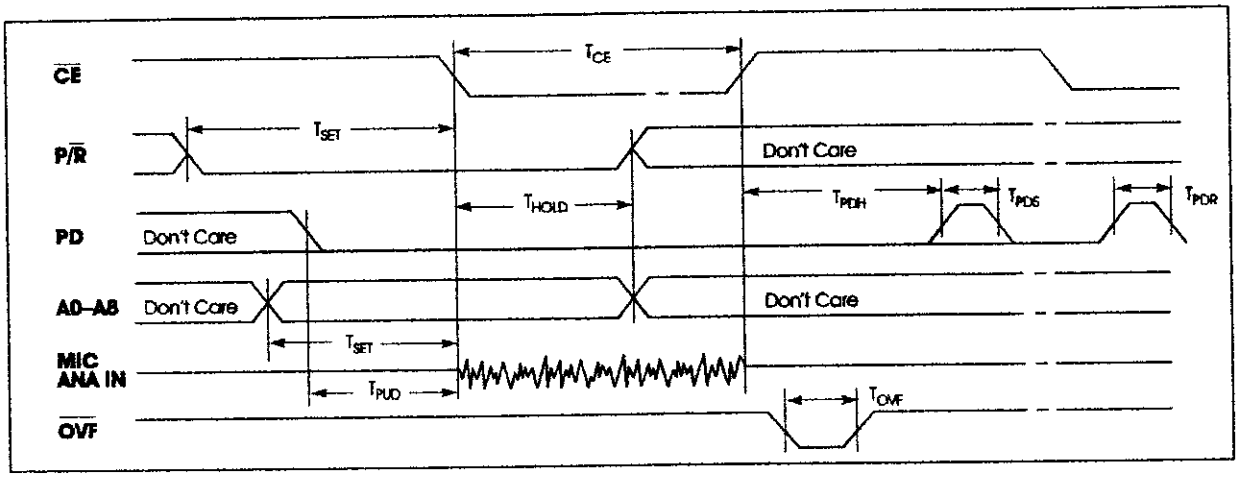


Figure 3: Playback

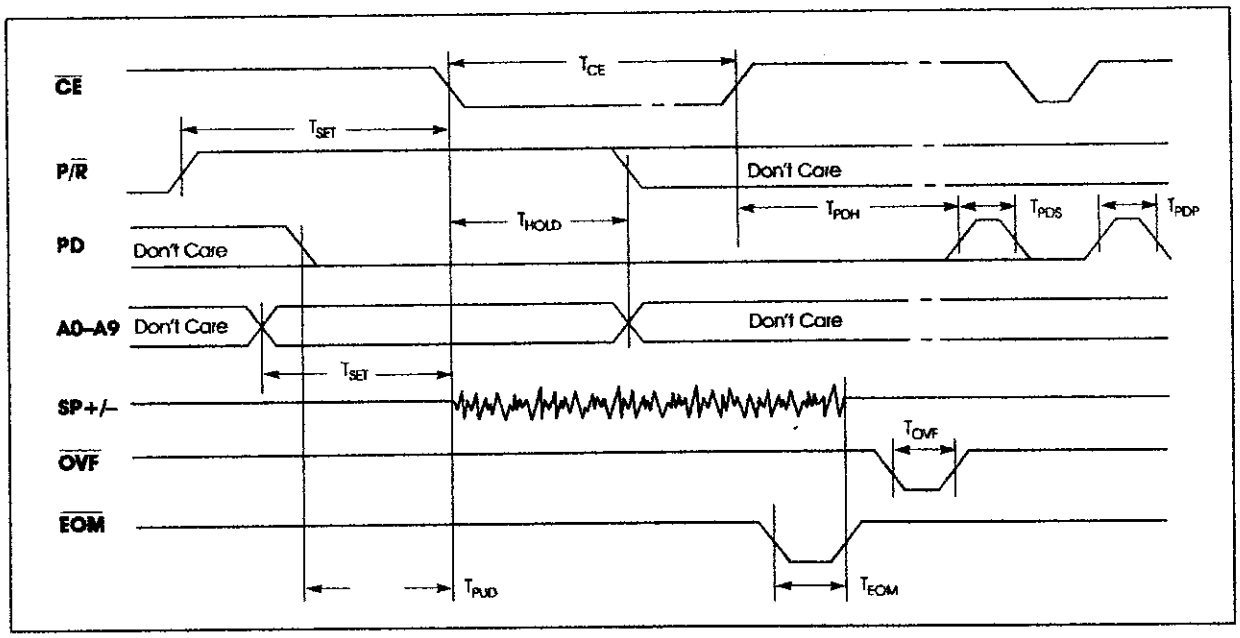


Table 4: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300°C
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Industrial operating temperature range[1]	–40°C to +85°C
Supply voltage (V_{CC})[2]	+4.5 V to +5.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
V_{OH1}	$\overline{OVF}$ Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH2}	$\overline{EOM}$ Output High Voltage	V_{CC} – 1.0	V_{CC} – 0.8		V	I_{OH} = –3.2 mA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$ [3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[3]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH with Pull Down			130	µA	Force V_{CC} [4]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp in Input Resistance	4	9	15	KΩ	MIC and MIC REF Pins
R_{AUX}	AUX INPUT Resistance	5	11	20	KΩ	

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
$R_{ANA\ IN}$	ANA IN Input Resistance	2.3	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		−15	5	dB	AGC = 2.5 V
A_{AUX}	AUX IN/SP+ Gain		0.98	1.0	V/V	
A_{ARP}	ANA IN to SP+/− Gain	21	23	26	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *XCLK pin only.*

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
F_S	Sampling Frequency	ISD2560		8.0		KHz	[7]
		ISD2575		6.4		KHz	[7]
		ISD2590		5.3		KHz	[7]
		ISD25120		4.0		KHz	[7]
F_{CF}	Filter Pass Band	ISD2560		3.4		KHz	3 dB Roll-Off Point [3] [8]
		ISD2575		2.7		KHz	3 dB Roll-Off Point [3] [8]
		ISD2590		2.3		KHz	3 dB Roll-Off Point [3] [8]
		ISD25120		1.7		KHz	3 dB Roll-Off Point [3] [8]
T_{REC}	Record Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation[7]
		ISD2560	56.5	60.0	63.8	sec	Industrial Operation[7]
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation[7]
		ISD2575	70.7	75.0	79.7	sec	Industrial Operation[7]
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation[7]
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation[7]
T_{PLAY}	Playback Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation
		ISD2560	56.5	60.0	63.8	sec	Industrial Operation
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation
		ISD2575	70.7	75.0	79.7	sec	Industrial Operation
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation
T_{CE}	$\overline{CE}$ Pulse Width			100		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{HOLD}	Control/Address Hold Time			0		nsec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
T_{PUD}	Power-Up Delay	ISD2560	24.1	25.0	27.8	msec	Commercial Operation
		ISD2560	23.5		28.5	msec	Industrial Operation
		ISD2575	30.2	31.3	34.3	msec	Commercial Operation
		ISD2575	29.3	31.3	35.2	msec	Industrial Operation
		ISD2590	36.2	37.5	40.8	msec	Commercial Operation
		ISD25120	48.2	50.0	53.6	msec	Commercial Operation
T_{PDR}	PD Pulse Width Record	ISD2560		25		msec	
		ISD2575		31.25		msec	
		ISD2590		37.5		msec	
		ISD25120		50.0		msec	
T_{PDP}	PD Pulse Width Play	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{PDS}	PD Pulse Width Static			100		nsec	[6]
T_{PDH}	Power Down Hold			0		nsec	
T_{EOM}	$\overline{EOM}$ Pulse Width	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{OVF}	Overflow Pulse Width			6.5		µsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2	50	mW	R_{EXT} = 16 Ω [4]
V_{OUT}	Voltage Across Speaker Pins				2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak [5]
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak
V_{IN3}	Aux Input Voltage				1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).*
4. *From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.*
5. *With 5.1 KΩ series resistor at ANA IN.*
6. *T_{PDS} is required during a static condition, typically overflow.*
7. *Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range and voltage range and ±5 percent over the industrial temperature and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).*
8. *Filter specification applies to both the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

Chart 1: Record Mode Operating Current (I_{CC})

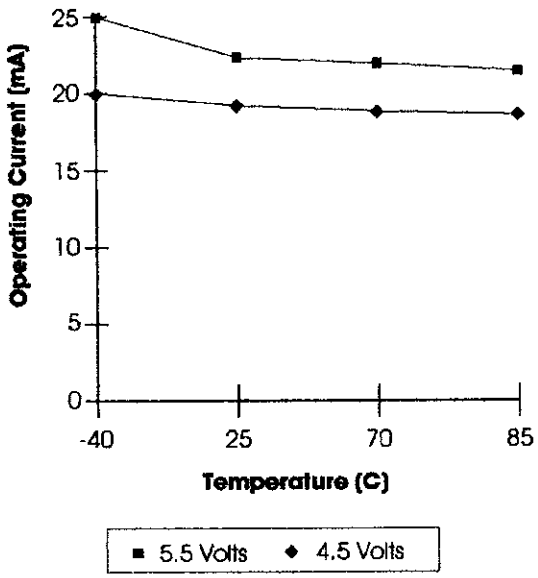


Chart 3: Standby Current (I_{SB})

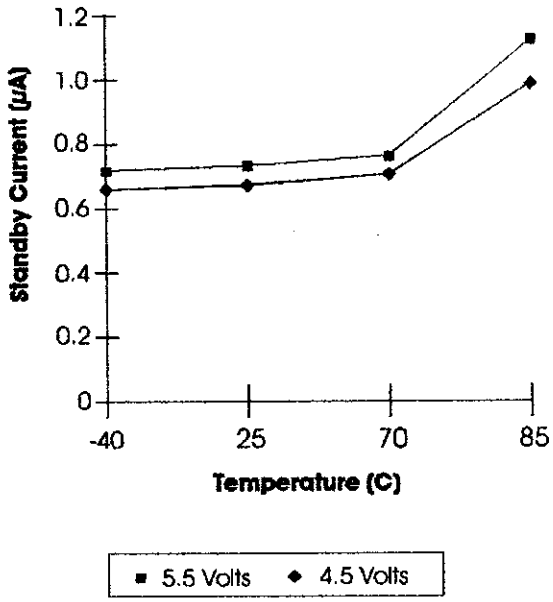


Chart 2: Total Harmonic Distortion

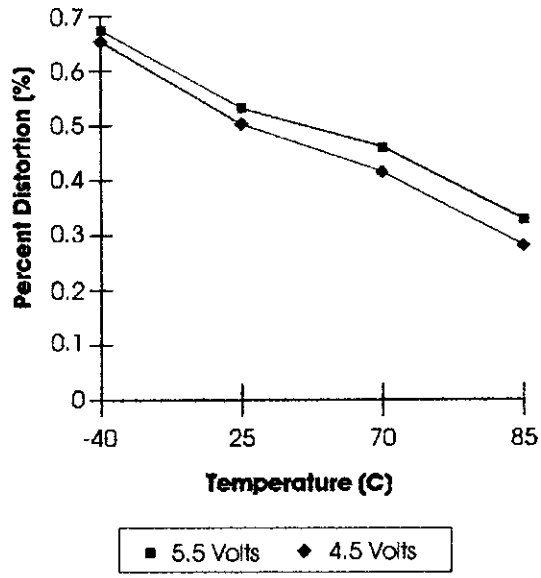


Chart 4: Oscillator Stability

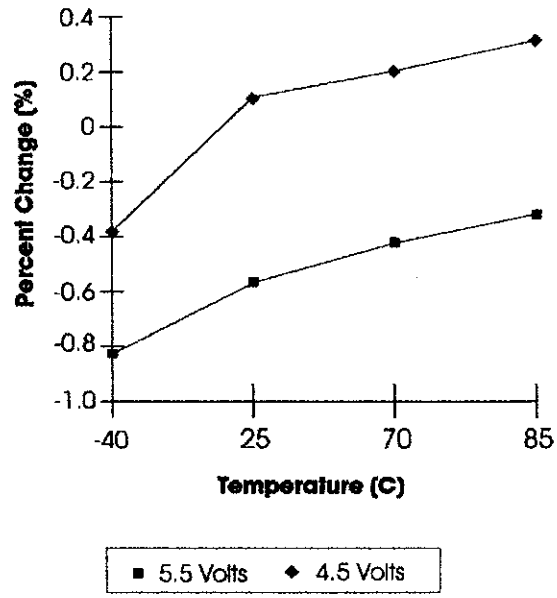


Table 8: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} –1.0 V) to (V_{CC} + 1.0 V)
$V_{CC} - V_{SS}$	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+4.5 V to +6.5 V
Ground voltage (V_{SS})[2]	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
V_{OH1}	$\overline{OVF}$ Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH2}	$\overline{EOM}$ Output High Voltage	V_{CC} – 1.0	V_{CC} – 0.8		V	I_{OH} = –3.2 mA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$ [3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[2]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH with Pull Down			130	µA	Force V_{CC} [4]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	15	KΩ	MIC and MIC REF Pads
R_{AUX}	AUX INput Resistance	5	11	20	KΩ	
$R_{ANA\ IN}$	ANA IN Input Resistance	2.3	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
A_{PRE2}	Preamp Gain 2		-15	5	dB	AGC = 2.5 V
A_{AUX}	AUX IN/SP+ Gain		0.98	1.0	V/V	
A_{ARP}	ANA IN to SP+/- Gain	21	23	26	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *XCLK pad only.*

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
F_S	Sampling Frequency	ISD2560		8.0		KHz	[7]
		ISD2575		6.4		KHz	[7]
		ISD2590		5.3		KHz	[7]
		ISD25120		4.0		KHz	[7]
F_{CF}	Filter Pass Band	ISD2560		3.4		KHz	3 dB Roll-Off Point [3] [8]
		ISD2575		2.7		KHz	3 dB Roll-Off Point [3] [8]
		ISD2590		2.3		KHz	3 dB Roll-Off Point [3] [8]
		ISD25120		1.7		KHz	3 dB Roll-Off Point [3] [8]
T_{REC}	Record Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation[7]
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation[7]
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation[7]
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation[7]
T_{PLAY}	Playback Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation[7]
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation[7]
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation[7]
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation[7]
T_{CE}	$\overline{CE}$ Pulse Width			100		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{HOLD}	Control/Address Hold Time			0		nsec	
T_{PUD}	Power-Up Delay	ISD2560	24.1	25.0	27.8	msec	Commercial Operation
		ISD2575	30.2	31.3	34.3	msec	Commercial Operation
		ISD2590	36.2	37.5	40.8	msec	Commercial Operation
		ISD25120	48.2	50.0	53.6	msec	Commercial Operation

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min[2]	Typ [1]	Max[2]	Units	Conditions
T_{PDR}	PD Pulse Width Record	ISD2560		25		msec	
		ISD2575		31.25		msec	
		ISD2590		37.5		msec	
		ISD25120		50.0		msec	
T_{PDP}	PD Pulse Width Play	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{PDS}	PD Pulse Width Static			100		nsec	[6]
T_{PDH}	Power Down Hold			0		nsec	
T_{EOM}	$\overline{EOM}$ Pulse Width	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{OVF}	Overflow Pulse Width			6.5		µsec	
THD	Total Harmonic Distortion			1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2	50	mW	R_{EXT} = 16 Ω[4]
V_{OUT}	Voltage Across Speaker Pins				2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak [5]
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak
V_{IN3}	Aux Input Voltage				1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).*
4. *From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.*
5. *With 5.1 KΩ series resistor at ANA IN.*
6. *T_{PDS} is required during a static condition, typically overflow.*
7. *Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).*
8. *Filter specification applies to the antialiasing filter and the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

Chart 5: Record Mode Operating Current (I_{CC})

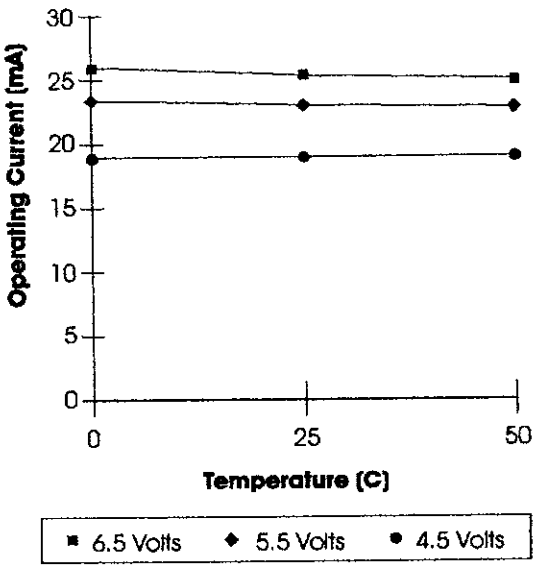


Chart 7: Standby Current (I_{SB})

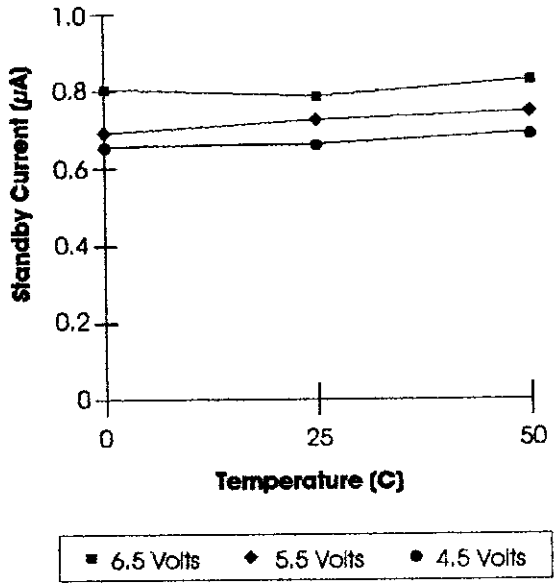


Chart 6: Total Harmonic Distortion

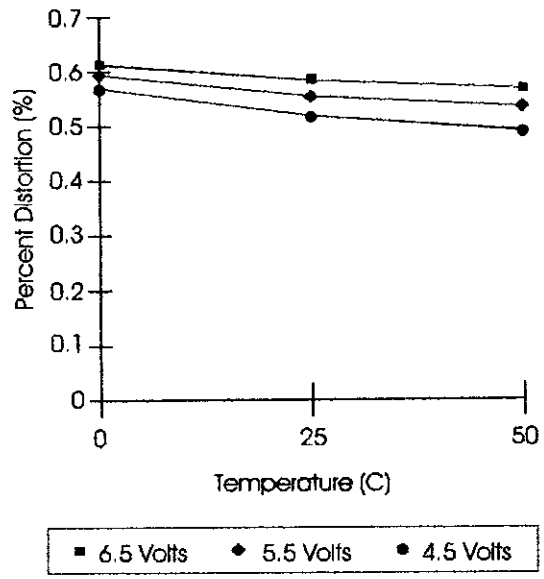


Chart 8: Oscillator Stability

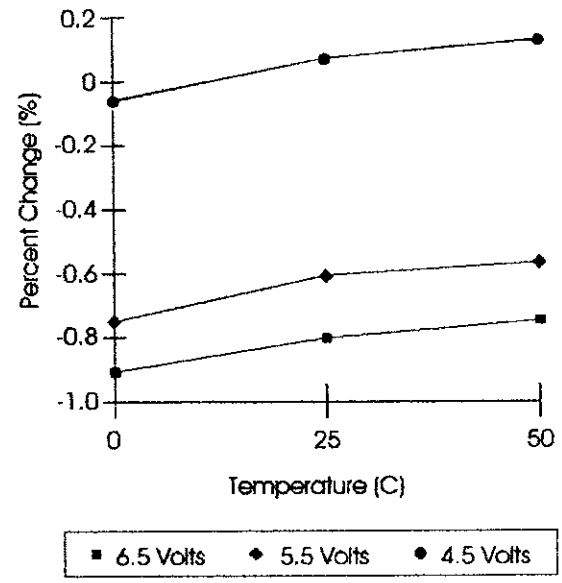
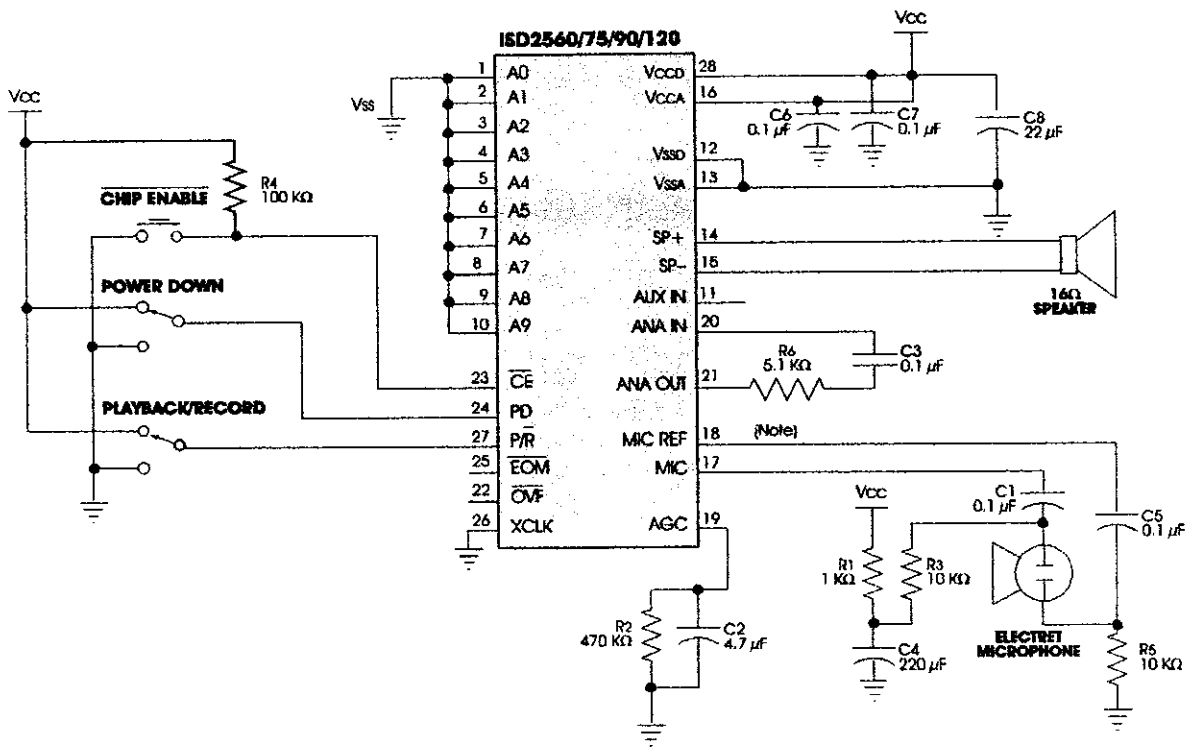


Figure 4: ISD2560/75/90/120 Application Example—Design Schematic



NOTE: *If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided in the Application Notes in this book.*

Table 12: Application Example—Basic Device Control

Control Step	Function	Action
1	Power up chip and select record/playback mode	(1.) PD = LOW, (2.) P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0–A9
3A	Begin playback	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulsed LOW
3B	Begin record	P/$\overline{R}$ = LOW, $\overline{CE}$ = LOW
4A 4B	End playback End record	Automatic PD or $\overline{CE}$ = HIGH

Table 13: Application Example—Passive Component Functions

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R5	Microphone biasing resistors	Provides biasing for microphone operation
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages.
R6	Series limiting resistor	Reduces level to high supply voltages
C1, C5	Microphone DC–blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-frequency cutoff and common mode noise rejection.
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply

EXPLANATION

In this simplified block diagram of a microcontroller application, the Push-Button mode and message cueing are used. The microcontroller is a 16-pin version with enough port pins for buttons, an LED, and the ISD2500 series device. The software can be written to use three buttons: one each for play and record, and one for message selection. Because the microcontroller is interpreting the buttons and commanding the ISD2500 device, software can be written for any functions desired in a particular application.

NOTE *ISD does not recommend connecting address lines directly to a microprocessor bus. Address lines should be externally latched.*

Figure 5: ISD2560/75/90/120 Application Example—Microcontroller/ISD2500 Interface

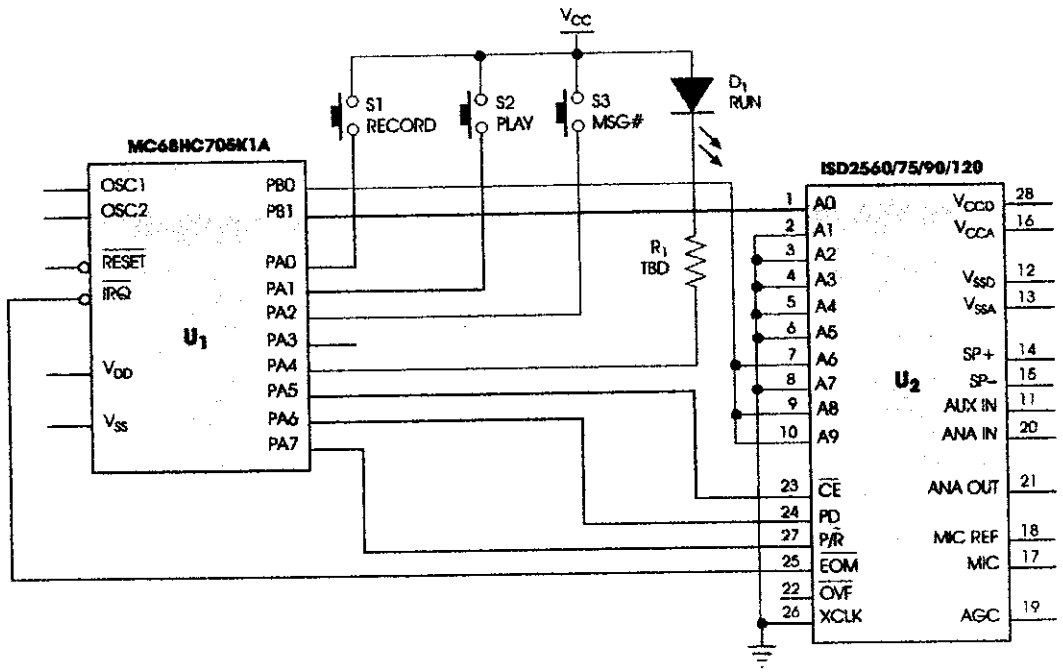
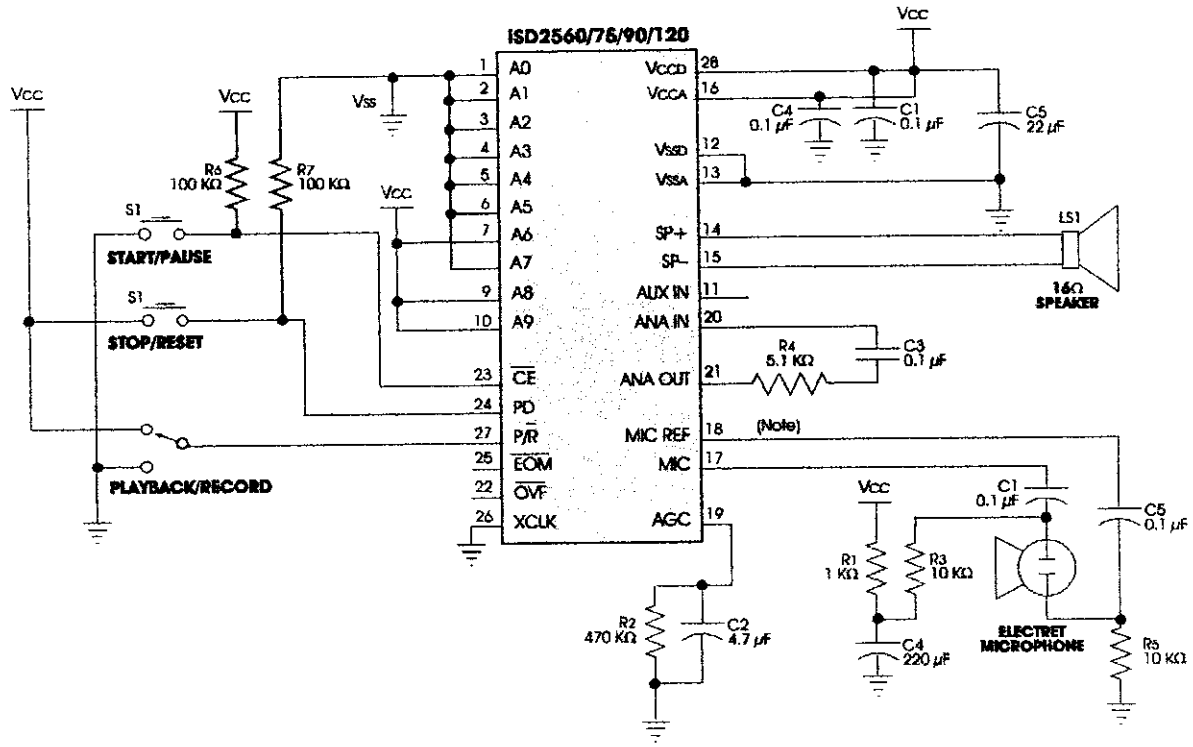


Figure 6: ISD2500 Application Example—Push-Button



NOTE: *Please refer to Application Information.*

Table 14: Application Example—Push-Button Control

Control Step	Function	Action
1	Select record/playback mode	P/$\overline{R}$ = As desired
2A 2B	Begin playback Begin record	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulsed LOW P/$\overline{R}$ = LOW, $\overline{CE}$ = Pulsed LOW
3	Pause record or playback	$\overline{CE}$ = Pulsed LOW
4A 4B	End playback End record	Automatic at $\overline{EOM}$ marker or PD = Pulsed HIGH PD = Pulsed HIGH

Table 15: Application Example—Passive Component Functions

Part	Function	Comments
R2	Release time constant	Sets release time for AGC
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6, R7	Pull-up and pull-down resistors	Defines static state of inputs
C1, C4, C5	Power supply capacitors	Filters and bypass of power supply
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff

Table 16: Push-Button Parameters

Symbol	Characteristic		Min	Typ (1)	Max	Units	Conditions
T_{CE}	$\overline{CE}$ Pulse Width [Start/Pause]			300		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{PUD}	Power-Up Delay	ISD2560 ISD2575 ISD2590 ISD25120		25 31.25 37.25 50.0		msec msec msec msec	
T_{PD}	PD Pulse Width [Stop/Reset]			300		nsec	
T_{RUN}	$\overline{CE}$ to $\overline{EOM}$ HIGH		25		400	nsec	
T_{PAUSE}	$\overline{CE}$ to $\overline{EOM}$ LOW		50		400	nsec	
T_{DB}	$\overline{CE}$ HIGH Debounce	ISD2560 ISD2575 ISD2590 ISD25120	70 85 105 135		105 135 160 215	msec msec msec msec	

PUSH-BUTTON TIMING DIAGRAMS

Figure 7: Push-Button Mode Record

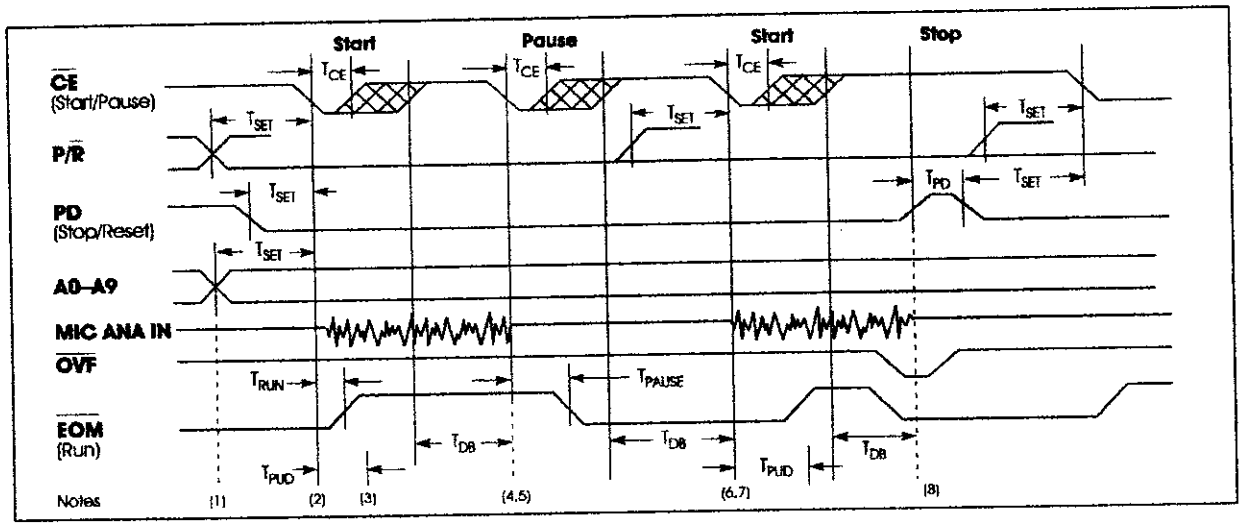
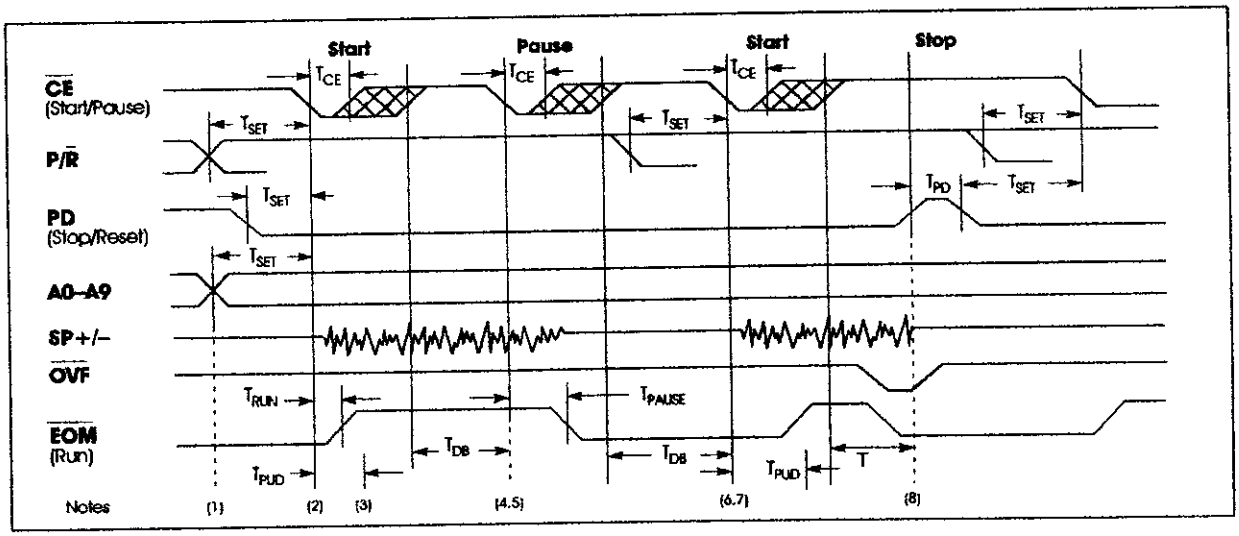


Figure 8: Push-Button Mode Playback



1. *A9, A8, and A6 = 1 for push-button operation.*
2. *The first $\overline{CE}$ LOW pulse performs a Start function.*
3. *The part will begin to play or record after a power-up delay T_{PUD}.*
4. *The part must have $\overline{CE}$ HIGH for a debounce period TDB before it will recognize another falling edge of $\overline{CE}$ and pause.*
5. *The second $\overline{CE}$ LOW pulse, and every even pulse thereafter, performs a Pause function.*
6. *Again, the part must have $\overline{CE}$ HIGH for a debounce period TDB before it will recognize another falling edge of CE, which would restart an operation. In addition, the part will not do an internal power down until CE is HIGH for the TDB time.*
7. *The third $\overline{CE}$ LOW pulse, and every odd pulse thereafter, performs a Resume function.*
8. *At any time, a HIGH level on PD will stop the current function, reset the address counter, and power down the device.*

DEVICE PHYSICAL DIMENSIONS

Figure 9: 28-Lead 8x13.4mm Plastic Thin Small Outline Package (TSOP) Type I (E)

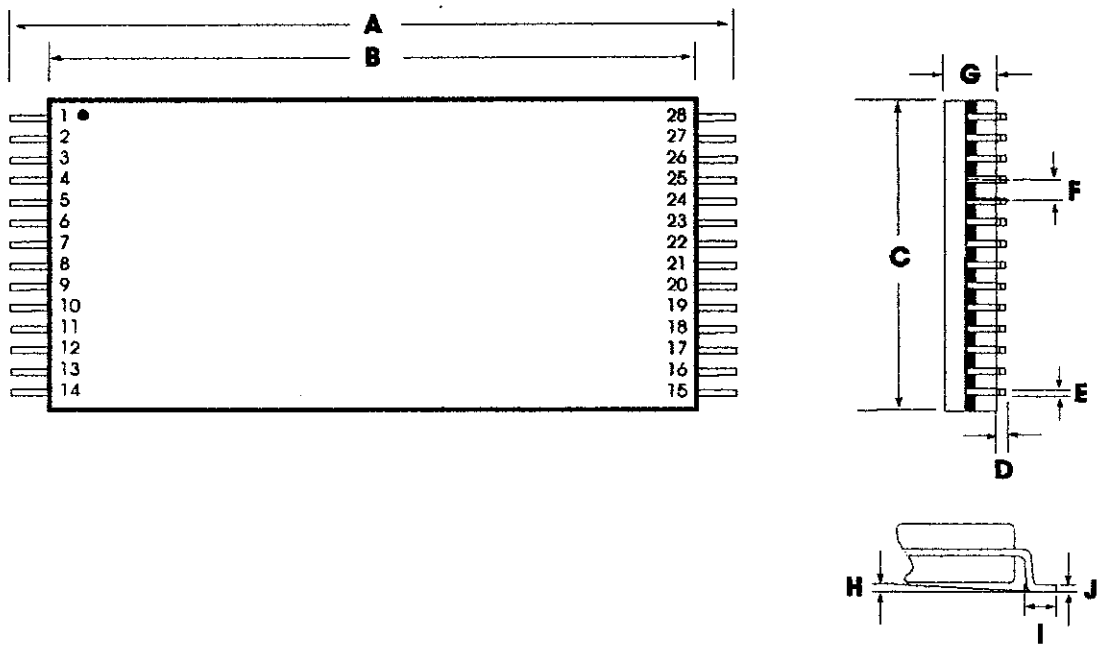


Table 17: Plastic Thin Small Outline Package (TSOP) Type I (E) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	6°	0°	3°	6°
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

NOTE: *Lead coplanarity to be within 0.004 inches.*

Figure 10: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

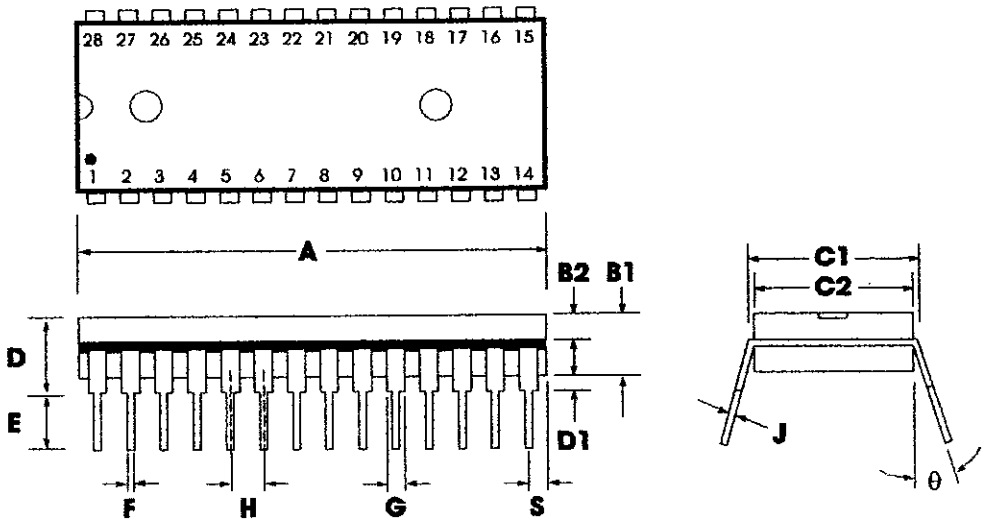


Table 18: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

NOTE: *Lead coplanarity to be within 0.004 inches.*

Figure 11: 32-Lead 8x20mm Plastic Thin Small Outline Package (TSOP) Type I (T)

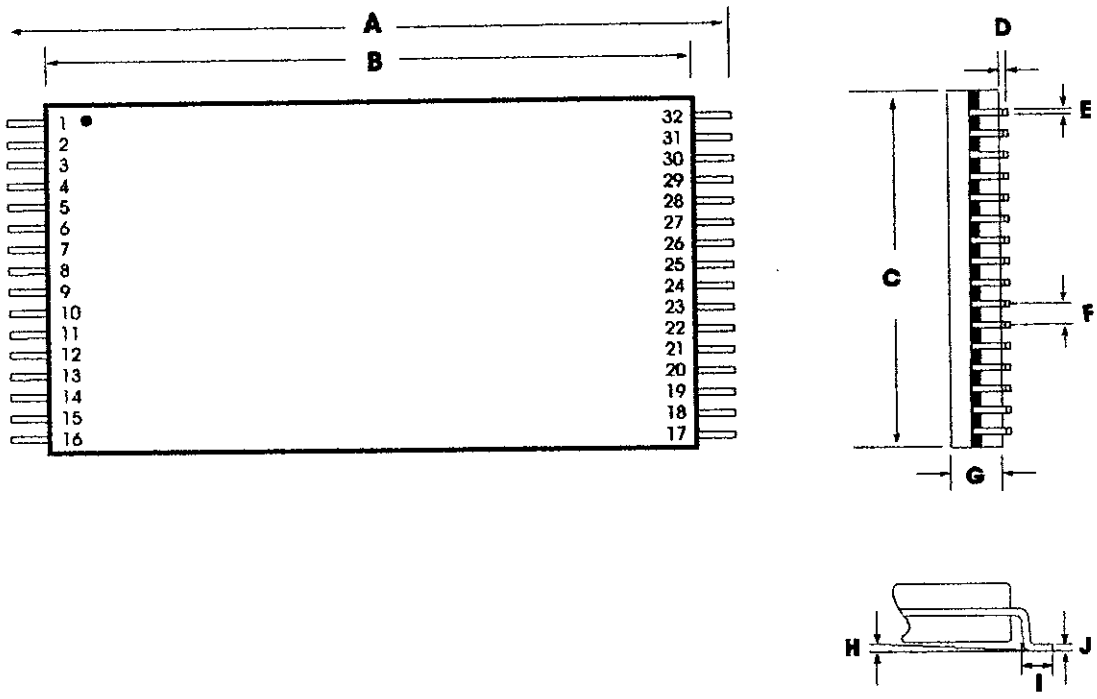


Table 19: Plastic Thin Small Outline Package (TSOP) Type I (T) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min		Max
A	0.780	0.787	0.795	19.80	20.00	20.20
B	0.720	0.724	0.728	18.30	18.40	18.50
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.006	0.009	0.011	0.17	0.22	0.27
F		0.0197			0.50	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	5°	0°	3°	5°
I	0.020	0.024	0.028	0.50	0.60	0.70
J	0.004		0.008	0.10		0.21

NOTE: *Lead coplanarity to be within 0.002 inches.*

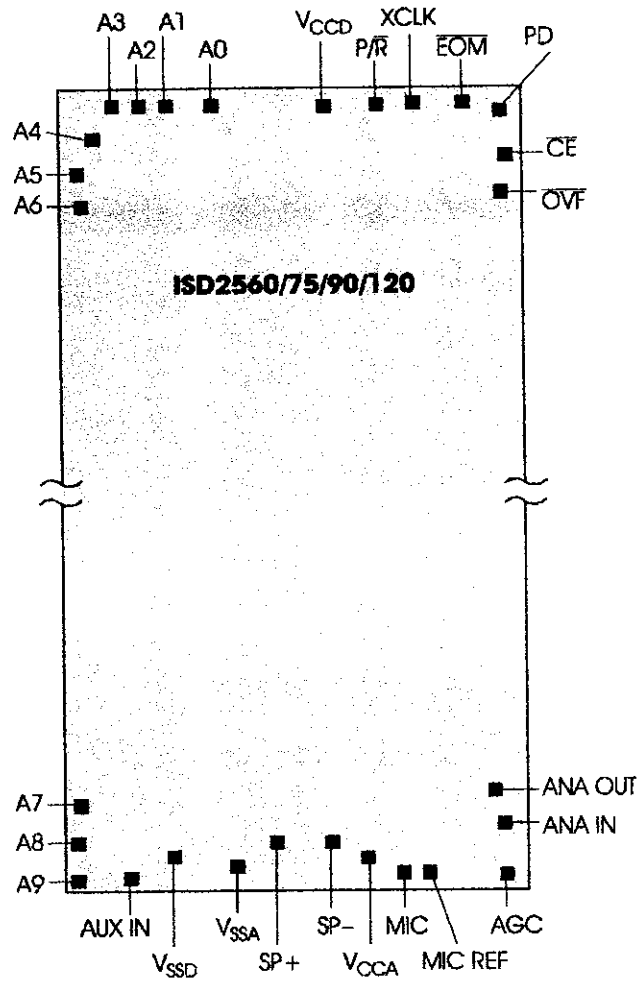
Figure 12: ISD2560/75/90/120 Products *Current* Bonding Physical Layout[1] (Unpackaged Die)

ISD2560/75/90/12[2]

I. Die Dimensions
X: 187 ±1 mils
Y: 399 ±1 mils

II. Die Thickness[2]
17.5 ±1 mils

III. Pad Opening
109 x 109 microns
4.3 x 4.3 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status.*

Table 20: ISD2560/75/90/120 Products *Current* PIN/PAD Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-1148.9	4898.2
A1	Address 1	-1406.9	4898.2
A2	Address 2	-1661.9	4898.2
A3	Address 3	-1916.9	4898.2
A4	Address 4	-2069.9	4608.2
A5	Address 5	-2194.9	4358.2
A6	Address 6	-2194.9	4108.2
A7	Address 7	-2194.9	-4212.3
A8	Address 8	-2194.9	-4456.3
A9	Address 9	-2076.4	-4897.3
AUX IN	Auxiliary Input	-1607.9	-4868.3
V_{SSD}	V_{SS} Digital Power Supply	-1343.9	-4850.8
V_{SSA}	V_{SS} Analog Power Supply	-551.9	-4884.8
SP+	Speaker Output +	-111.4	-4790.8
SP-	Speaker Output -	425.6	-4790.8
V_{CCA}	V_{CC} Analog Power Supply	865.1	-4848.32
MIC	Microphone Input	1320.7	-4897.3
MIC REF	Microphone Reference	1605.1	-4897.3
AGC	Automatic Gain Control	1877.6	-4871.3
ANA IN	Analog Input	2202.11	-4269.8
ANA OUT	Analog Output	2123.1	-3910.8
$\overline{OVF}$	Overflow Output	2142.6	4154.7
$\overline{CE}$	Chip Enable Input	2202.1	4558.7
PD	Power Down Input	2048.1	4898.2
$\overline{EOM}$	End of Message	1648.1	4865.7
XCLK	No Connect (optional)	1221.1	4898.2
P/$\overline{R}$	Playback/Record	965.6	4898.2
V_{CCD}	V_{CC} Digital Power Supply	646.1	4895.7

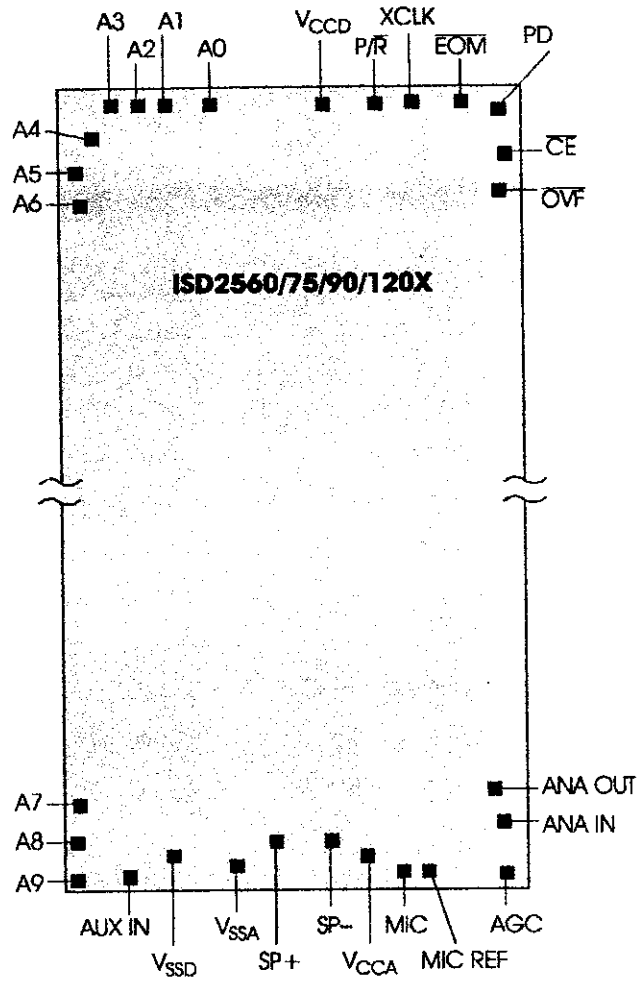
Figure 13: ISD2560/75/90/120 Products *Future* Bonding Physical Layout[1] (Unpackaged Die)

ISD2560/75/90/120X[2]

I. Die Dimensions
X: 149.5 ±1 mils
Y: 262.0 ±1 mils

II. Die Thickness[2]
11.8 ±.4 mils

III. Pad Opening
111 x 111 microns
4.4 x 4.4 mils



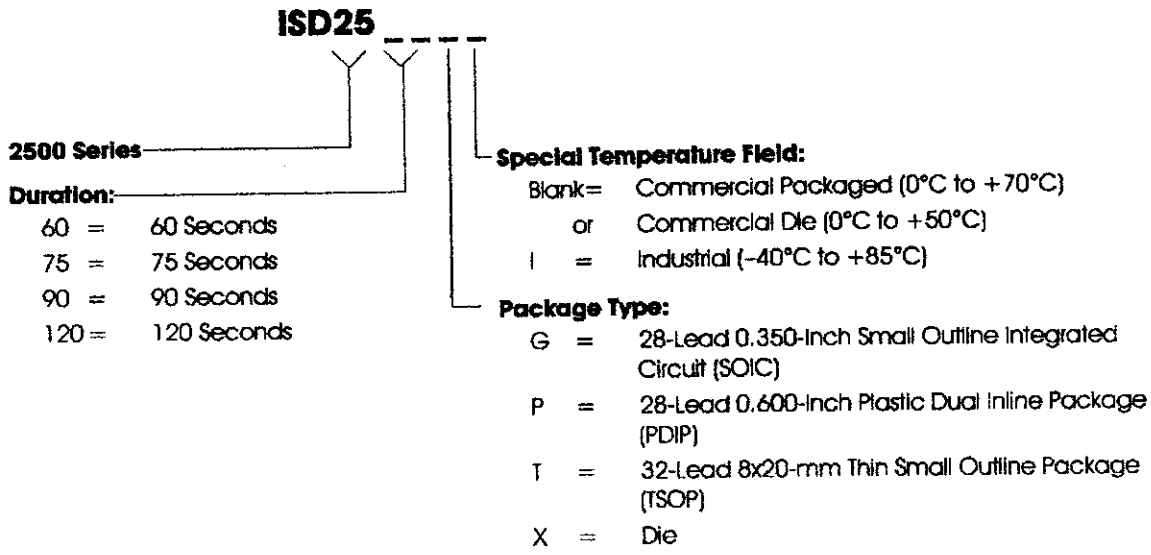
1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status and availability.*

Table 21: ISD2560/75/90/120 Products *Future* PIN/PAD Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
A0	Address 0	–897.9	3135.2
A1	Address 1	–1115.4	3135.2
A2	Address 2	–1331.0	3135.2
A3	Address 3	–1544.0	3135.2
A4	Address 4	–1640.4	2888.9
A5	Address 5	–1698.2	2671.0
A6	Address 6	–1698.2	2441.5
A7	Address 7	–1731.2	–2583.2
A8	Address 8	–1731.2	–2768.4
A9	Address 9	–1731.2	–3050.8
AUX IN	Auxiliary Input	–1410.1	–3115.7
V_{SSD}	V_{SS} Digital Power Supply	–1112.8	–3096.2
V_{SSA}	V_{SS} Analog Power Supply	–407.8	–3138.5
SP+	Speaker Output +	–47.4	–3067.7
SP–	Speaker Output –	386.9	–3067.7
V_{CCA}	V_{CC} Analog Power Supply	746.5	–3110.4
MIC	Microphone Input	1101.2	–3146.0
MIC REF	Microphone Reference	1294.7	–3146.0
AGC	Automatic Gain Control	1666.4	–3130.3
ANA IN	Analog Input	1728.6	–2654.0
ANA OUT	Analog Output	1700.9	–2411.0
$\overline{OVF}$	Overflow Output	1340.9	3121.7
$\overline{CE}$	Chip Enable Input	1726.7	2824.4
PD	Power Down Input	1730.5	3094.0
$\overline{EOM}$	End of Message	1340.9	3121.7
XCLK	No Connect (optional)	986.5	3160.7
P/$\overline{R}$	Playback/Record	807.2	3163.4
V_{CCD}	V_{CC} Digital Power Supply	544.7	3159.2

ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD2560/75/90/120 products, please refer to the following valid part numbers.

Part Number	Part Number	Part Number	Part Number
ISD2560G	ISD2575G	ISD2590G	ISD25120G
ISD2560GI	ISD2575GI	ISD2590P	ISD25120P
ISD2560P	ISD2575P	ISD2590T	ISD25120X
ISD2560PI	ISD2575PI	ISD2590X	
ISD2560T	ISD2575T		
ISD2560TI	ISD2575TI		
ISD2560X	ISD2575X		

For the latest product information, access ISD's worldwide website at http://www.isd.com.

MT8888C

Integrated DTMF Transceiver with Intel Micro Interface

ISSUE 6 March 1997

Features

- Central office quality DTMF transmitter/receiver
- Low power consumption
- High speed Intel micro interface
- Adjustable guard time
- Automatic tone burst mode
- Call progress tone detection to -30dBm

Applications

- Credit card systems
- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- Personal computers

Ordering Information

MT8888CE	20 Pin Plastic DIP
MT8888CS	20 Pin SOIC
MT8888CN	24 Pin SSOP

-40°C to +85°C

Description

The MT8888C is a monolithic DTMF transceiver with call progress filter. It is fabricated in CMOS technology offering low power consumption and high reliability.

The receiver section is based upon the industry standard MT8870 DTMF receiver while the transmitter utilizes a switched capacitor D/A converter for low distortion, high accuracy DTMF signalling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones.

The MT8888C utilizes an Intel micro interface, which allows the device to be connected to a number of popular microcontrollers with minimal external logic.

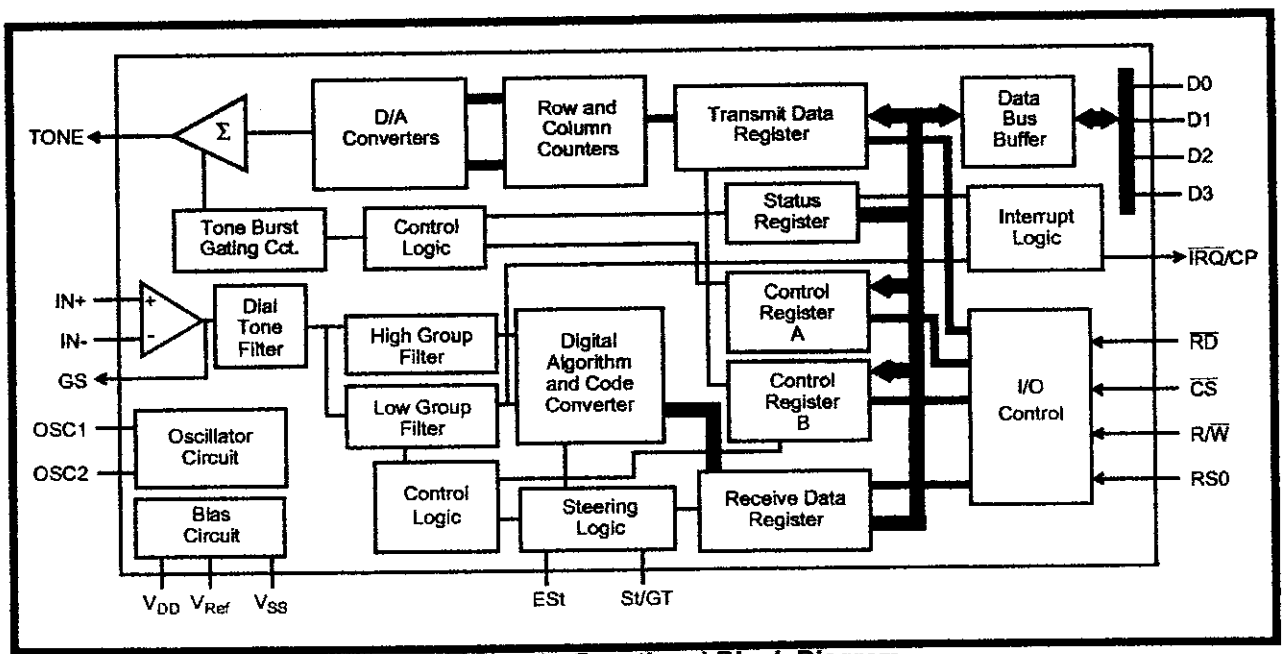


Figure 1 - Functional Block Diagram

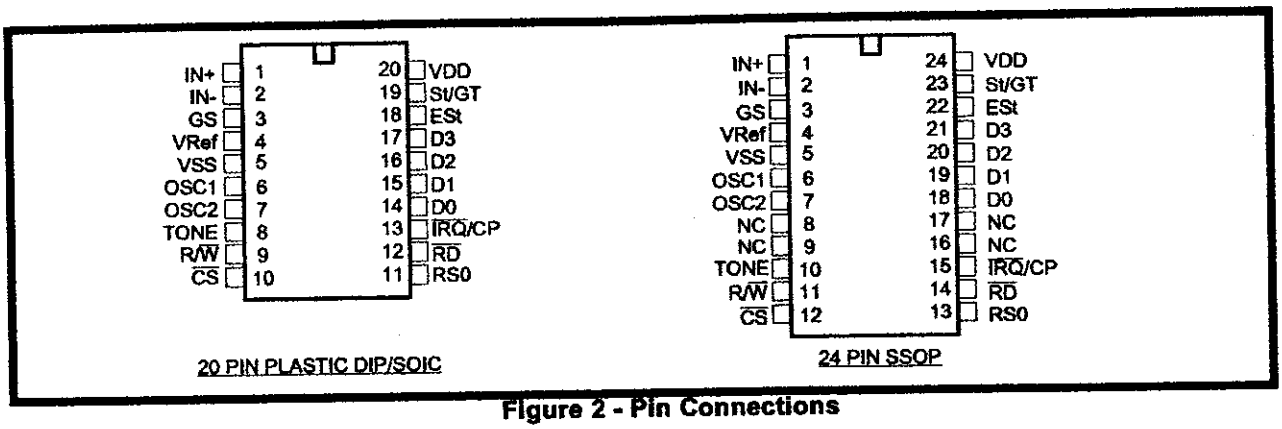


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
20	24		
1	1	IN+	**Non-inverting** op-amp input.
2	2	IN-	**Inverting** op-amp input.
3	3	GS	**Gain Select**. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V_{Ref}	**Reference Voltage** output ($V_{DD}/2$).
5	5	V_{SS}	Ground (0V).
6	6	OSC1	**Oscillator** input. This pin can also be driven directly by an external clock.
7	7	OSC2	**Oscillator** output. A 3.579545 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit. Leave open circuit when OSC1 is driven externally.
8	10	TONE	Output from internal DTMF transmitter.
9	11	$\overline{WR}$	**Write** microprocessor input. TTL compatible.
10	12	$\overline{CS}$	**Chip Select** input. Active Low. This signal must be qualified externally by address latch enable (ALE) signal, see Figure 12.
11	13	RS0	**Register Select** input. Refer to Table 3 for bit interpretation. TTL compatible.
12	14	$\overline{RD}$	**Read** microprocessor input. TTL compatible.
13	15	$\overline{IRQ}$/ CP	**Interrupt Request/Call Progress** (open drain) output. In interrupt mode, this output goes low when a valid DTMF tone burst has been transmitted or received. In call progress mode, this pin will output a rectangular signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter, see Figure 8.
14-17	18-21	D0-D3	Microprocessor Data Bus. High impedance when $\overline{CS}$ = 1 or $\overline{RD}$ = 1. TTL compatible.
18	22	ESt	**Early Steering** output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	23	St/GT	**Steering Input/Guard Time** output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
20	24	V_{DD}	Positive power supply (5V typ.).
	8,9 16,17	NC	No Connection.

Functional Description

The MT8888C Integrated DTMF Transceiver consists of a high performance DTMF receiver with an internal gain setting amplifier and a DTMF generator which employs a burst counter to synthesize precise tone bursts and pauses. A call progress mode can be selected so that frequencies within the specified passband can be detected. The Intel micro interface allows microcontrollers, such as the 8080, 80C31/51 and 8085, to access the MT8888C internal registers.

Input Configuration

The input arrangement of the MT8888C provides a differential-input operational amplifier as well as a bias source (V_{Ref}), which is used to bias the inputs at $V_{DD}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for gain adjustment. In a single-ended configuration, the input pins are connected as shown in Figure 3.

Figure 4 shows the necessary connections for a differential input configuration.

Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies (see Table 1). These filters incorporate notches at 350 Hz and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order switched capacitor filter section, which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

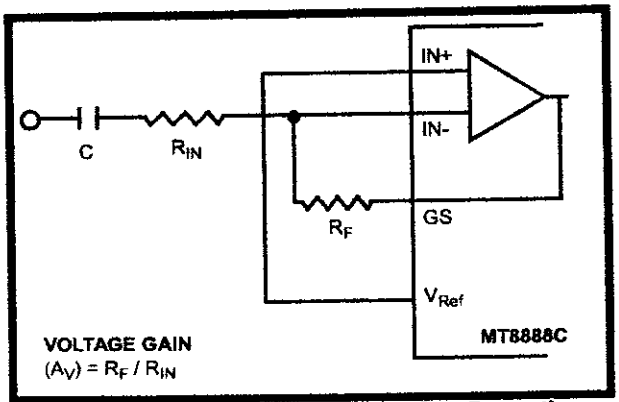


Figure 3 - Single-Ended Input Configuration

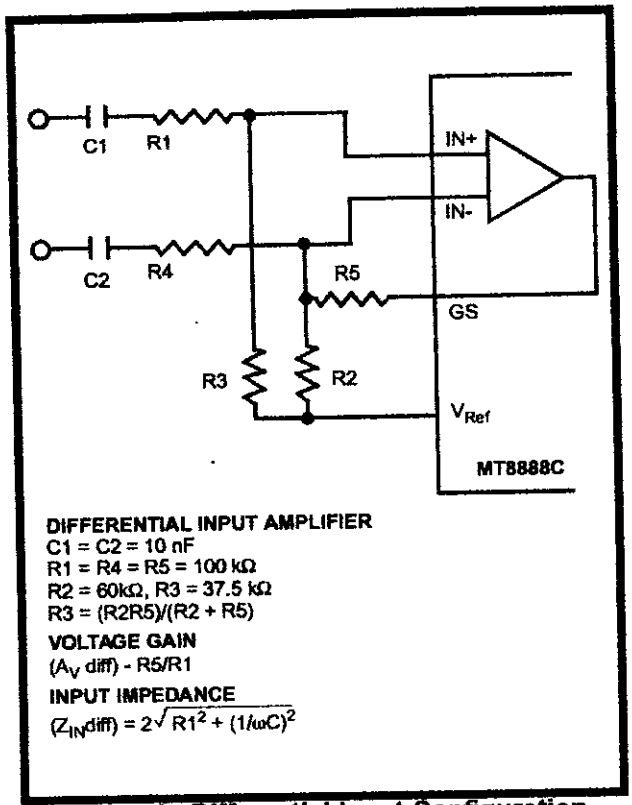


Figure 4 - Differential Input Configuration

F_{LOW}	F_{HIGH}	DIGIT	D_3	D_2	D_1	D_0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0= LOGIC LOW, 1= LOGIC HIGH

Table 1. Functional Encode/Decode Table

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 5) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the Receive Data Register. At this point the GT output is activated and drives v_c to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signalling that a received tone pair has been registered. The status of the delayed steering flag can be monitored by checking the appropriate bit in the status register. If Interrupt mode has been selected, the $\overline{IRQ}$/CP pin will pull low when the delayed steering flag is active.

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the four bit bidirectional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

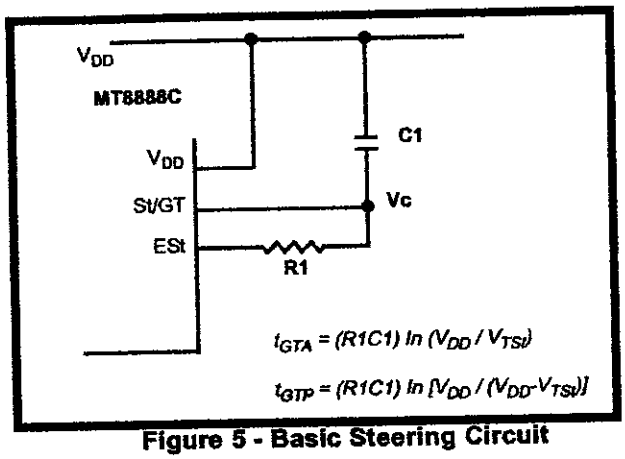


Figure 5 - Basic Steering Circuit

Guard Time Adjustment

The simple steering circuit shown in Figure 5 is adequate for most applications. Component values are chosen according to the following inequalities (see Figure 7):

$$t_{REC} \geq t_{DPmax} + t_{GTPmax} - t_{DAmin}$$
$$t_{\overline{REC}} \leq t_{DPmin} + t_{GTPmin} - t_{DAmax}$$
$$t_{ID} \geq t_{DAmax} + t_{GTAmax} - t_{DPmin}$$
$$t_{DO} \leq t_{DAmin} + t_{GTAmin} - t_{DPmax}$$

The value of t_{DP} is a device parameter (see AC Electrical Characteristics) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C1 of 0.1 µF is recommended for most

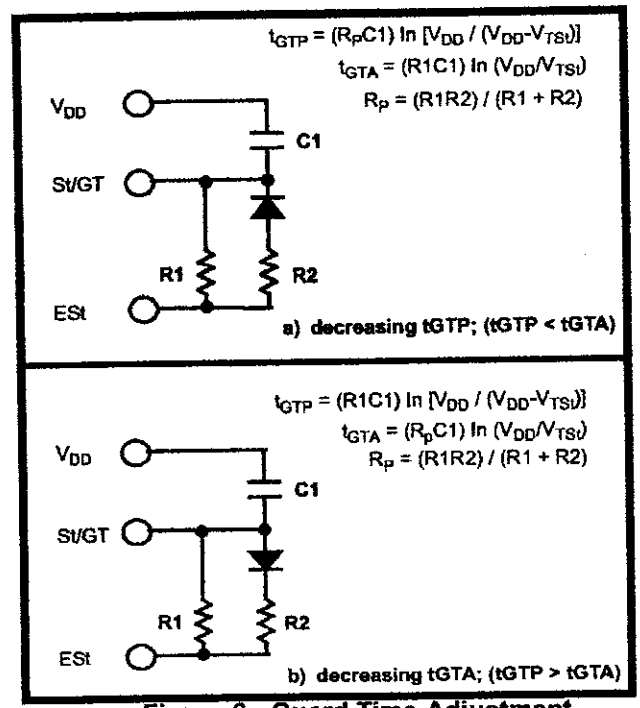


Figure 6 - Guard Time Adjustment

applications, leaving R1 to be selected by the designer. Different steering arrangements may be used to select independent tone present (t_{GTP}) and tone absent (t_{GTA}) guard times. This may be necessary to meet system specifications which place both accept and reject limits on tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity.

Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain a valid signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 6. The receiver timing is shown in Figure 7 with a description of the events in Figure 9.

Call Progress Filter

A call progress mode, using the MT8888C, can be selected allowing the detection of various tones, which identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common, however, call progress tones can only be detected when CP mode has been selected. DTMF signals cannot be detected if CP mode has been selected (see Table 7). Figure 8 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input, which are within the 'accept' bandwidth limits of the filter, are hard-limited by a high gain comparator with the $\overline{IRQ}$/CP pin serving as the output. The squarewave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies which are in the 'reject' area will not be detected and consequently the $\overline{IRQ}$/CP pin will remain low.

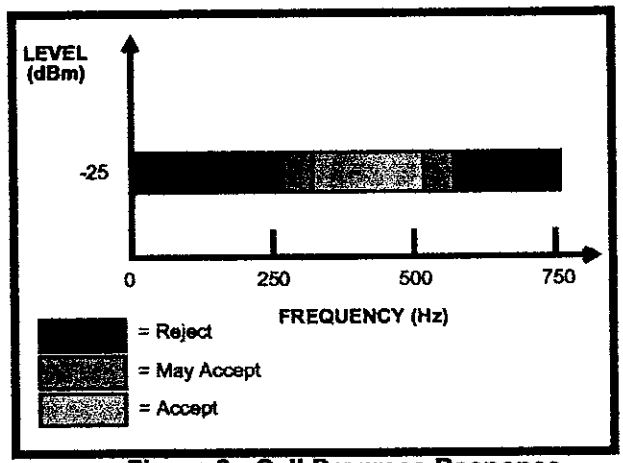


Figure 8 - Call Progress Response

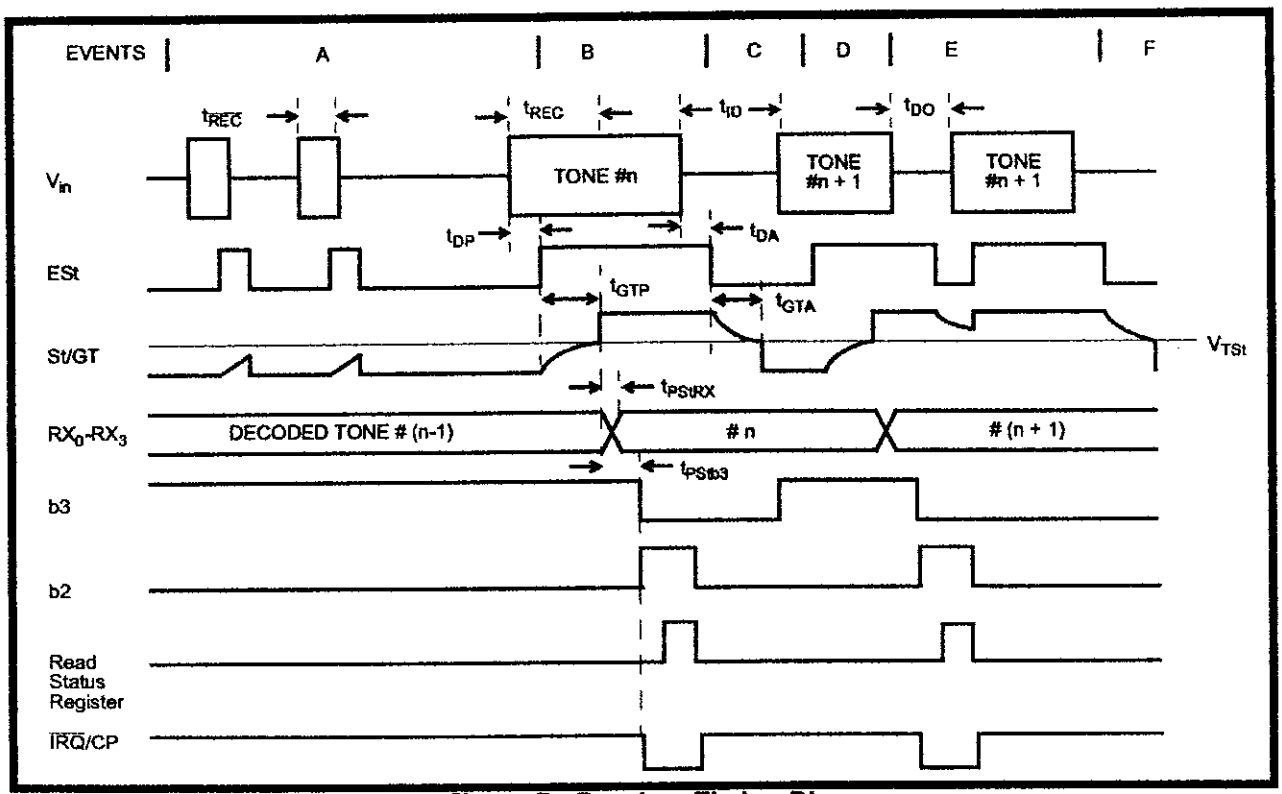


Figure 7 - Receiver Timing Diagram

EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, RX DATA REGISTER NOT UPDATED.
B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.
D) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
E) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, DATA REMAINS UNCHANGED.
F) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
RX_0-RX_3	4-BIT DECODED DATA IN RECEIVE DATA REGISTER
b3	DELAYED STEERING. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL. ACTIVE LOW FOR THE DURATION OF A VALID DTMF SIGNAL.
b2	INDICATES THAT VALID DATA IS IN THE RECEIVE DATA REGISTER. THE BIT IS CLEARED AFTER THE STATUS REGISTER IS READ.
$\overline{IRQ}$/CP	INTERRUPT IS ACTIVE INDICATING THAT NEW DATA IS IN THE RX DATA REGISTER. THE INTERRUPT IS CLEARED AFTER THE STATUS REGISTER IS READ.
t_{REC}	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
$t_{\overline{REC}}$	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Figure 9 - Description of Timing Events

DTMF Generator

The DTMF transmitter employed in the MT8888C is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.579545 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Table 1 must be written to the transmit Data Register. Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as Low Group and High Group tones. As seen from the table, the low group frequencies are 697, 770, 852 and 941 Hz. The high group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically, the high group to low group amplitude ratio (twist) is 2 dB to com-pensate for high group attenuation on long loops.

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the Transmit Data Register the 4 bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify a time segment length, which will ultimately determine the frequency of the tone. When the divider reaches the appropriate count, as determined by the input code, a reset pulse is issued and the counter starts again. The number of time segments is fixed at 32, however, by varying the segment length as described above the frequency can also be varied. The divider output clocks another counter, which addresses the sinewave lookup ROM.

The lookup table contains codes which are used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are employed to produce row and column tones, which are then mixed using a low noise summing amplifier. The oscillator described needs no "start-up" time as in other DTMF generators since the crystal oscillator is running continuously thus providing a high degree of tone burst accuracy. A bandwidth limiting filter is incorporated and serves to attenuate distortion products above 8 kHz. It can be seen from Figure 8 that the distortion products are very low in amplitude.

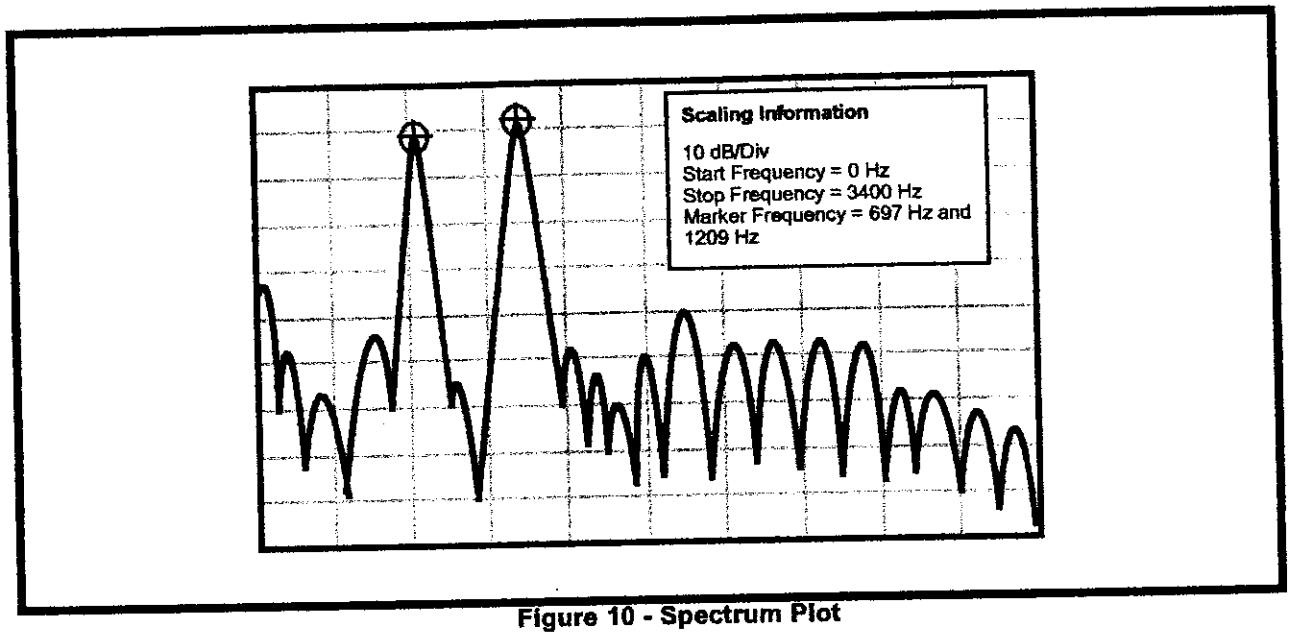


Figure 10 - Spectrum Plot

Burst Mode

In certain telephony applications it is required that DTMF signals being generated are of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms±1 ms, which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register indicating that the transmitter is ready for more data. The timing described above is available when DTMF mode has been selected. However, when CP mode (Call Progress mode) is selected, the burst/pause duration is doubled to 102 ms ±2 ms. Note that when CP mode and Burst mode have been selected, DTMF tones may be transmitted only and *not* received. In applications where a non-standard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

Single Tone Generation

A single tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgment tone generation and distortion measurements. Refer to Control Register B description for details.

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		%ERROR
	SPECIFIED	ACTUAL	
L1	697	699.1	+0.30
L2	770	766.2	-0.49
L3	852	847.4	-0.54
L4	941	948.0	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	-0.32
H3	1477	1471.9	-0.35
H4	1633	1645.0	+0.73

Table 2. Actual Frequencies Versus Standard Requirements

Distortion Calculations

The MT8888C is capable of producing precise tone bursts with minimal error in frequency (see Table 2). The internal summing amplifier is followed by a first-order lowpass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single tone* can be calculated using Equation 1, which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage.

$$\text{THD (\%)} = 100 \frac{\left(\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + \ldots V^2_{nf}}\right)}{V_{fundamental}}$$

Equation 1. THD (%) For a Single Tone

The Fourier components of the tone output correspond to V_{2f}.... V_{nf} as measured on the output waveform. The total harmonic distortion for a *dual tone* can be calculated using Equation 2. V_L and V_H correspond to the low group amplitude and high group amplitude, respectively and V^2_{IMD} is the sum of all the intermodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 10.

$$THD\ (\%) = 100 \frac{\left(\sqrt{V^2_{2L} + V^2_{3L} + ... V^2_{nL} + V^2_{2H} + V^2_{3H} + .. V^2_{nH} + V^2_{IMD}}\right)}{\sqrt{V^2_L + V^2_H}}$$

Equation 2. THD (%) For a Dual Tone

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television colour burst crystal. The crystal specification is as follows:

Frequency:	3.579545 MHz
Frequency Tolerance:	±0.1%
Resonance Mode:	Parallel
Load Capacitance:	18pF
Maximum Series Resistance:	150 ohms
Maximum Drive Level:	2mW

e.g. CTS Knights MP036S
Toyocom TQC-203-A-9S

A number of MT8888C devices can be connected as shown in Figure 11 such that only one crystal is required. Alternatively, the OSC1 inputs on all devices can be driven from a TTL buffer with the OSC2 outputs left unconnected.

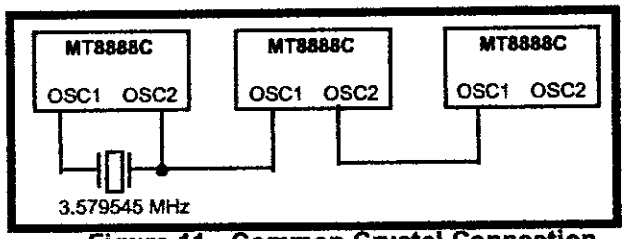


Figure 11 - Common Crystal Connection

Microprocessor Interface

The MT8888C incorporates an Intel microprocessor interface which is compatible with fast versions (16 MHz) of the 80C51. No wait cycles need to be inserted.

Figures 17 and 18 are the timing diagrams for the Intel 8031, 8051 and 8085 (5 MHz) microcontrollers. By NANDing the address latch enable (ALE) output with the high-byte address (P2) decode output, $\overline{CS}$ is generated. Figure 12 summarizes the connection of these Intel processors to the MT8888C transceiver.

The microprocessor interface provides access to five internal registers. The read-only Receive Data Register contains the decoded output of the last valid DTMF digit received. Data entered into the write-only Transmit Data Register will determine which tone pair is to be generated (see Table 1 for coding details). Transceiver control is accomplished with two control registers (see Tables 6 and 7), CRA and CRB, which have the same address. A write operation to CRB is executed by first setting the most significant bit (b3) in CRA. The following write operation to the same address will then be directed to CRB, and subsequent write cycles will be directed back to CRA. The read-only status register indicates the current transceiver state (see Table 8).

A software reset must be included at the beginning of all programs to initialize the control registers upon power-up or power reset (see Figure 17). Refer to Tables 4-7 for bit descriptions of the two control registers.

The multiplexed $\overline{IRQ}$/CP pin can be programmed to generate an interrupt upon validation of DTMF signals or when the transmitter is ready for more data (burst mode only). Alternatively, this pin can be configured to provide a squarewave output of the call progress signal. The $\overline{IRQ}$/CP pin is an open drain output and requires an external pull-up resistor (see Figure 13).

RS0	$\overline{WR}$	$\overline{RD}$	FUNCTION
0	0	1	Write to Transmit Data Register
0	1	0	Read from Receive Data Register
1	0	1	Write to Control Register
1	1	0	Read from Status Register

Table 3. Internal Register Functions

b3	b2	b1	b0
RSEL	IRQ	CP/DTMF	TOUT

Table 4. CRA Bit Positions

b3	b2	b1	b0
C/R	S/D	TEST	BURST $\overline{ENABLE}$

Table 5. CRB Bit Positions

BIT	NAME	DESCRIPTION
b0	TOUT	Tone Output Control. A logic high enables the tone output; a logic low turns the tone output off. This bit controls all transmit tone functions.
b1	CP/$\overline{\text{DTMF}}$	Call Progress or DTMF Mode Select. A logic high enables the receive call progress mode; a logic low enables DTMF mode. In DTMF mode the device is capable of receiving and transmitting DTMF signals. In CP mode a rectangular wave representation of the received tone signal will be present on the $\overline{\text{IRQ}}$/CP output pin if IRQ has been enabled (control register A, b2=1). In order to be detected, CP signals must be within the bandwidth specified in the AC Electrical Characteristics for Call Progress. Note: DTMF signals cannot be detected when CP mode is selected.
b2	IRQ	Interrupt Enable. A logic high enables the interrupt function; a logic low de-activates the interrupt function. When IRQ is enabled and DTMF mode is selected (control register A, b1=0), the $\overline{\text{IRQ}}$/CP output pin will go low when either 1) a valid DTMF signal has been received for a valid guard time duration, or 2) the transmitter is ready for more data (burst mode only).
b3	RSEL	Register Select. A logic high selects control register B for the next write cycle to the control register address. After writing to control register B, the following control register write cycle will be directed to control register A.

Table 6. Control Register A Description

BIT	NAME	DESCRIPTION
b0	$\overline{\text{BURST}}$	Burst Mode Select. A logic high de-activates burst mode; a logic low enables burst mode. When activated, the digital code representing a DTMF signal (see Table 1) can be written to the transmit register, which will result in a transmit DTMF tone burst and pause of equal durations (typically 51 msec.). Following the pause, the status register will be updated (b1 - Transmit Data Register Empty), and an interrupt will occur if the interrupt mode has been enabled. When CP mode (control register A, b1) is enabled the normal tone burst and pause durations are extended from a typical duration of 51 msec to 102 msec. When $\overline{\text{BURST}}$ is high (de-activated) the transmit tone burst duration is determined by the TOUT bit (control register A, b0).
b1	TEST	Test Mode Control. A logic high enables the test mode; a logic low de-activates the test mode. When TEST is enabled and DTMF mode is selected (control register A, b1=0), the signal present on the $\overline{\text{IRQ}}$/CP pin will be analogous to the state of the DELAYED STEERING bit of the status register (see Figure 7, signal b3).
b2	S/$\overline{\text{D}}$	Single or Dual Tone Generation. A logic high selects the single tone output; a logic low selects the dual tone (DTMF) output. The single tone generation function requires further selection of either the row or column tones (low or high group) through the C/$\overline{\text{R}}$ bit (control register B, b3).
b3	C/$\overline{\text{R}}$	Column or Row Tone Select. A logic high selects a column tone output; a logic low selects a row tone output. This function is used in conjunction with the S/$\overline{\text{D}}$ bit (control register B, b2).

Table 7. Control Register B Description

BIT	NAME	STATUS FLAG SET	STATUS FLAG CLEARED
b0	IRQ	Interrupt has occurred. Bit one (b1) or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	TRANSMIT DATA REGISTER EMPTY (BURST MODE ONLY)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in non-burst mode.
b2	RECEIVE DATA REGISTER FULL	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	$\overline{\text{DELAYED STEERING}}$	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

Table 8. Status Register Description

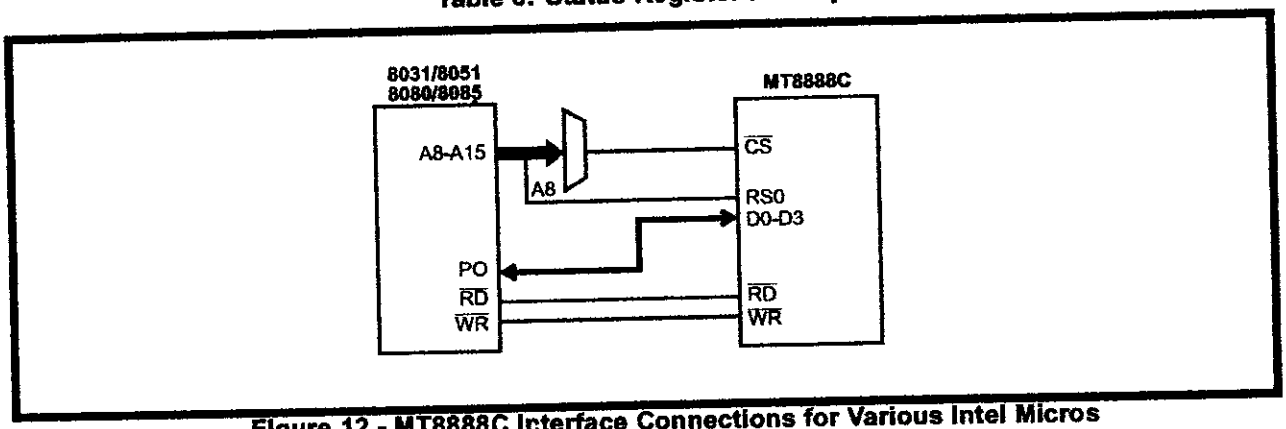
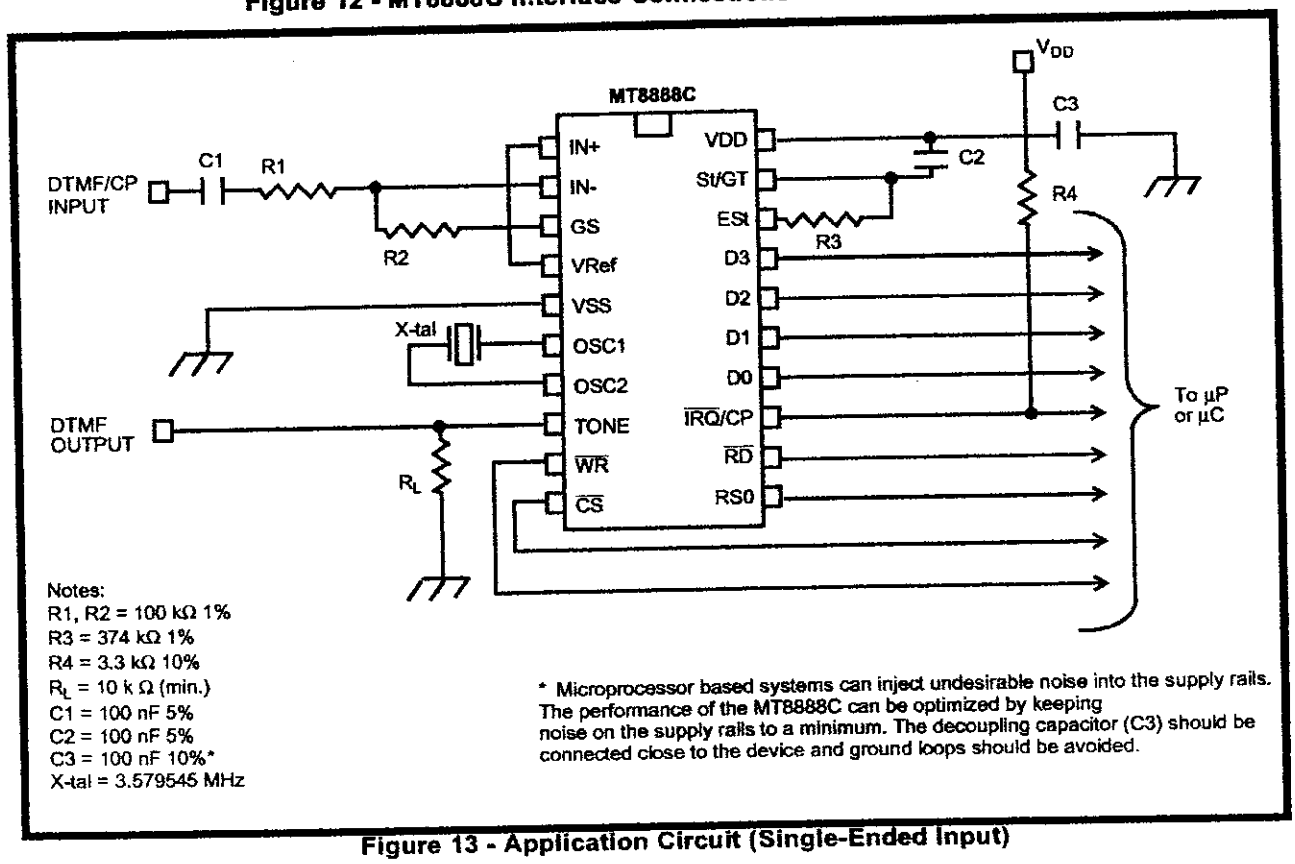


Figure 12 - MT8888C Interface Connections for Various Intel Micros



Notes:
R1, R2 = 100 kΩ 1%
R3 = 374 kΩ 1%
R4 = 3.3 kΩ 10%
R_L = 10 k Ω (min.)
C1 = 100 nF 5%
C2 = 100 nF 5%
C3 = 100 nF 10%*
X-tal = 3.579545 MHz

* Microprocessor based systems can inject undesirable noise into the supply rails. The performance of the MT8888C can be optimized by keeping noise on the supply rails to a minimum. The decoupling capacitor (C3) should be connected close to the device and ground loops should be avoided.

Figure 13 - Application Circuit (Single-Ended Input)

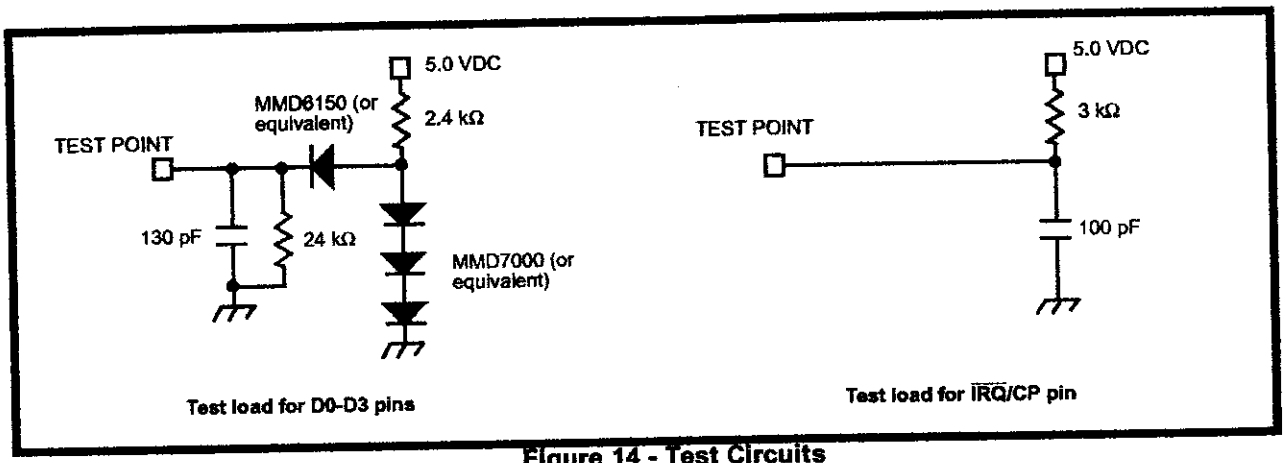


Figure 14 - Test Circuits

INITIALIZATION PROCEDURE

A software reset must be included at the beginning of all programs to initialize the control registers after power up. The initialization procedure should be implemented 100ms after power up.

Description:	**Control**			**Data**			
	RS0	**$\overline{WR}$**	**$\overline{RD}$**	**b3**	**b2**	**b1**	**b0**
1) Read Status Register	1	1	0	X	X	X	X
2) Write to Control Register	1	0	1	0	0	0	0
3) Write to Control Register	1	0	1	0	0	0	0
4) Write to Control Register	1	0	1	1	0	0	0
5) Write to Control Register	1	0	1	0	0	0	0
6) Read Status Register	1	1	0	X	X	X	X

TYPICAL CONTROL SEQUENCE FOR BURST MODE APPLICATIONS

Transmit DTMF tones of 50 ms burst/50 ms pause and Receive DTMF Tones.

Sequence:	**RS0**	**$\overline{WR}$**	**$\overline{RD}$**	**b3**	**b2**	**b1**	**b0**
1) Write to Control Register A (tone out, DTMF, $\overline{IRQ}$, Select Control Register B)	1	0	1	1	1	0	1
2) Write to Control Register B (burst mode)	1	0	1	0	0	0	0
3) Write to Transmit Data Register (send a digit 7)	0	0	1	0	1	1	1
4) Wait for an interrupt or poll Status Register							
5) Read the Status Register	1	1	0	X	X	X	X
-if bit 1 is set, the Tx is ready for the next tone, in which case... Write to Transmit Register (send a digit 5)	0	0	1	0	1	0	1
-if bit 2 is set, a DTMF tone has been received, in which case.... Read the Receive Data Register	0	1	0	X	X	X	X
-if both bits are set...							
Read the Receive Data Register	0	1	0	X	X	X	X
Write to Transmit Data Register	0	0	1	0	1	0	1

NOTE: IN THE TX BURST MODE, STATUS REGISTER BIT 1 WILL NOT BE SET UNTIL 100 ms (±2 ms) AFTER THE DATA IS WRITTEN TO THE TX DATA REGISTER. IN EXTENDED BURST MODE THIS TIME WILL BE DOUBLED TO 200 ms (± 4 ms).

Figure 15 - Application Notes

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}	V_{DD}		6	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (Except V_{DD} and V_{SS})			10	mA
4	Storage temperature	T_{ST}	-65	+150	°C
5	Package power dissipation	P_D		1000	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive power supply	V_{DD}	4.75	5.00	5.25	V	
2	Operating temperature	T_O	-40		+85	°C	
3	Crystal clock frequency	f_{CLK}	3.575965	3.579545	3.583124	MHz	

‡ Typical figures are at 25 °C and for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - V_{SS}=0 V.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUP	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		7.0	11	mA	
3		Power consumption	P_C			57.8	mW	
4	INPUTS	High level input voltage (OSC1)	V_{IHO}	3.5			V	Note 9*
5		Low level input voltage (OSC1)	V_{ILO}			1.5	V	Note 9*
6		Steering threshold voltage	V_{TSt}	2.2	2.3	2.5	V	V_{DD}=5V
7	OUTPUTS	Low level output voltage (OSC2)	V_{OLO}			0.1	V	No load Note 9*
8		High level output voltage (OSC2)	V_{OHO}	4.9			V	No load Note 9*
9		Output leakage current (IRQ)	I_{OZ}		1	10	µA	V_{OH}=2.4 V
10		V_{Ref} output voltage	V_{Ref}	2.4	2.5	2.6	V	No load, V_{DD}=5V
11		V_{Ref} output resistance	R_{OR}		1.3		kΩ	
12	Digital	Low level input voltage	V_{IL}			0.8	V	
13		High level input voltage	V_{IH}	2.0			V	
14		Input leakage current	I_{IZ}			10	µA	V_{IN}=V_{SS} to V_{DD}
15	Data Bus	Source current	I_{OH}	-1.4	-6.6		mA	V_{OH}=2.4V
16		Sink current	I_{OL}	2.0	4.0		mA	V_{OL}=0.4V
17	ESt and St/Gt	Source current	I_{OH}	-0.5	-3.0		mA	V_{OH}=4.6V
18		Sink current	I_{OL}	2	4		mA	V_{OL}=0.4V
19	$\overline{IRQ}$/CP	Sink current	I_{OL}	4	16		mA	V_{OL}=0.4V

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25 °C, V_{DD} =5V and for design aid only: not guaranteed and not subject to production testing.
* See "Notes" following AC Electrical Characteristics Tables.

Electrical Characteristics

Gain Setting Amplifier - Voltages are with respect to ground (V_{SS}) unless otherwise stated, V_{SS}= 0V.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	
6	DC open loop voltage gain	A_{VOL}	40			dB	C_L = 20p
7	Unity gain bandwidth	BW	1.0			MHz	C_L = 20p
8	Output voltage swing	V_O	0.5		V_{DD}-0.5	V	$R_L \ge 100$ kΩ to V_{SS}
9	Allowable capacitive load (GS)	C_L			100	pF	PM>40°
10	Allowable resistive load (GS)	R_L	50			kΩ	V_O = 4Vpp
11	Common mode range	V_{CM}	1.0		V_{DD}-1.0	V	R_L = 50kΩ

Figures are for design aid only: not guaranteed and not subject to production testing.
Characteristics are over recommended operating conditions unless otherwise stated.

MT8888C AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	RX	Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,5,6
				27.5		869	mV_{RMS}	1,2,3,5,6

† Characteristics are over recommended operating conditions (unless otherwise stated) using the test circuit shown in Figure 13.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. f_C=3.579545 MHz

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	RX	Positive twist accept				8	dB	2,3,6,9
2		Negative twist accept				8	dB	2,3,6,9
3		Freq. deviation accept		±1.5%± 2Hz				2,3,5
4		Freq. deviation reject		±3.5%				2,3,5
5		Third tone tolerance			-16		dB	2,3,4,5,9,10
6		Noise tolerance			-12		dB	2,3,4,5,7,9,10
7		Dial tone tolerance			22		dB	2,3,4,5,8,9

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD} = 5V, and for design aid only: not guaranteed and not subject to production testing.
* *See "Notes" following AC Electrical Characteristics Tables.

AC Electrical Characteristics† - Call Progress - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	Accept Bandwidth	f_A	310		500	Hz	@ -25 dBm, Note 9
2	Lower freq. (REJECT)	f_{LR}		290		Hz	@ -25 dBm
3	Upper freq. (REJECT)	f_{HR}		540		Hz	@ -25 dBm
4	Call progress tone detect level (total power)		-30			dBm	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - DTMF Reception - Typical DTMF tone accept and reject requirements. Actual values are user selectable as per Figures 5, 6 and 7.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	Minimum tone accept duration	t_{REC}		40		ms	
2	Maximum tone reject duration	$t_{\overline{REC}}$		20		ms	
3	Minimum interdigit pause duration	t_{ID}		40		ms	
4	Maximum tone drop-out duration	t_{OD}		20		ms	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	TONE IN	Tone present detect time	t_{DP}	3	11	14	ms	Note 11
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 11
3		Delay St to b3	t_{PStb3}		13		µs	See Figure 7
4		Delay St to RX_0-RX_3	t_{PStRX}		8		µs	See Figure 7
5	TONE OUT	Tone burst duration	t_{BST}	50		52	ms	DTMF mode
6		Tone pause duration	t_{PS}	50		52	ms	DTMF mode
7		Tone burst duration (extended)	t_{BSTE}	100		104	ms	Call Progress mode
8		Tone pause duration (extended)	t_{PSE}	100		104	ms	Call Progress mode
9		High group output level	V_{HOUT}	-6.1		-2.1	dBm	R_L=10kΩ
10		Low group output level	V_{LOUT}	-8.1		-4.1	dBm	R_L=10kΩ
11		Pre-emphasis	dB_P	0	2	3	dB	R_L=10kΩ
12		Output distortion (Single Tone)	THD		-35		dB	25 kHz Bandwidth
13								R_L=10kΩ
14		Frequency deviation	f_D		±0.7	±1.5	%	f_C=3.579545 MHz
15		Output load resistance	R_{LT}	10		50	kΩ	
16	XTAL	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
17		Clock input rise and fall time	t_{CLRF}			110	ns	Ext. clock
18		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
19		Capacitive load (OSC2)	C_{LO}			30	pF	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics†- Call Progress - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	Accept Bandwidth	f_A	310		500	Hz	@ -25 dBm, Note 9
2	Lower freq. (REJECT)	f_{LR}		290		Hz	@ -25 dBm
3	Upper freq. (REJECT)	f_{HR}		540		Hz	@ -25 dBm
4	Call progress tone detect level (total power)		-30			dBm	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics†- DTMF Reception - Typical DTMF tone accept and reject requirements. Actual values are user selectable as per Figures 5, 6 and 7.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	Minimum tone accept duration	t_{REC}		40		ms	
2	Maximum tone reject duration	$t_{\overline{REC}}$		20		ms	
3	Minimum interdigit pause duration	t_{ID}		40		ms	
4	Maximum tone drop-out duration	t_{OD}		20		ms	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	TONE IN	Tone present detect time	t_{DP}	3	11	14	ms	Note 11
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 11
3		Delay St to b3	t_{PStb3}		13		µs	See Figure 7
4		Delay St to RX_0-RX_3	t_{PStRX}		8		µs	See Figure 7
5	TONE OUT	Tone burst duration	t_{BST}	50		52	ms	DTMF mode
6		Tone pause duration	t_{PS}	50		52	ms	DTMF mode
7		Tone burst duration (extended)	t_{BSTE}	100		104	ms	Call Progress mode
8		Tone pause duration (extended)	t_{PSE}	100		104	ms	Call Progress mode
9		High group output level	V_{HOUT}	-6.1		-2.1	dBm	R_L=10kΩ
10		Low group output level	V_{LOUT}	-8.1		-4.1	dBm	R_L=10kΩ
11		Pre-emphasis	dB_P	0	2	3	dB	R_l=10kΩ
12		Output distortion (Single Tone)	THD		-35		dB	25 kHz Bandwidth
13								R_L=10kΩ
14		Frequency deviation	f_D		±0.7	±1.5	%	f_C=3.579545 MHz
15		Output load resistance	R_{LT}	10		50	kΩ	
16	XTAL	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
17		Clock input rise and fall time	t_{CLRF}			110	ns	Ext. clock
18		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
19		Capacitive load (OSC2)	C_{LO}			30	pF	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - MPU Interface - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	$\overline{RD}/\overline{WR}$ clock frequency	t_{CYC}		4.0		MHz	Figure 16
2	$\overline{RD}/\overline{WR}$ cycle period	t_{CYC}		250		ns	Figure 16
3	$\overline{RD}/\overline{WR}$ rise and fall time	t_R, t_F			20	ns	Figure 16
4	Address setup time	t_{AS}	23			ns	Figures 17 & 18
5	Address hold time	t_{AH}	26			ns	Figures 17 & 18
6	Data hold time (read)	t_{DHR}	22			ns	Figures 17 & 18
7	$\overline{RD}$ to valid data delay (read)	t_{DDR}			100	ns	Figures 17 & 18
8	$\overline{RD}$, $\overline{WR}$ pulse width low	t_{PWL}	150			ns	Figures 16, 17 & 18
9	$\overline{RD}$, $\overline{WR}$ pulse width high	t_{PWH}		100		ns	Figures 16, 17 & 18
10	Data setup time (write)	t_{DSW}	45			ns	Figures 17 & 18
11	Data hold time (write)	t_{DHW}	10			ns	Figures 17 & 18
12	Input Capacitance (data bus)	C_{IN}		5		pF	
13	Output Capacitance ($\overline{IRQ}$/CP)	C_{OUT}		5		pF	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

NOTES: 1) dBm=decibels above or below a reference power of 1 mW into a 600 ohm load.
2) Digit sequence consists of all 16 DTMF tones.
3) Tone duration=40 ms. Tone pause=40 ms.
4) Nominal DTMF frequencies are used.
5) Both tones in the composite signal have an equal amplitude.
6) The tone pair is deviated by ± 1.5%±2 Hz.
7) Bandwidth limited (3 kHz) Gaussian noise.
8) The precise dial tone frequencies are 350 and 440 Hz (±2%).
9) Guaranteed by design and characterization. Not subject to production testing.
10) Referenced to the lowest amplitude tone in the DTMF signal.
11) For guard time calculation purposes.

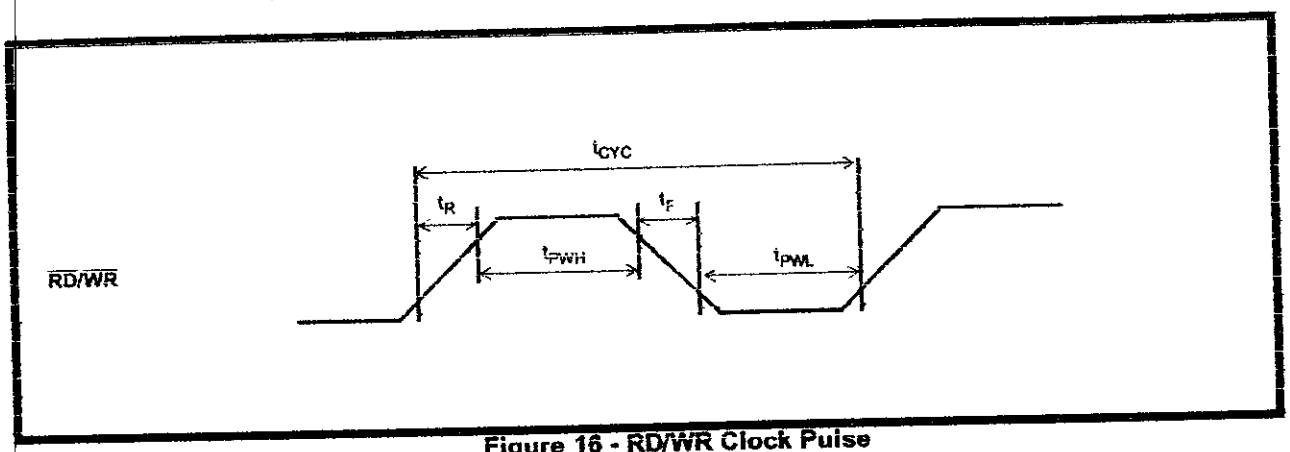


Figure 16 - RD/WR Clock Pulse

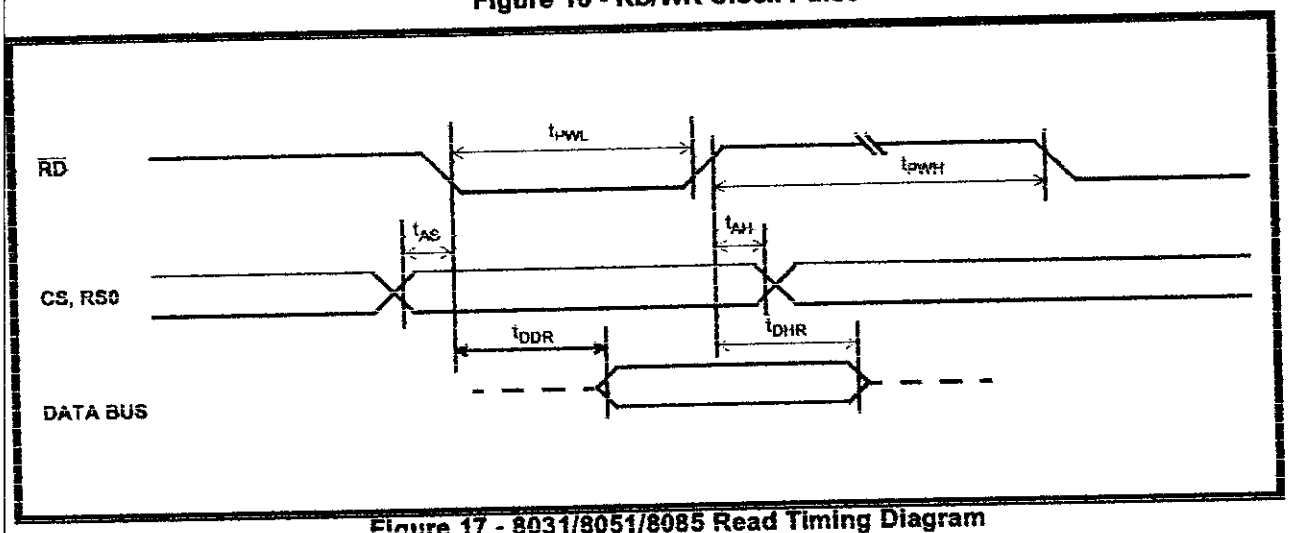


Figure 17 - 8031/8051/8085 Read Timing Diagram

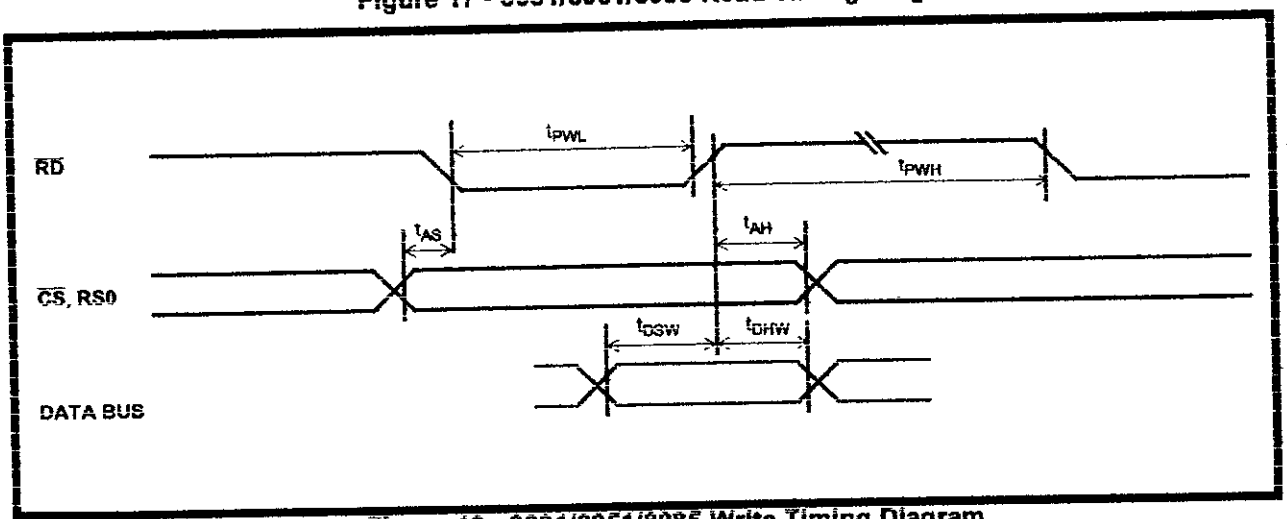
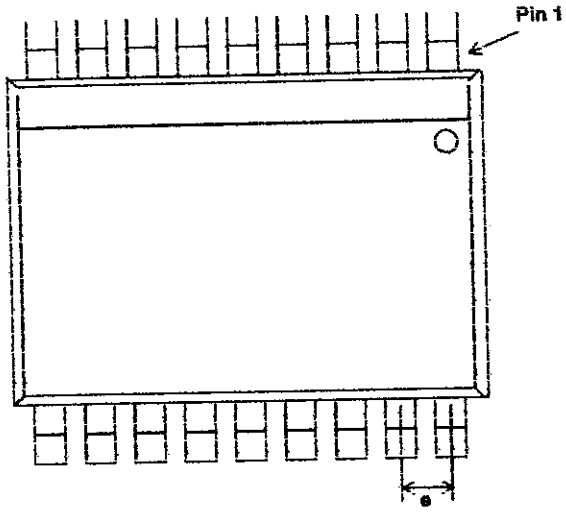
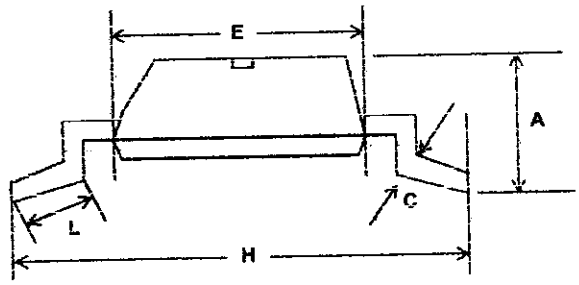
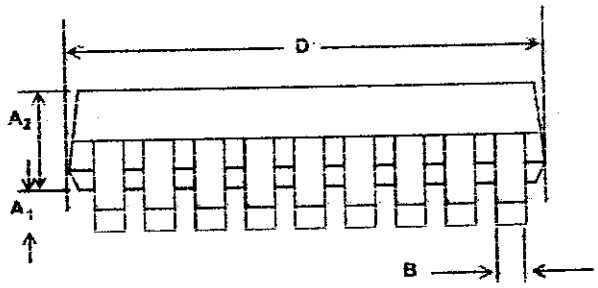


Figure 18 - 8031/8051/8085 Write Timing Diagram



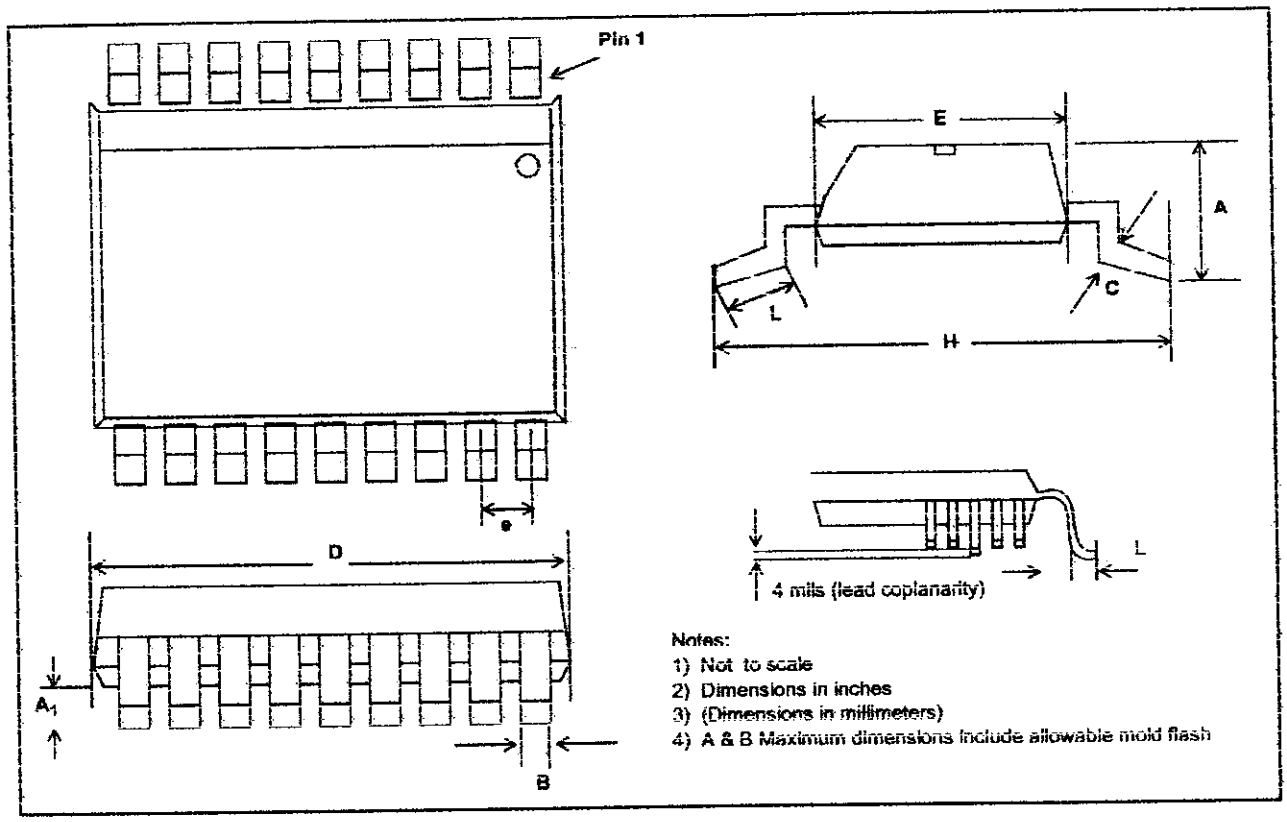




Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)
4) Ref. JEDEC Standard MO-150/M0118 for 48 Pin
5) A & B Maximum dimensions include allowable mold flash

Dim	20-Pin		24-Pin		28-Pin		48-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max
A		0.079 (2)	-	0.079 (2)		0.079 (2)	0.095 (2.41)	0.110 (2.79)
A_1	0.002 (0.05)		0.002 (0.05)		0.002 (0.05)		0.008 (0.2)	0.016 (0.406)
B	0.0087 (0.22)	0.013 (0.33)	0.0087 (0.22)	0.013 (0.33)	0.0087 (0.22)	0.013 (0.33)	0.008 (0.2)	0.0135 (0.342)
C		0.008 (0.21)		0.008 (0.21)		0.008 (0.21)		0.010 (0.25)
D	0.27 (6.9)	0.295 (7.5)	0.31 (7.9)	0.33 (8.5)	0.39 (9.9)	0.42 (10.5)	0.62 (15.75)	0.63 (16.00)
E	0.2 (5.0)	0.22 (5.6)	0.2 (5.0)	0.22 (5.6)	0.2 (5.0)	0.22 (5.6)	0.291 (7.39)	0.299 (7.59)
e	0.025 BSC (0.635 BSC)		0.025 BSC (0.635 BSC)		0.025 BSC (0.635 BSC)		0.025 BSC (0.635 BSC)	
A_2	0.065 (1.65)	0.073 (1.85)	0.065 (1.65)	0.073 (1.85)	0.065 (1.65)	0.073 (1.85)	0.089 (2.26)	0.099 (2.52)
H	0.29 (7.4)	0.32 (8.2)	0.29 (7.4)	0.32 (8.2)	0.29 (7.4)	0.32 (8.2)	0.395 (10.03)	0.42 (10.67)
L	0.022 (0.55)	0.037 (0.95)	0.022 (0.55)	0.037 (0.95)	0.022 (0.55)	0.037 (0.95)	0.02 (0.51)	0.04 (1.02)

Small Shrink Outline Package (SSOP) - N Suffix

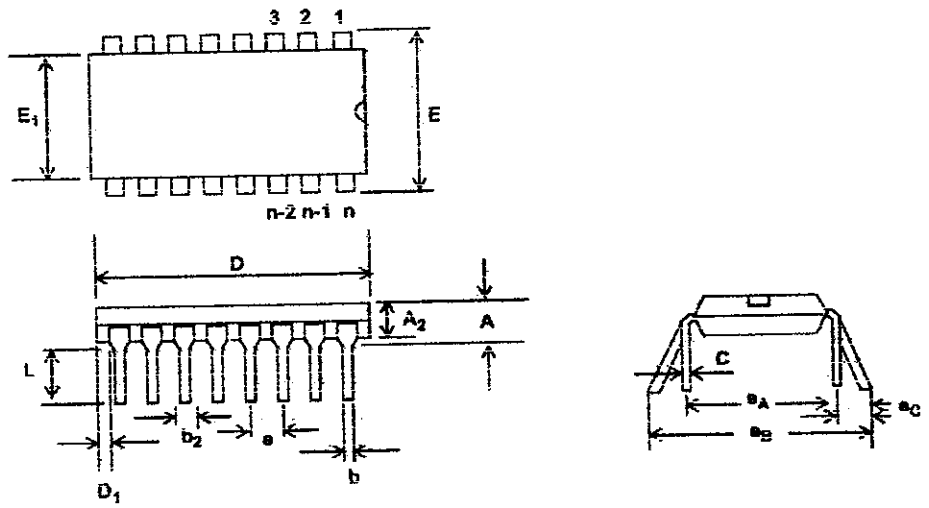


DIM	16-Pin		18-Pin		20-Pin		24-Pin		28-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)
A_1	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)
B	0.013 (0.33)	0.020 (0.51)	0.013 (0.33)	0.030 (0.51)	0.013 (0.33)	0.020 (0.51)	0.013 (0.33)	0.020 (0.51)	0.013 (0.33)	0.020 (0.51)
C	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)
D	0.398 (10.1)	0.413 (10.5)	0.447 (11.35)	0.4625 (11.75)	0.496 (12.60)	0.512 (13.00)	0.5985 (15.2)	0.614 (15.6)	0.697 (17.7)	0.7125 (18.1)
E	0.291 (7.40)	0.299 (7.40)	0.291 (7.40)	0.299 (7.40)	0.291 (7.40)	0.299 (7.40)	0.291 (7.40)	0.299 (7.40)	0.291 (7.40)	0.299 (7.40)
e	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
H	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)
L	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)

Lead SOIC Package - S Suffix

NOTES: 1. Controlling dimensions in parenthesis ( ) are in millimeters.
2. Converted inch dimensions are not necessarily exact.

Package Outlines

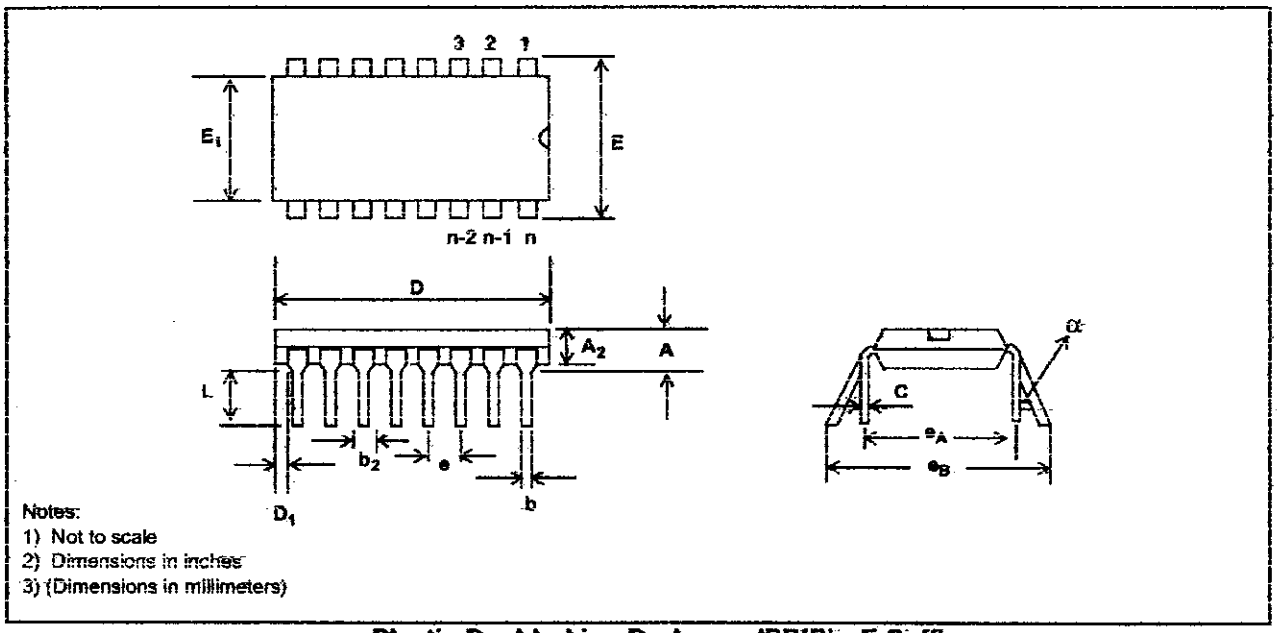


Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)

Plastic Dual-In-Line Packages (PDIP) - E Suffix

DIM	8-Pin		16-Pin		18-Pin		20-Pin	
	Plastic		Plastic		Plastic		Plastic	
	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)		0.210 (5.33)		0.210 (5.33)		0.210 (5.33)
A_2	0.115 (2.92)	0.195 (4.95)	0.115 (2.92)	0.195 (4.95)	0.115 (2.92)	0.195 (4.95)	0.115 (2.92)	0.195 (4.95)
b	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)
b_2	0.045 (1.14)	0.070 (1.77)	0.045 (1.14)	0.070 (1.77)	0.045 (1.14)	0.070 (1.77)	0.045 (1.14)	0.070 (1.77)
C	0.008 (0.203)	0.014 (0.356)	0.008 (0.203)	0.014(0.356)	0.008 (0.203)	0.014 (0.356)	0.008 (0.203)	0.014 (0.356)
D	0.355 (0.02)	0.400 (10.16)	0.780 (19.81)	0.800 (20.32)	0.880 (22.35)	0.920 (23.37)	0.980 (24.89)	1.060 (26.9)
D_1	0.005 (0.13)		0.005 (0.13)		0.005 (0.13)		0.005 (0.13)	
E	0.300 (7.62)	0.325 (8.26)	0.300 (7.62)	0.325 (8.26)	0.300 (7.62)	0.325 (8.26)	0.300 (7.62)	0.325 (8.26)
E_1	0.240 (6.10)	0.280 (7.11)	0.240 (6.10)	0.280 (7.11)	0.240 (6.10)	0.280 (7.11)	0.240 (6.10)	0.280 (7.11)
e	0.100 BSC (2.54)		0.100 BSC (2.54)		0.100 BSC (2.54)		0.100 BSC (2.54)	
e_A	0.300 BSC (7.62)		0.300 BSC (7.62)		0.300 BSC (7.62)		0.300 BSC (7.62)	
L	0.115 (2.92)	0.150 (3.81)	0.115 (2.92)	0.150 (3.81)	0.115 (2.92)	0.150 (3.81)	0.115 (2.92)	0.150 (3.81)
e_B		0.430 (10.92)		0.430 (10.92)		0.430 (10.92)		0.430 (10.92)
e_C	0	0.060 (1.52)	0	0.060 (1.52)	0	0.060 (1.52)	0	0.060 (1.52)

NOTE: Controlling dimensions in parenthesis ( ) are in millimeters.



Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)

Plastic Dual-In-Line Packages (PDIP) - E Suffix

DIM	22-Pin		24-Pin		28-Pin		40-Pin	
	Plastic		Plastic		Plastic		Plastic	
	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)		0.250 (6.35)		0.250 (6.35)		0.250 (6.35)
A_2	0.125 (3.18)	0.195 (4.95)	0.125 (3.18)	0.195 (4.95)	0.125 (3.18)	0.195 (4.95)	0.125 (3.18)	0.195 (4.95)
b	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)
b_2	0.045 (1.15)	0.070 (1.77)	0.030 (0.77)	0.070 (1.77)	0.030 (0.77)	0.070 (1.77)	0.030 (0.77)	0.070 (1.77)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.015 (0.381)
D	1.050 (26.67)	1.120 (28.44)	1.150 (29.3)	1.290 (32.7)	1.380 (35.1)	1.565 (39.7)	1.980 (50.3)	2.095 (53.2)
D_1	0.005 (0.13)		0.005 (0.13)		0.005 (0.13)		0.005 (0.13)	
E	0.390 (9.91)	0.430 (10.92)	0.600 (15.24)	0.670 (17.02)	0.600 (15.24)	0.670 (17.02)	0.600 (15.24)	0.670 (17.02)
E			0.290 (7.37)	0.320 (8.13)				
E_1	0.330 (8.39)	0.380 (9.65)	0.485 (12.32)	0.580 (14.73)	0.485 (12.32)	0.580 (14.73)	0.485 (12.32)	0.580 (14.73)
E_1			0.246 (6.25)	0.254 (6.45)				
e	0.100 BSC (2.54)		0.100 BSC (2.54)		0.100 BSC (2.54)		0.100 BSC (2.54)	
e_A	0.400 BSC (10.16)		0.600 BSC (15.24)		0.600 BSC (15.24)		0.600 BSC (15.24)	
e_A			0.300 BSC (7.62)					
e_B				0.430 (10.92)				
L	0.115 (2.93)	0.160 (4.06)	0.115 (2.93)	0.200 (5.08)	0.115 (2.93)	0.200 (5.08)	0.115 (2.93)	0.200 (5.08)
α		15°		15°		15°		15°

Shaded areas for 300 Mil Body Width 24 PDIP only

MITEL

SEMICONDUCTOR

http://www.mitelsemi.com

World Headquarters - Canada
Tel: +1 (613) 592 2122
Fax: +1 (613) 592 6909

North America
Tel: +1 (770) 486 0194
Fax: +1 (770) 631 8213

Asia/Pacific
Tel: +65 333 6193
Fax: +65 333 6192

Europe, Middle East, and Africa (EMEA)
Tel: +44 (0) 1793 518528
Fax: +44 (0) 1793 518581